CY28446

Clock Generator for Intel®Calistoga Chipset

Features

- **Compliant to Intel® CK410M**
- **Selectable CPU frequencies**
- **Low power differential CPU clock pairs**
- **100 MHz Low power differential SRC clocks**
- **96 MHz Low power differential DOT clock**
- **48 MHz USB clock**
- **SRC clocks stoppable through OE#**
- **33 MHz PCI clocks**
- **Buffered 14.318 MHz reference clock**
- **Low-voltage frequency select input**
- **I^2C support with readback capabilities**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **3.3V Power supply**
- **64 pin QFN package**

Table 1. Output Configuration Table

CPU	SRC	PCI	REF	DOT96	48M
x2/x3	x9/10	x5	x1	x 1	x 1

Pin Configuration

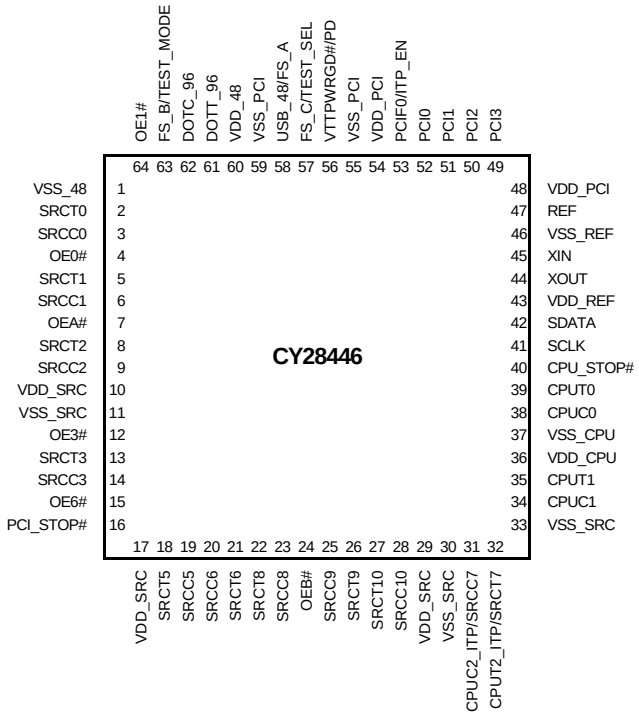

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Table 2. Frequency Table

FS_C	FS_B	FS_A	CPU	SRC/SATA	PCIF/PCI	REF	LCD	DOT96	USB
MID	0	1	100	100	33	14.318	100	96	48
0	0	1	133	100	33	14.318	100	96	48
0	1	1	166	100	33	14.318	100	96	48
0	1	0	200	100	33	14.318	100	96	48
0	0	0							
MID	0	0							
MID	1	0							
MID	1	1	Reserved	100	33	14.318	100	96	
1	0	x	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	1	0	REF/2	REF/8	REF/24	REF	REF/8	REF	REF
1	1	1	REF/2	REF/8	REF/24	REF	REF/8	REF	REF

Pin Description

Pin No.	Name	Type	Description
1	VSS_48	GND	**Ground for outputs**.
2, 3, 5, 6, 8, 9, 13, 14, 18, 19, 20, 21, 22, 23, 25, 26, 27, 28	SRC(0:3, 5:6, 8:10) [T/C]	O, DIF	**100 MHz Differential serial reference clocks**
4, 7, 12, 15, 24, 64	OE[0, 1, 3, 6, A, B]#	I, PU	**3.3V LVTTL input for enabling assigned SRC clock (active LOW)**
10, 17, 29,	VDD_SRC	PWR	**3.3V power supply for outputs**.
11, 30, 33	VSS_SRC	GND	**Ground for outputs**.
16	PCI_STP#	I, PU	**3.3V LVTTL input for PCI_STP#** Stops SRC and PCI clocks not set to free running in the SMBUS registers.
31, 32	CPU2_ITPT/SRCT7, CPU2_ITPC/SRCC7	O, DIF	**Selectable differential CPU clock/100 MHz Differential serial reference clock**. Selectable via Pin 53 PCIF0/ITP_EN
34, 35, 38, 39	CPUT/C[0:1]	O, DIF	**Differential CPU clock outputs**.
36	VDD_CPU	PWR	**3.3V power supply for outputs**.
37	VSS_CPU	GND	**Ground for outputs**.
40	CPU_STP#	I, PU	**3.3V LVTTL input for CPU_STP# active LOW**.
41	SCLK	I	**SMBus-compatible SCLOCK**.
42	SDATA	I/O, OD	**SMBus-compatible SDATA**.
43	VDD_REF	PWR	**3.3V power supply for outputs**.
44	XOUT	O, SE	**14.318 MHz crystal output**.
45	XIN	I	**14.318 MHz crystal input**.
46	VSS_REF	GND	**Ground for outputs**.
47	REF	O,SE	**Fixed 14.318 MHz clock output**.
48, 54	VDD_PCI	PWR	**3.3V power supply for outputs**.
49, 50, 51, 52	PCI[0:3]	O, SE	**33 MHz clock output**
53	PCIF0/ITP_EN	I/O, PD	**33 MHz clock output (not stoppable by PCI_STOP#)/3.3V LVTTL input for selecting pins 31/32 (CPU2_ITP[T/C]/SRC7[T/C])** (sampled on the VTT_PWRGD# assertion). 0 (default): SRC7[T/C] 1: CPU2_ITP[T/C]
55, 59	VSS_PCI	GND	**Ground for outputs**.
56	VTT_PWRGD#/PD	I, PD	**3.3V LVTTL input.** This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C, and all I/O configuration pins,. After VTT_PWRGD# (active LOW) assertion, this pin becomes a real-time input for asserting power-down (active HIGH).
57	FS_C/TEST_SEL	I, PD	**3.3V-tolerant input for CPU frequency selection/Selects test mode if pulled to V_{IMFS_C} when VTT_PWRGD# is asserted LOW**. *Refer to DC Electrical Specifications table for V_{ILFS_C},V_{IMFS_C},V_{IHFS_C} specifications.*
58	USB_48/FS_A	I/O, PU	**Fixed 48 MHz clock output/3.3V-tolerant input for CPU frequency selection**. Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.
60	VDD_48	PWR	**3.3V power supply for outputs**.
61,62	DOT_96[T/C]	O, DIF	**Fixed 96 MHz clock output**.
63	FS_B/TEST_MODE	I, PU	**3.3V-tolerant input for CPU frequency selection Selects Ref/N or Tri-state when in test mode** 0 = Tri-state, 1 = Ref/N *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*

Frequency Select Pins (FS_A, FS_B, and FS_C)

Apply the appropriate logic levels to FSA, FSB, and FSC before CK-PWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CK-PWRGD and indicates that VTT voltage is stable then FSA, FSB, and FSC input values are sampled. This process employs a one-shot functionality and once the CK-PWRGD sampled a valid HIGH, all other FSA, FSB, FSC and CK-PWRGD transitions are ignored except in test mode

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up, making this interface optional. Clock device register changes are made at system initialization if required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after complete byte has been transferred. For byte write and byte read operations, the system controller accesses individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3*.

The block write and block read protocol is outlined in *Table 4* while *Table 5* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 3. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation.
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'.

Table 4. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits (Skip this step if I^2C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	1	CPU2_ITP[T/C]/SRC7[T/C]	CPU2_ITP[T/C]/SRC[T/C]7 Output Enable 0 = Disable (Tri-state), 1 = Enable
6	1	SRC[T/C]6	SRC[T/C]6 Output Enable 0 = Disable (Tri-state), 1 = Enable
5	1	SRC[T/C]5	SRC[T/C]5 Output Enable 0 = Disable (Tri-state), 1 = Enable
4	1	Reserved	Reserved
3	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Tri-state), 1 = Enable
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Tri-state), 1 = Enable
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enable
0	1	SRC[T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Tri-state), 1 = Enable

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	PCIF0	PCIF0 Output Enable 0 = Disable, 1 = Enable
6	1	DOT_96[T/C]	DOT_96 MHz Output Enable 0 = Disable (Tri-state), 1 = Enable
5	1	USB_48	USB_48 Output Enable 0 = Disable, 1 = Enable
4	1	REF	REF Output Enable 0 = Disable, 1 = Enable
3	1	Reserved	Reserved
2	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Tri-state), 1 = Enable
1	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Tri-state), 1 = Enable

Byte 1: Control Register 1

Bit	@Pup	Name	Description
0	0	CPU PLL Spread Enable	PLL1 (CPU PLL) Spread Spectrum Enable 0 = Spread off 1 = Spread on (–0.5% spread spectrum on CPU/SRC/PCI clocks)

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	Reserved	Reserved set to 1
6	1	Reserved	Reserved set to 1
5	1	PCI3	PCI3 Output Enable 0 = Disable, 1 = Enable
4	1	PCI2	PCI2 Output Enable 0 = Disable, 1 = Enable
3	1	PCI1	PCI1Output Enable 0 = Disable, 1 = Enable
2	1	PCI0	PCI0 Output Enable 0 = Disable, 1 = Enable
1	1	Reserved	Reserved set to 1
0	1	Reserved	Reserved set to 1

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	0	SRC7	Allow control of SRC[T/C]7 with assertion of OEB# 0 = Free running, 1 = Stopped with OEB#
6	0	Reserved	Reserved set to 0
5	0	SRC5	Allow control of SRC[T/C]5 with assertion of OEB# 0 = Free running, 1 = Stopped with OEB#
4	0	Reserved	Reserved set to 0
3	0	Reserved	Reserved set to 0
2	0	SRC2	Allow control of SRC[T/C]2 with assertion of OEB# 0 = Free running, 1 = Stopped with OEB#
1	0	Reserved	Reserved set to 0
0	0	Reserved	Reserved set to 0

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	1	Reserved	Reserved set to 1
6	0	DOT96[T/C]	DOT PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
5	0	Reserved	Reserved set to 0
4	1	Reserved	Reserved set to 1
3	0	PCIF0	Allow control of PCIF0 with assertion of SW and HW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	1	CPU[T/C]2	Allow control of CPU[T/C]2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
1	1	CPU[T/C]1	Allow control of CPU[T/C]1 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
0	1	CPU[T/C]0	Allow control of CPU[T/C]0 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	Reserved	Reserved set to 0
6	0	CPU[T/C]2	CPU[T/C]2 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Tri-state when CPU_STP# asserted
5	0	CPU[T/C]1	CPU[T/C]1 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Tri-state when CPU_STP# asserted
4	0	CPU[T/C]0	CPU[T/C]0 Stop Drive Mode 0 = Driven when CPU_STP# asserted, 1 = Tri-state when CPU_STP# asserted
3	0	SRC[T/C]	SRC[T/C] PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Tri-state when PD asserted
2	0	CPU[T/C]2	CPU[T/C]2 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Tri-state when PD asserted
1	0	CPU[T/C]1	CPU[T/C]1 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Tri-state when PD asserted
0	0	CPU[T/C]0	CPU[T/C]0 PWRDWN Drive Mode 0 = Driven when PD asserted, 1 = Tri-state when PD asserted

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	REF/N or Tri-state Select	REF/N or Tri-state Select 1 = REF/N, 0 = Tri-state
6	0	Test Mode	Test Mode Control 1 = Ref/N or Tristate, 0 = Normal Operation
5	1	Reserved	Reserved set to 1
4	0	REF	REF Output Drive Strength 0 = Low, 1 = High
3	1	PCI and PCIF clock outputs except those set to free running	SW PCI_STP Function 0 = SW PCI_STP assert, 1 = SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI and PCIF outputs are stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI and PCIF outputs resumes in a synchronous manner with no short pulses.
2	HW	FS_C	FSC Reflects the value of the FS_C pin sampled on power-up 0 = FSC was low during VTT_PWRGD# assertion
1	HW	FS_B	FSB Reflects the value of the FS_B pin sampled on power-up 0 = FSB was low during VTT_PWRGD# assertion
0	HW	FS_A	FSA Reflects the value of the FS_A pin sampled on power-up 0 = FSA was low during VTT_PWRGD# assertion

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Revision Code Bit 3	Revision Code Bit 3
6	0	Revision Code Bit 2	Revision Code Bit 2
5	1	Revision Code Bit 1	Revision Code Bit 1
4	1	Revision Code Bit 0	Revision Code Bit 0
3	1	Vendor ID Bit 3	Vendor ID Bit 3
2	0	Vendor ID Bit 2	Vendor ID Bit 2
1	0	Vendor ID Bit 1	Vendor ID Bit 1
0	0	Vendor ID Bit 0	Vendor ID Bit 0

Byte 8: Control Register 7

Bit	@Pup	Name	Description
7	0	Reserved	Reserved set to 0
6	1	SRC[T/C]10	SRC[T/C]10 Output Enable 0 = Disable (Tri-state), 1 = Enable
5	1	SRC[T/C]9	SRC[T/C]9 Output Enable 0 = Disable (Tri-state), 1 = Enable
4	1	SRC[T/C]8	SRC[T/C]8 Output Enable 0 = Disable (Tri-state), 1 = Enable
3	0	Reserved	Reserved set to 0
2	0	SRC10	Allow control of SRC[T/C]10 with assertion of OEA# 0 = Free running, 1 = Stopped with OEA#
1	0	SRC9	Allow control of SRC[T/C]9 with assertion of OEB# 0 = Free running, 1 = Stopped with OEB#
0	0	SRC8	Allow control of SRC[T/C]8 with assertion of OEA# 0 = Free running, 1 = Stopped with OEA#

Byte 9: Control Register 8

Bit	@Pup	Name	Description
7	0	PCI3	33-MHz Output drive strength 0 = Low, 1 = High
6	0	PCI2	33-MHz Output drive strength 0 = Low, 1 = High
5	0	PCI1	33-MHz Output drive strength 0 = Low, 1 = High
4	0	PCI0	33-MHz Output drive strength 0 = Low, 1 = High
3	0	PCIF0	33-MHz Output drive strength 0 = Low, 1 = High
2	1	Reserved	Reserved set to 1
1	1	Reserved	Reserved set to 1
0	1	Reserved	Reserved set to 1

Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The CY28446 requires a Parallel Resonance Crystal. Substituting a series resonance crystal causes the CY28446 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal. It is not true that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal.

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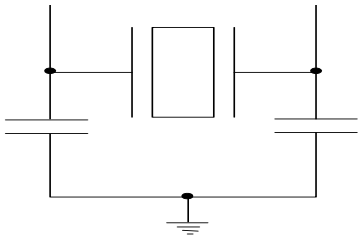

Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side

is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

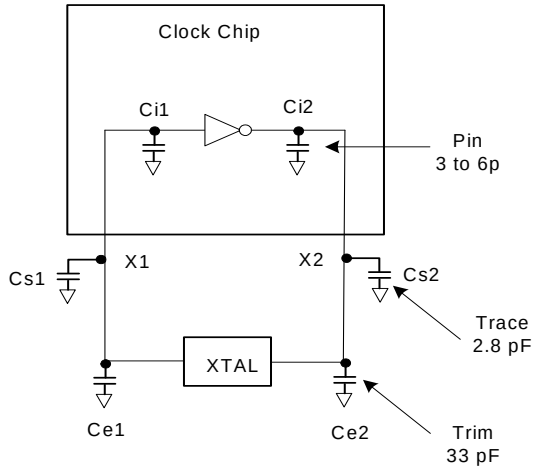

Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL.....Crystal load capacitance

CLe..... Actual loading seen by crystal using standard value trim capacitors

Ce..... External trim capacitors

Cs.....Stray capacitance (terraced)

Ci .....Internal capacitance (lead frame, bond wires etc.)

OE# Description

The OE# signals are active LOW inputs used for clean enabling and disabling selected SRC outputs. The outputs controlled by OE[A,B]# are determined by the settings in register byte 3 and byte 8. OE[0,1,3,6]# controls SRC[0,1,3,6], respectively. The OE# signal is a debounced signal and its state must remain unchanged during two consecutive rising edges of SRCC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

OE# Assertion (OE# -> LOW)

All differential stopped outputs resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2 and 6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously. All stopped SRC outputs must be driven HIGH within 10 ns of OE# deassertion to a voltage er than 200 mV.

OE# Deassertion (OE# -> HIGH)

The impact of deasserting the OE# pins is that all SRC outputs that are set in the control registers to stoppable via deassertion of OE# are stopped after their next transition. The final state of all stopped SRC clocks is Low/low.

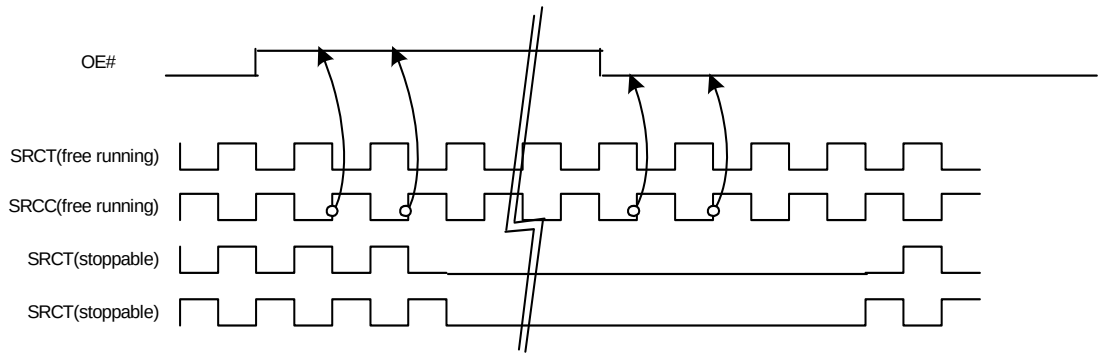

Figure 3. OE# Deassertion/Assertion Waveform

PD (Power down) Clarification

The CKPWRGD/PWRDWN# pin is a dual-function pin. During initial power-up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internal to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, all clocks need to be driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PD (Power down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held HIGH or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# HIGH-to-LOW transition within 4 clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to ‘0’, the clock output are held with “Diff clock” pin driven HIGH and “Diff clock#” driven LOW. If the control register PD drive mode bit corresponding to the output of interest is programmed to “1”, then both the “Diff clock” and the “Diff clock#” are LOW. *Figure 4* shows CPUT = 133 MHz and PD drive mode = ‘1’ for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166 and 200 MHz. If PD mode has the initial power-on state, PD must be asserted HIGH in less than 10 µs after asserting Vtt_PwrGd#. The 96_100_SSC follows the DOT waveform selected for 96 MHz and the SRC waveform in 100 MHz mode.

PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power-down will be driven HIGH in less than 300 µs of PD deassertion to a voltage greater than 200 mV. After the clock chip’s internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. *Figure 5* is an example showing the relationship of clocks coming up. It should be noted that 96_100_SSC will follow the DOT waveform is selected for 96 MHz and the SRC waveform when in 100-MHz mode.

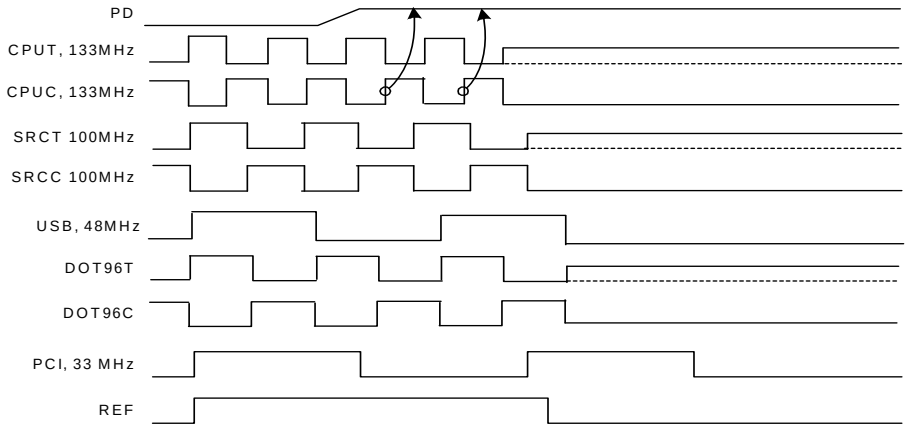

Figure 4. Power down Assertion Timing Waveform

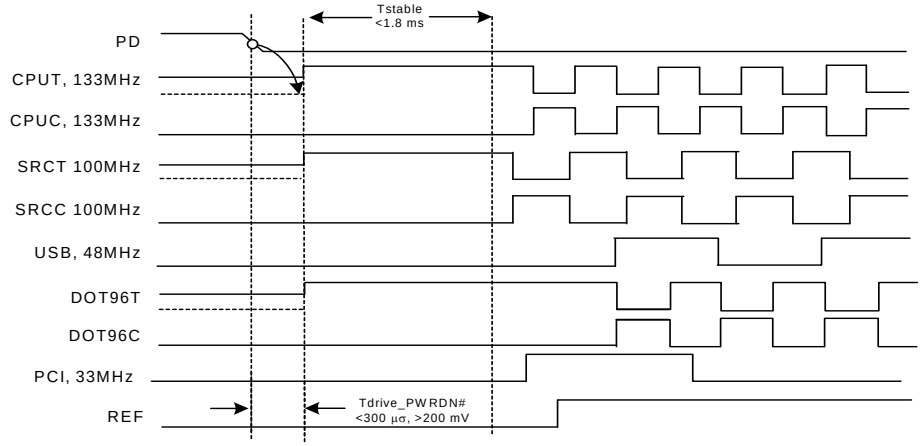

Figure 5. Power-down Deassertion Timing Waveform

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped within two to six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final state of all stopped CPU clocks is High/Low when driven, Low/Low when tri-stated

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner, synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

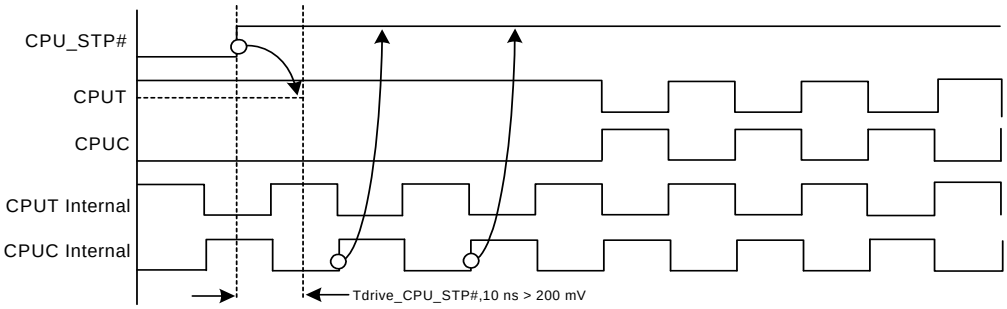

Figure 6. CPU_STP# Deassertion Waveform

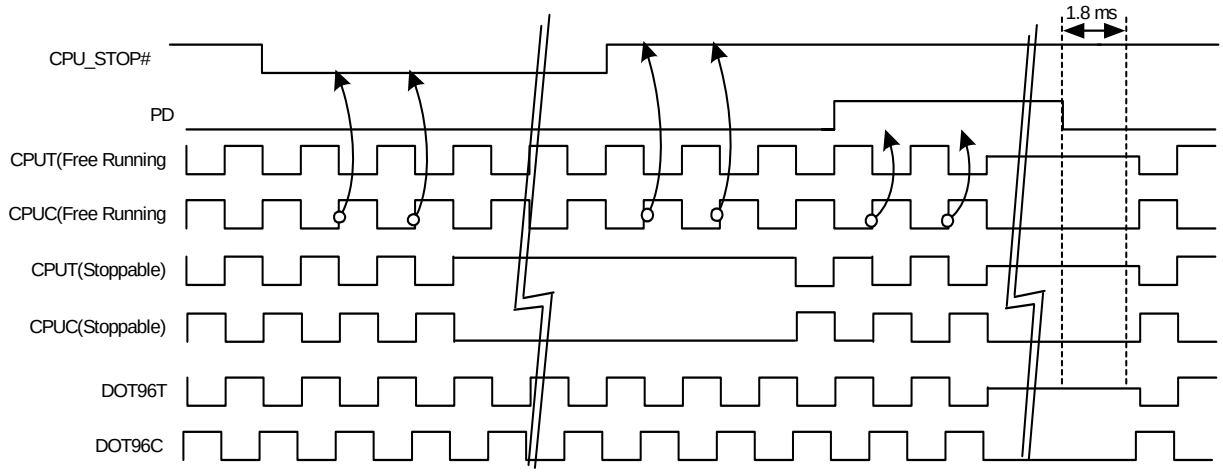

Figure 7. CPU_STP#= Driven, CPU_PD = Driven, DOT_PD = Driven

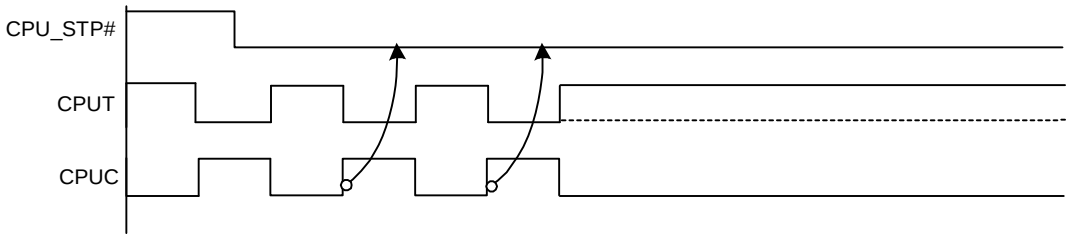

Figure 8. CPU_STP# Assertion Waveform

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See *Figure 10*.) The PCIF clocks will not be affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running.

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a high level.

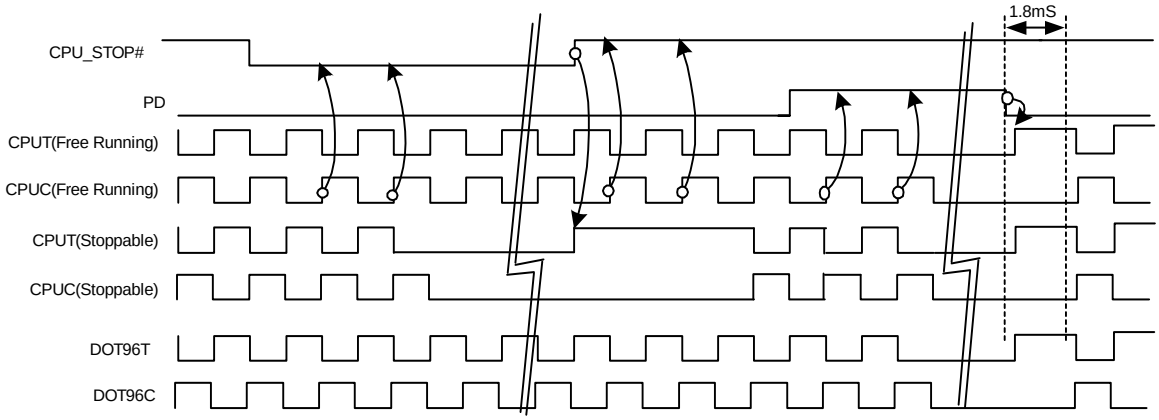

Figure 9. CPU_STP# = Tri-state, CPU_PD = Tri-state, DOT_PD = Tri-state

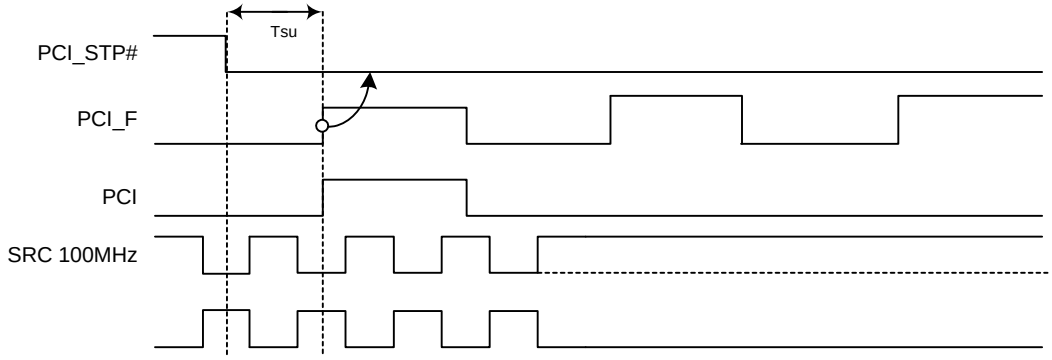

Figure 10. PCI_STP# Assertion Waveform

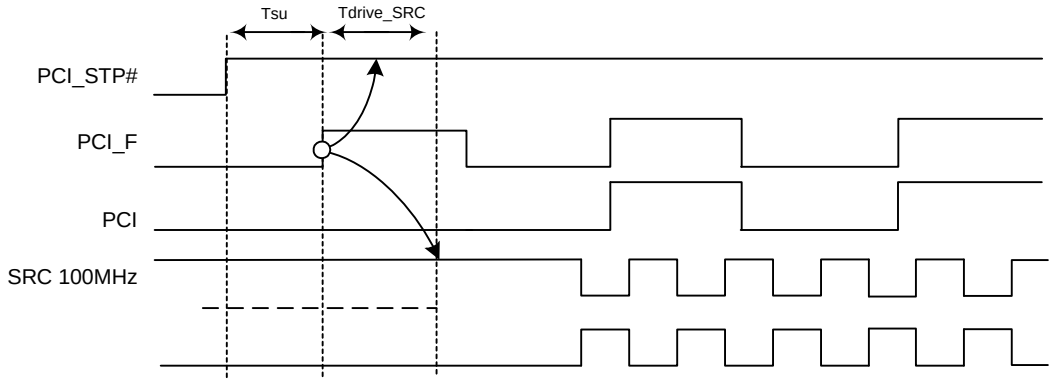

Figure 11. PCI_STP# Deassertion Waveform

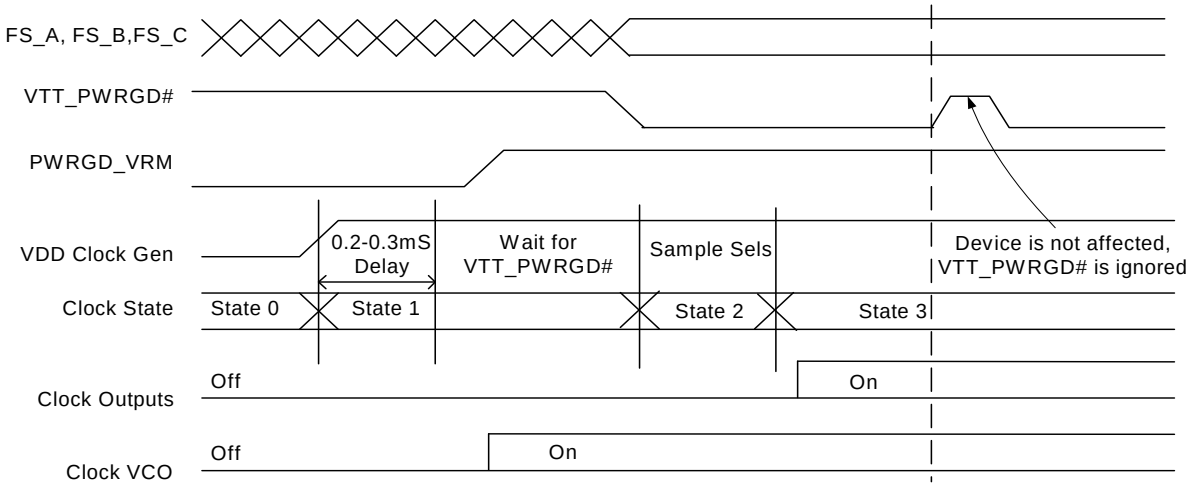

Figure 12. VTT_PWRGD# Timing Diagram

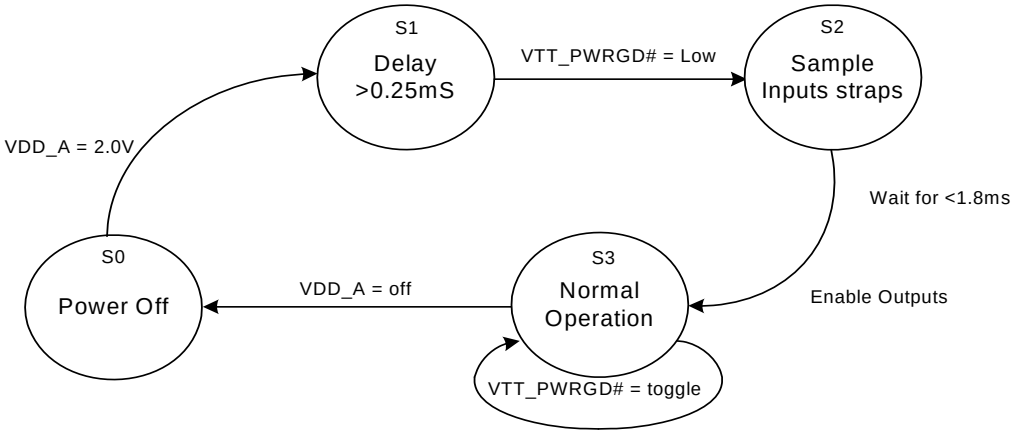

Figure 13. Clock Generator Power-up/Run State Diagram

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DD_A}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-STD-883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
All V_{DD}s	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL_FS}	FS_[A,B] Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IH_FS}	FS_[A,B] Input High Voltage		0.7	V_{DD} + 0.5	V
V_{ILFS_C}	FS_C Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IMFS_C}	FS_C Input Middle Voltage	Typical	0.7	1.7	V
V_{IHFS_C}	FS_C Input High Voltage	Typical	2.0	V_{DD} + 0.5	V
V_{IL}	3.3V Input Low Voltage		V_{SS} – 0.3	0.8	V
V_{IH}	3.3V Input High Voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, 0 < V_{IN} < V_{DD}	–5	5	µA
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, 0 < V_{IN} < V_{DD}	–	5	µA
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	3.3V Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High-impedance Output Current	Single-ended output	–10	10	µA
I_{OZL}	High-impedance Output Current	Differnetial output	-100	100	µA
C_{IN}	Input Pin Capacitance		3	5	pF
C_{OUT}	Output Pin Capacitance		3	6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
$I_{DD3.3V}$	Dynamic Supply Current	At max. load and freq. per *Figure 15*	–	250	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Driven	–	70	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Tri-state	–	5	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R/T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-µs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
CPU at 0.7V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
T_{PERIOD}	133-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	7.497751	7.502251	ns
T_{PERIOD}	166-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	5.998201	6.001801	ns
T_{PERIOD}	200-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	4.998500	5.001500	ns
$T_{PERIODSS}$	100-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODSS}$	133-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	7.497751	7.539950	ns
$T_{PERIODSS}$	166-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	5.998201	6.031960	ns
$T_{PERIODSS}$	200-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	4.998500	5.026634	ns
$T_{PERIODAbs}$	100-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	9.912001	10.08800	ns
$T_{PERIODAbs}$	133-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	7.412751	7.587251	ns
$T_{PERIODAbs}$	166-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	5.913201	6.086801	ns
$T_{PERIODAbs}$	200-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	4.913500	5.086500	ns
$T_{PERIODSSAbs}$	100-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	9.912001	10.13827	ns
$T_{PERIODSSAbs}$	133-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	7.412751	7.624950	ns
$T_{PERIODSSAbs}$	166-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	5.913201	6.116960	ns
$T_{PERIODSSAbs}$	200-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	4.913500	5.111634	ns
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	100	ps
T_{CCJ2}	CPU2_ITP Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	Long-term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at crossing point V_{OX}	–	150	ps
T_R/T_F	CPUT and CPUC Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	155	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		180	550	mV

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15*. Measure SE	–	0.2	V
SRC at 0.7V					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100-MHz SRCT and SRCC Absolute Period	Measured at crossing point V_{OX}	9.872001	10.12800	ns
$T_{PERIODSSAbs}$	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	370	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R/T_F	SRCT and SRCC Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	165	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		180	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15.* Measure SE	–	0.2	V
DOT96 at 0.7V					
T_{DC}	DOT96T and DOT96C Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	DOT96T and DOT96C Period	Measured at crossing point V_{OX}	10.41354	10.41979	ns
$T_{PERIODAbs}$	DOT96T and DOT96C Absolute Period	Measured at crossing point V_{OX}	10.16354	10.66979	ns
T_{CCJ}	DOT96T/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	250	ps
L_{ACC}	DOT96T/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R/T_F	DOT96T and DOT96C Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	155	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		180	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
V_{RB}	Ring Back Voltage	See *Figure 15.* Measure SE	–	0.2	V
PCI/PCIF at 3.3V					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99100	30.00900	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.9910	30.15980	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49100	30.50900	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.49100	30.65980	ns
T_{HIGH}	PCIF and PCI high time	Measurement at 2.4V	12.0	–	ns
T_{LOW}	PCIF and PCI low time	Measurement at 0.4V	12.0	–	ns
T_R/T_F	PCIF/PCI rising and falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	500	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	PCIF/PCI Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
48_M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	48_M High time	Measurement at 2.4V	8.09	11.3	ns
T_{LOW}	48_M Low time	Measurement at 0.4V	7.694	11.3	ns
T_R/T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L_{ACC}	48M Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
REF at 3.3V					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T_R/T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	–	500	ps
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	300	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns
T_{SH}	Stopclock Hold Time		0	–	ns

Test and Measurement Set-up

For PCI Single-ended Signals and Reference

The following diagram shows the test load configuration of single-ended PCI, USB output signals.

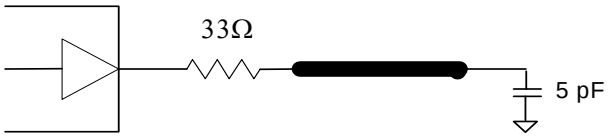

Figure 14. Single-ended PCI, USB Load Configuration

The following diagram shows the test load configuration for the differential CPU and SRC outputs.

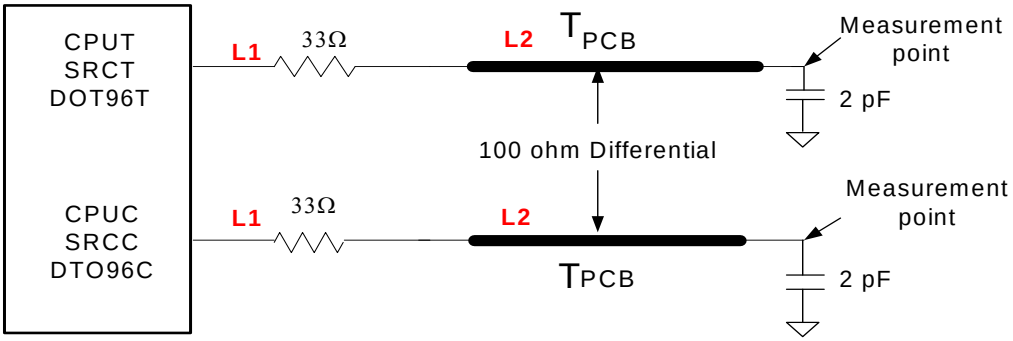

Figure 15. 0.7V Differential Load Configuration

3.3V signals

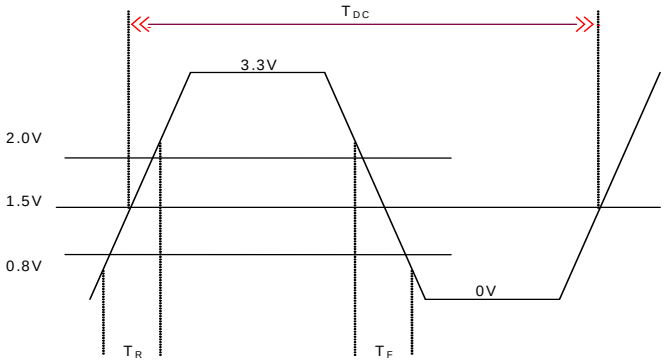

Figure 16. Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
CY28446LFXC	64-pin QFN	Commercial, 0° to 70°C
CY28446LFXCT	64-pin QFN—Tape and Reel	Commercial, 0° to 70°C

Package Diagram

64-Lead QFN 9 x 9 mm (Punch Version) LF64A