

N-channel 600 V, 0.078 Ω typ., 34 A MDmesh M2
Power MOSFETs in TO-220FP, I²PAKFP and TO-3PF packages

Datasheet – production data

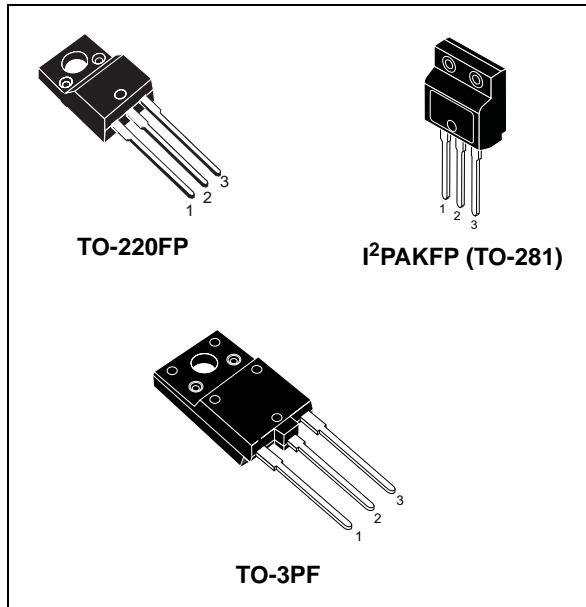
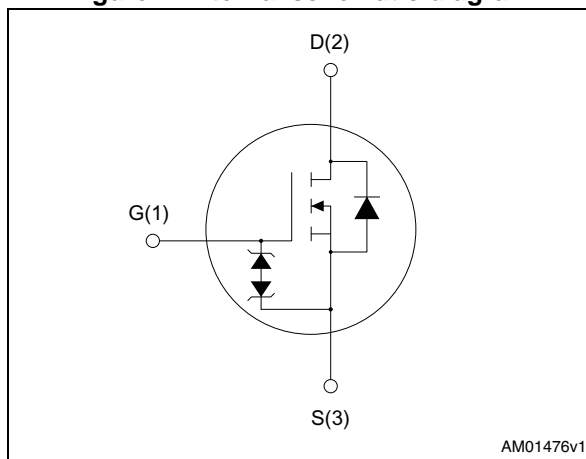


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS} @ T _{Jmax}	R _{DS(on)} max	I _D
STF40N60M2	650 V	0.088 Ω	34 A
STFI40N60M2			
STFW40N60M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packing
STF40N60M2	40N60M2	TO-220FP	Tube
STFI40N60M2		I ² PAKFP (TO-281)	
STFW40N60M2		TO-3PF	

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves) 6
- 3 Test circuits 9**
- 4 Package information 10**
 - 4.1 TO-220FP, package information11
 - 4.2 I²PAKFP (TO-281) package information 13
 - 4.3 TO-3PF, package information 15
- 5 Revision history 17**

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP, I ² PAKFP	TO-3PF	
V _{GS}	Gate-source voltage	± 25		V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	34		A
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	22		A
I _{DM} ^{(1),(2)}	Drain current (pulsed)	136		A
P _{TOT}	Total dissipation at T _C = 25 °C	40	63	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)	2500	3500	V
T _{stg}	Storage temperature range	- 55 to 150		°C
T _j	Operating junction temperature range			°C

- Limited by maximum junction temperature
- Pulse width limited by safe operating area.
- I_{SD} ≤ 34 A, di/dt ≤ 400 A/μs; V_{DS peak} < V_{(BR)DSS}; V_{DD}=400 V.
- V_{DS} ≤ 480 V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP, I ² PAKFP	TO-3PF	
R _{thj-case}	Thermal resistance junction-case	3.13	2.00	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5	50	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	6	A
E _{AS}	Single pulse avalanche energy (starting T _j =25°C, I _D = I _{AR} ; V _{DD} =50 V)	500	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current ()	$V_{GS} = 0, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 17\text{ A}$		0.078	0.088	Ω

1. Defined by design, not subject to production test

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	2500	-	pF
C_{oss}	Output capacitance		-	117	-	pF
C_{rss}	Reverse transfer capacitance		-	2.4	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	342	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	4.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 34\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 17: Gate charge test circuit)	-	57	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain charge		-	25.5	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 34\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16: Switching times test circuit for resistive load and Figure 21: Switching time waveform)	-	20.5	-	ns
t_r	Rise time		-	13.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	96	-	ns
t_f	Fall time		-	11	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	34		A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	136		A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 34\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 34\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 18: Test circuit for inductive load switching and diode recovery times)	-	440		ns
Q_{rr}	Reverse recovery charge		-	8.2		μC
I_{RRM}	Reverse recovery current		-	37		A
t_{rr}	Reverse recovery time	$I_{SD} = 34\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18: Test circuit for inductive load switching and diode recovery times)	-	568		ns
Q_{rr}	Reverse recovery charge		-	11.5		μC
I_{RRM}	Reverse recovery current		-	40.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP and I²PAKFP

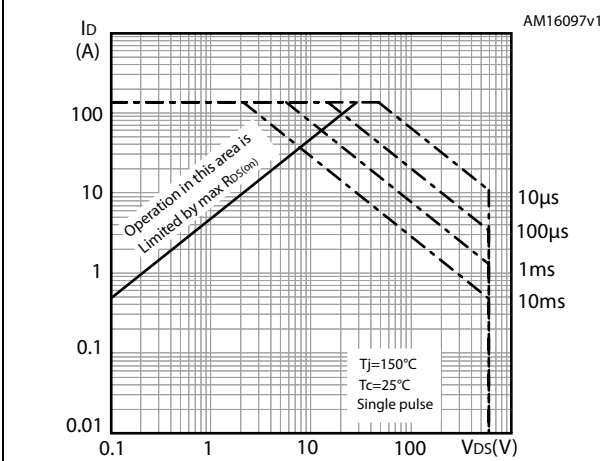


Figure 3. Thermal impedance for TO-220FP and I²PAKFP

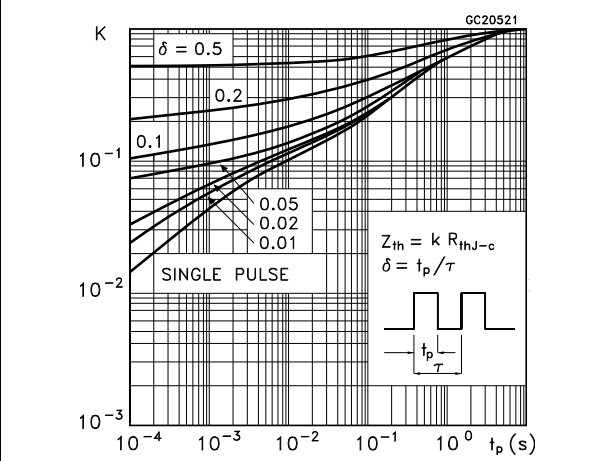


Figure 4. Safe operating area for TO-3PF

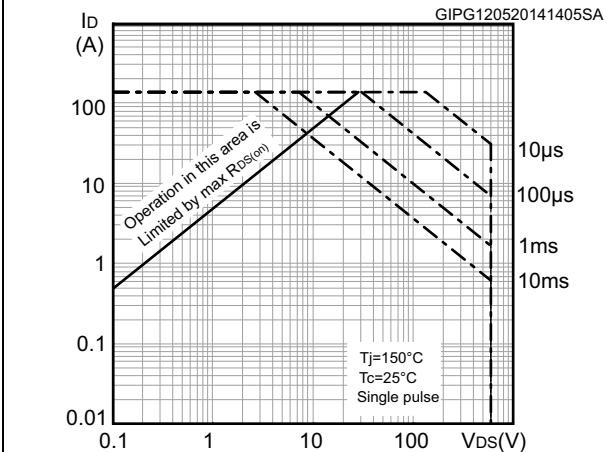


Figure 5. Thermal impedance for TO-3PF

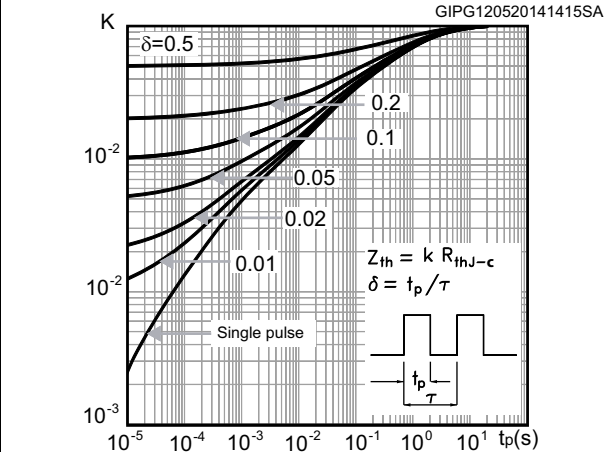


Figure 6. Output characteristics

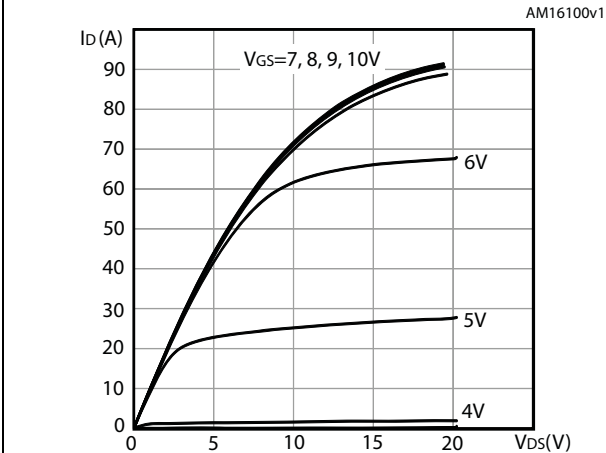
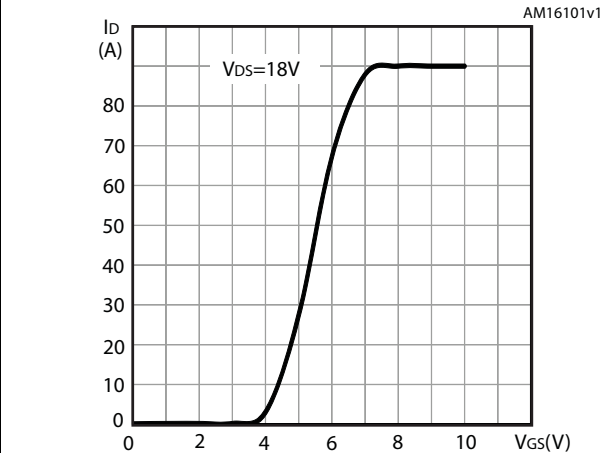


Figure 7. Transfer characteristics



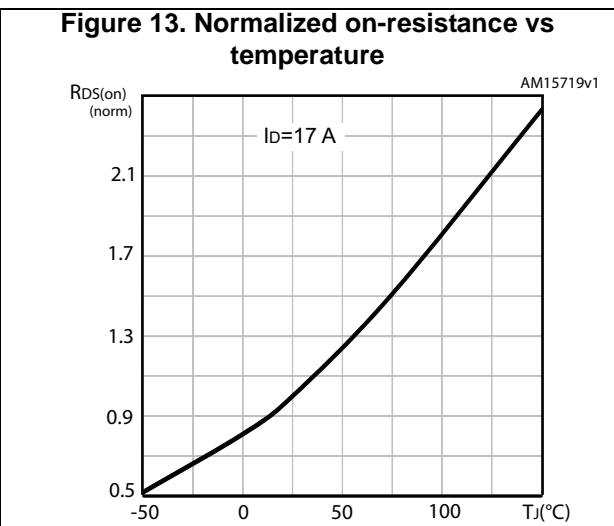
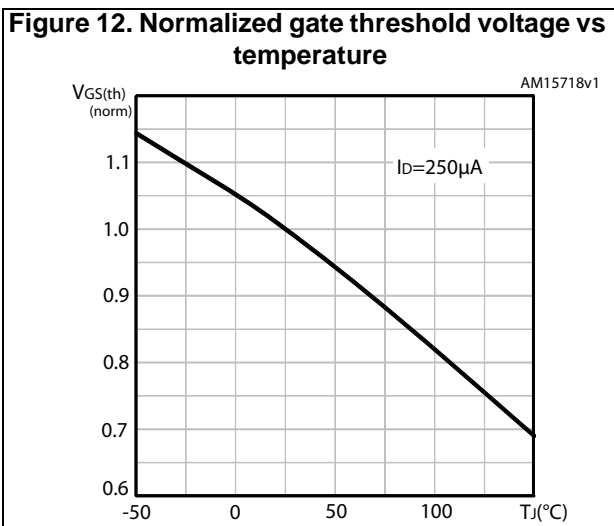
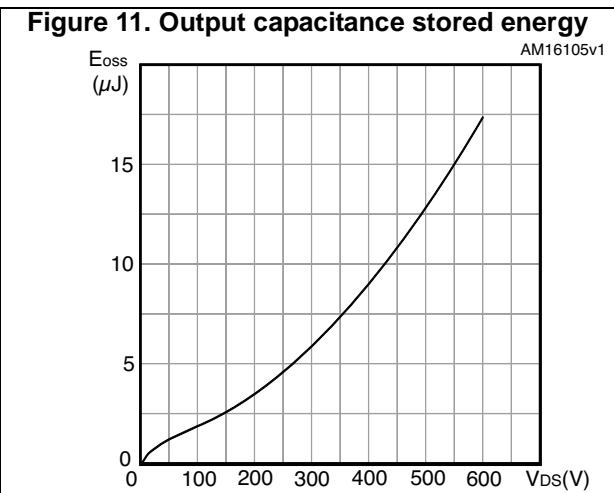
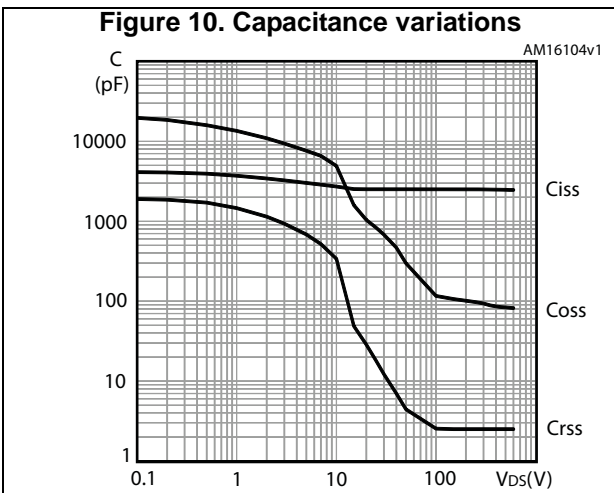
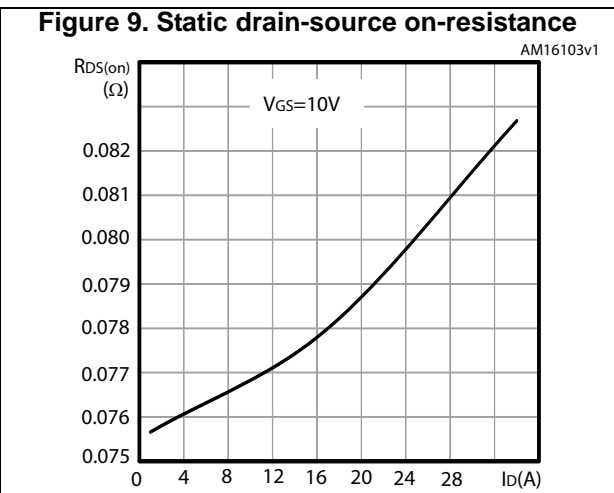
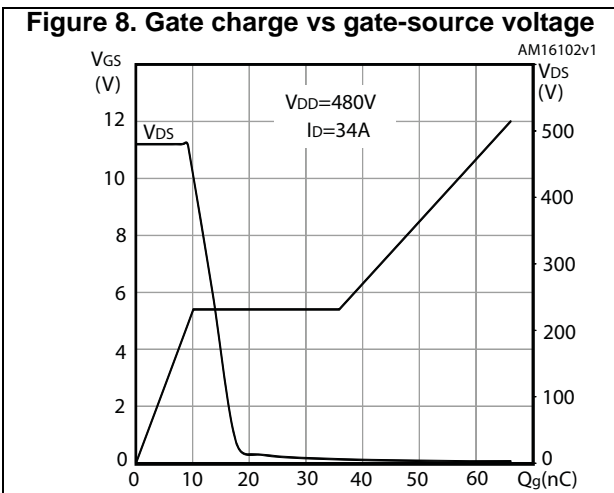


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

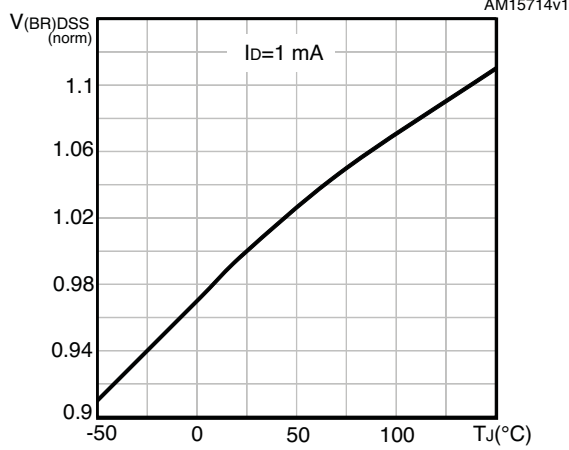
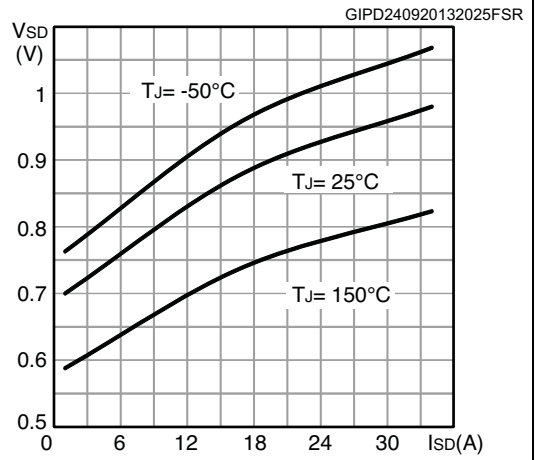
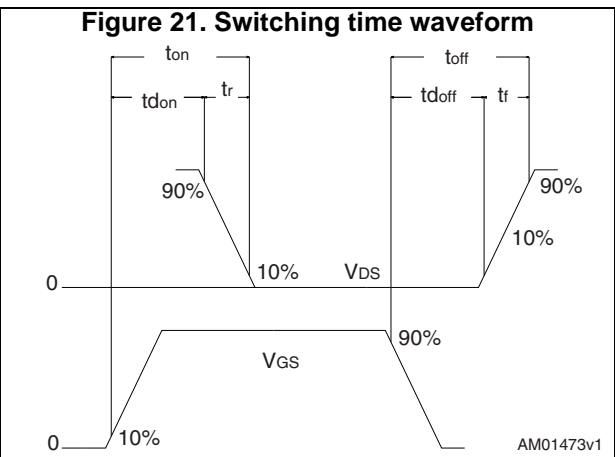
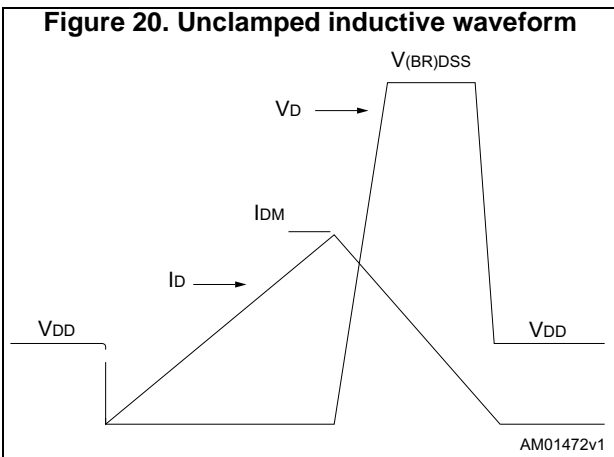
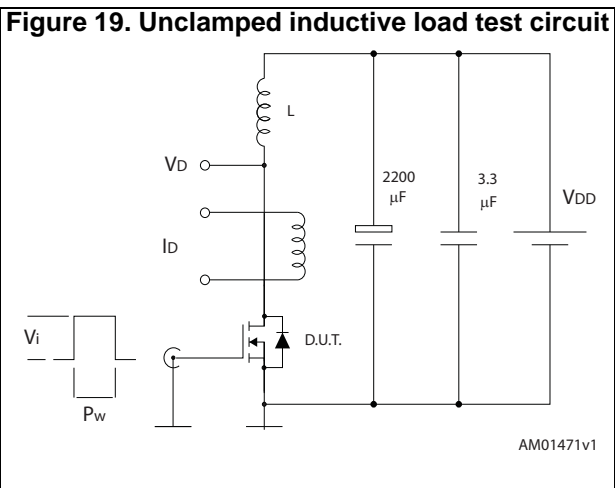
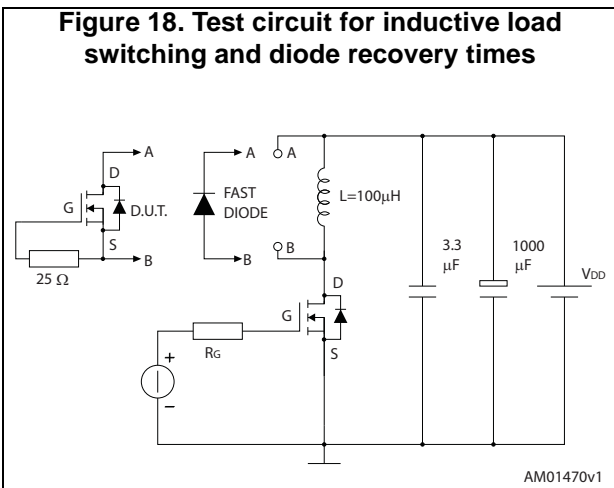
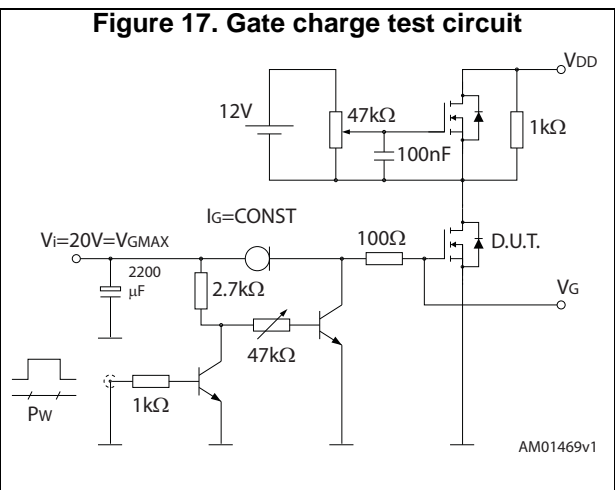
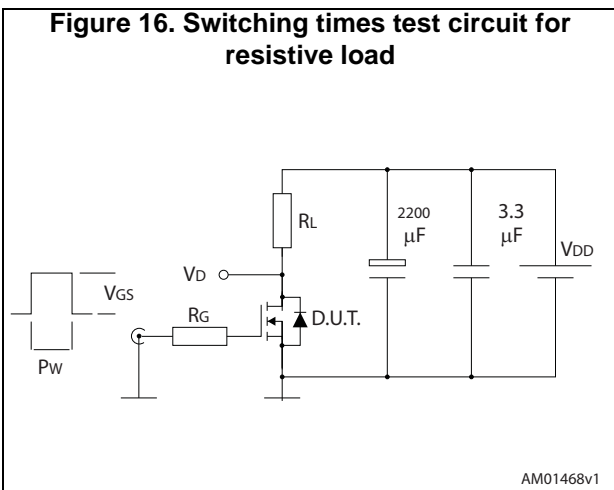


Figure 15. Source-drain diode forward vs temperature



3 Test circuits

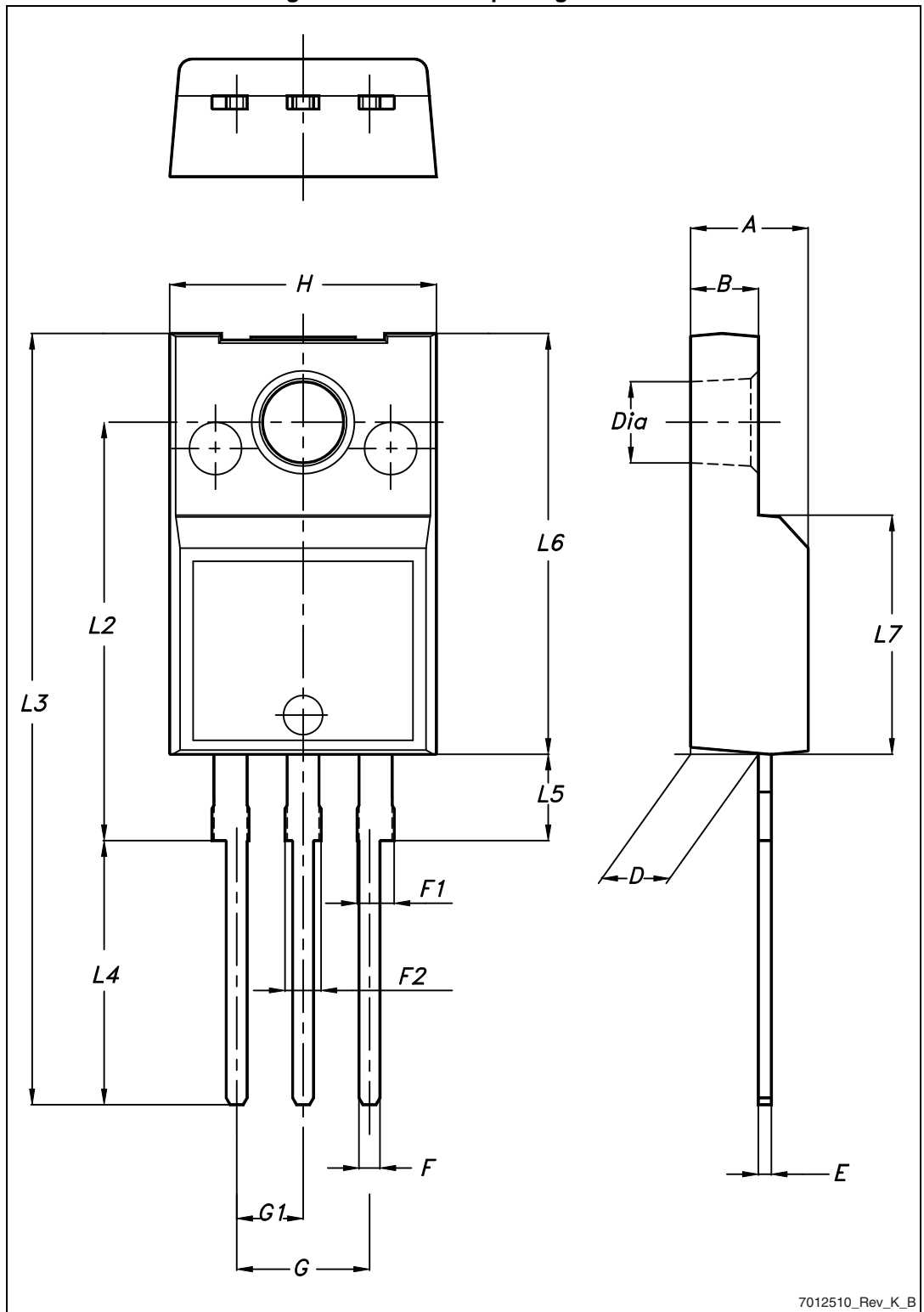


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-220FP, package outline

Figure 22. TO-220FP package outline



7012510_Rev_K_B

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.2 I²PAKFP (TO-281) package information

Figure 23. I²PAK(TO-281) package outline

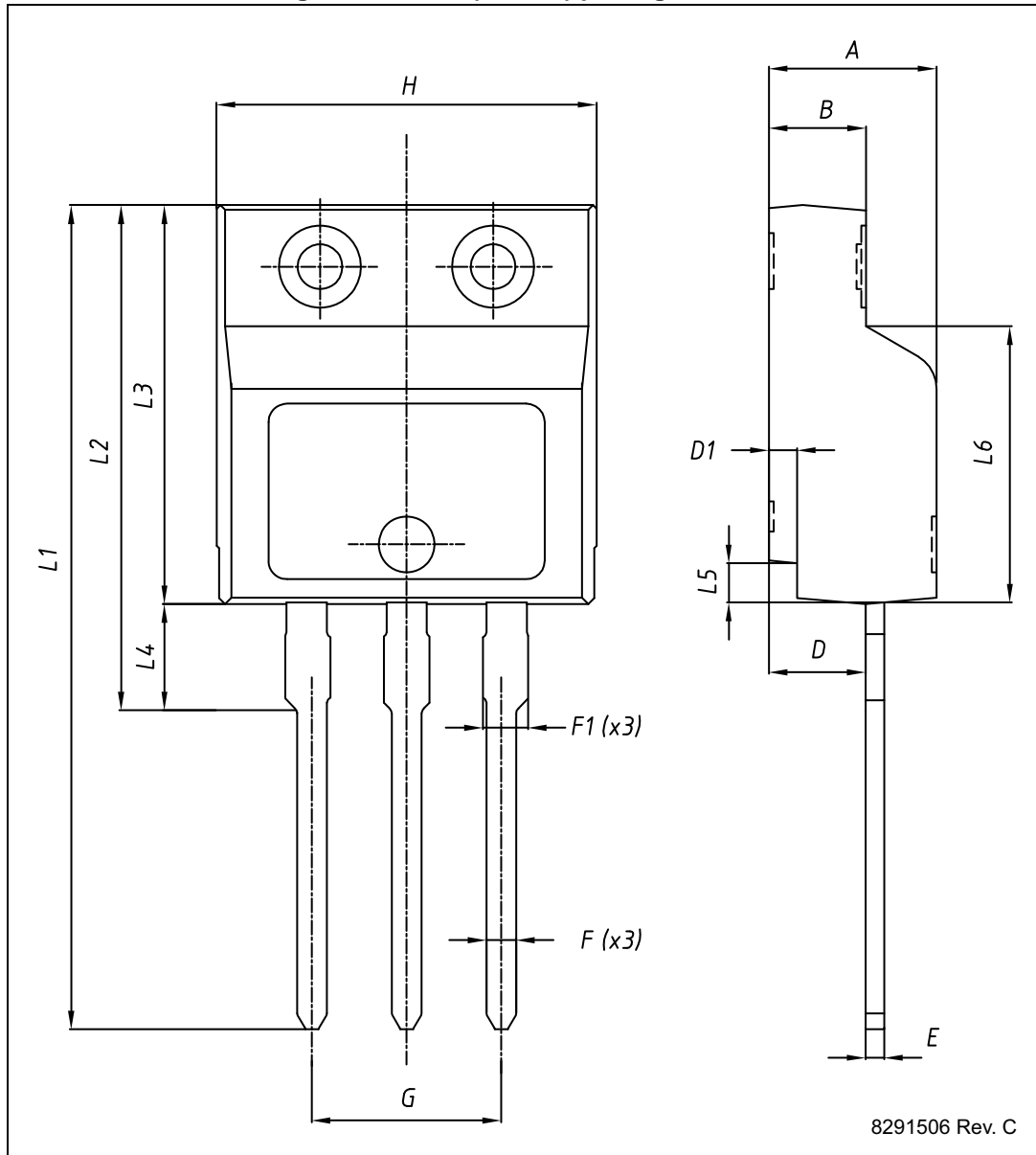


Table 10. I²PAKFP (TO-281) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

4.3 TO-3PF, package information

Figure 24. TO-3PF package outline

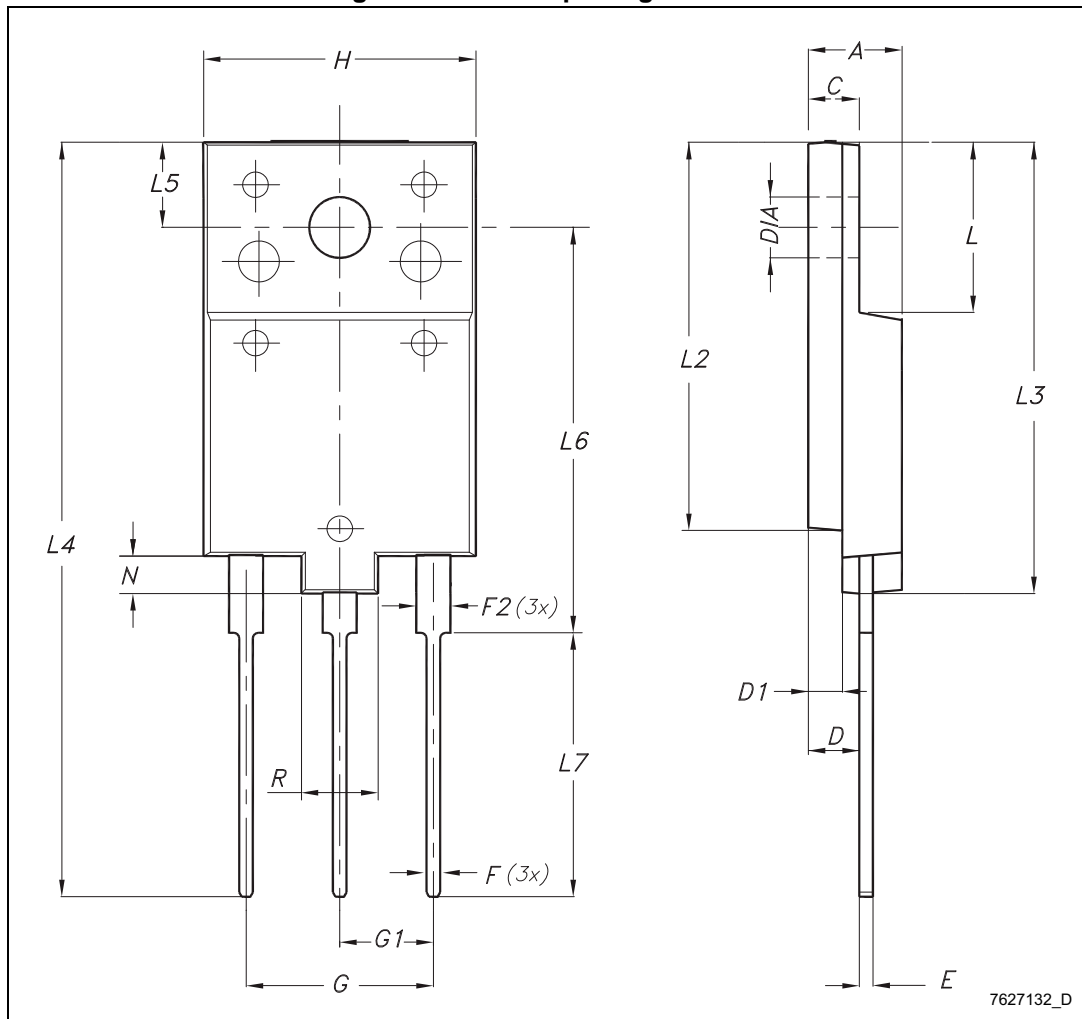


Table 11. TO-3PF package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
15-May-2014	1	First release. Part numbers STF40N60M2 and STFI40N60M2 previously included in datasheet DocID024932.
28-Sep-2016	2	Updated title in cover page. Updated Table 2: Absolute maximum ratings , Table 5: On /off states , Table 6: Dynamic and Table 8: Source drain diode . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved