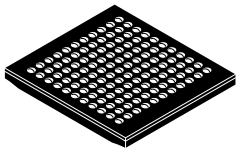
AR0231AT

Advance Information

AR0231AT 1/2.7-inch 2.3 Mp Digital Image Sensor

ON Semiconductor®

www.onsemi.com



IBGA121 10x11
CASE 503BG

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Description

The AR0231AT from ON Semiconductor is a 1/2.7−inch CMOS digital image sensor with a 1928(H) × 1208 (V) active−pixel array. It captures images in either linear, high dynamic range, or LFM modes, with a rolling−shutter readout. The LFM mode eliminates high frequency LED flicker in the image allowing Traffic Sign Reading (TSR) algorithms to operate in all lighting conditions. It includes sophisticated camera functions such as in−pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance, with sensor fault detection features that can enable ASIL B compliance for the camera system. It is programmable through a simple two−wire serial interface. The AR0231AT produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including automotive ADAS, automotive scene viewing, and 1080p HDR video.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Typical Value
Optical Format	1/2.7−inch (6.82 mm)
Maximum Resolution	1928 × 1208 (2.3 Mp)
Shutter Type	Electronic Rolling Shutter (ERS)
Pixel Size	3 μm
Pixel Output Interfaces	Up to 4−lane HiSPi with SLVS and HiVCM MIPI CSI−2 14−bit parallel
Output Formats	12−bit Uncompressed Linear 20−bit Uncompressed HDR 10−bit Companded Linear 16−bit, 14−bit, or 12−bit Companded HDR
Control Interface	2−wire, Serial Control 100 kHz/1 MHz
Input Clock Range	6−50 MHz in PLL Mode 6−88 MHz Max in PLL−bypass Mode
Maximum Frame Rate	Up to 40 fps at 1928 × 1208 / 3−exposure Up to 60 fps at 1928 × 1208 / 2−exposures and Linear
Output Pixel Clock Maximum	88 MHz
Responsivity	34 ke−/lux−sec
SNR_{MAX}	42.8 dB
Max Dynamic Range	> 120 dB
Operating Temp. Range	–40°C to 125°C Junction
Supply Voltage	I/O 1.8 V or 2.8 V Digital 1.2 V Analog 2.8 V HiSPi 0.4 V or 1.8 V
Power Consumption	< 350 mW Typical (1928 × 1208, 30 fps)
Packaging Options	11 × 10 iBGA Bare Die

Features

- Key Technologies:
  - Automotive Grade Backside Illuminated Pixel
  - LED Flicker Mitigation Mode
  - Sensor Fault Detection for ASIL−B Compliance
  - Up to 4−exposure HDR at 1928 × 1208 and 30 fps or 3−exposure HDR at 1928 × 1208 and 40 fps
- Latest 3.0 μm Back Side Illuminated (BSI) Pixel with ON Semiconductor DR−Pix™ Technology
- Data Interfaces: up to 4−lane MIPI CSI−2, Parallel, or up to 4−lane High Speed Pixel Interface (HiSPi) Serial Interface (SLVS and HiVCM)
- Advanced HDR with Flexible Exposure Ratio Control

Features (Continued)

- LED Flicker Mitigation (LFM) Mode
- Selectable Automatic or User Controlled Black Level Control
- Frame to Frame Switching among up to 4 Contexts to Enable Multi−function Systems
- Spread−spectrum Input Clock Support
- Multi−Camera Synchronization Support
- Multiple CFA Options

Applications

- Automotive ADAS
- 1080p30 Video Applications
- High Dynamic Range Imaging
- Mirror Replacement
- ADAS + Viewing Fusion

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Description
AR0231AT7C00XUEA0−DRBR−E	RGB, iBGA, Dry Pack without protective film
AR0231AT7C00XUEA0−DPBR−E	RGB, iBGA, Dry Pack
AR0231AT7R00XUEA0−DRBR−E	RCCC, iBGA, Dry Pack without protective film
AR0231AT7R00XUEA0−DPBR−E	RCCC, iBGA, Dry Pack
AR0231AT7B00XUEA0−DRBR−E	RCCB, iBGA, Dry Pack without protective film
AR0231AT7B00XUEA0−DPBR−E	RCCB, iBGA, Dry Pack
AR0231AT7C00XUD20−E	RGB, Bare Die
AR0231AT7R00XUD20−E	RCCC, Bare Die
AR0231AT7B00XUD20−E	RCCB, Bare Die
AR0231AT7C00XUEAH3−GEVB	RGB, Headboard
AR0231AT7R00XUEAH3−GEVB	RCCC, Headboard
AR0231AT7B00XUEAH3−GEVB	RCCB, Headboard
AR0231AT7C00XUEAD3−GEVK	RGB, Demo Kit
AR0231AT7R00XUEAD3−GEVK	RCCC, Demo Kit
AR0231AT7B00XUEAD3−GEVK	RCCB, Demo Kit

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

GENERAL DESCRIPTION

The AR0231AT from ON Semiconductor can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1208p−resolution image at 40 frames per second (fps) in 3−exposure HDR mode and 30 fps in 4−exposure HDR mode through the serial output ports. In linear mode, it outputs 12−bit or 14−bit uncompressed, or 10−bit compressed raw data, using either the parallel or serial output ports. In high dynamic range (HDR) mode, it outputs 12, 14−, or 16−bit compressed data using parallel output, or 12−, 14−, or 16−bit compressed or 20−bit linearized data using the serial port (HiSPi or MIPI). The device may be operated in video (master) mode or in single frame trigger mode. The LFM mode is used to minimize the impact of LED flicker for applications where there is dynamic LED lighting, such as TSR, and is output in linear mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The AR0231AT has additional ASIL features, including but not limited to: two on−board independent temperature sensor, startup tests, memory BIST, analog and digital CRC, and test patterns. Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

The sensor is designed to operate in a wide temperature range (−40°C to + 125°C).

FUNCTIONAL OVERVIEW

The AR0231AT is a 1/2.7 inch progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz. The PLL can also be bypassed in parallel mode, which allows for the input clock to run between 6 and 88 MHz. The maximum output pixel rate is 750 Mb/s in serial modes, and 88 Mp/s in parallel modes, corresponding to a clock rate of 88 MHz. Figure 1 shows a block diagram of the sensor.

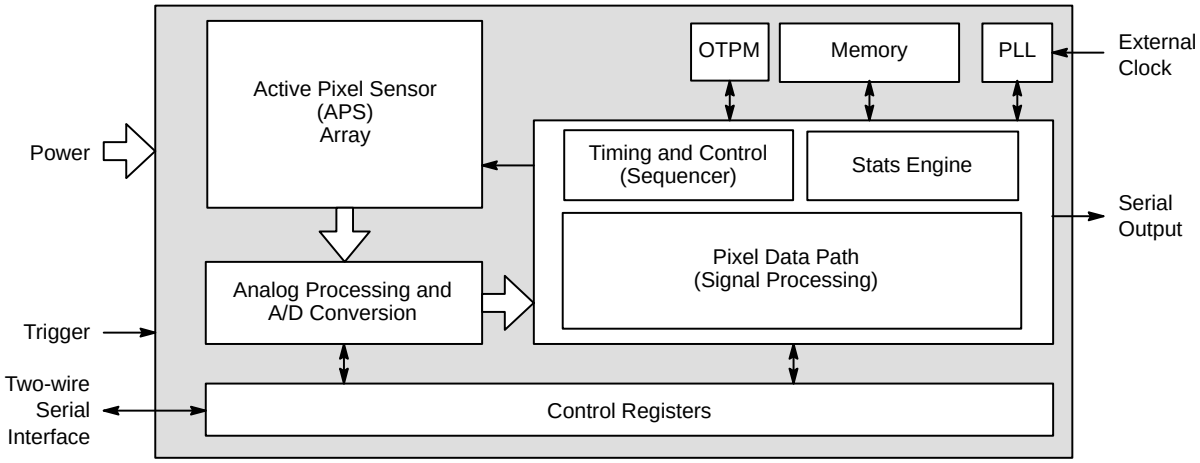
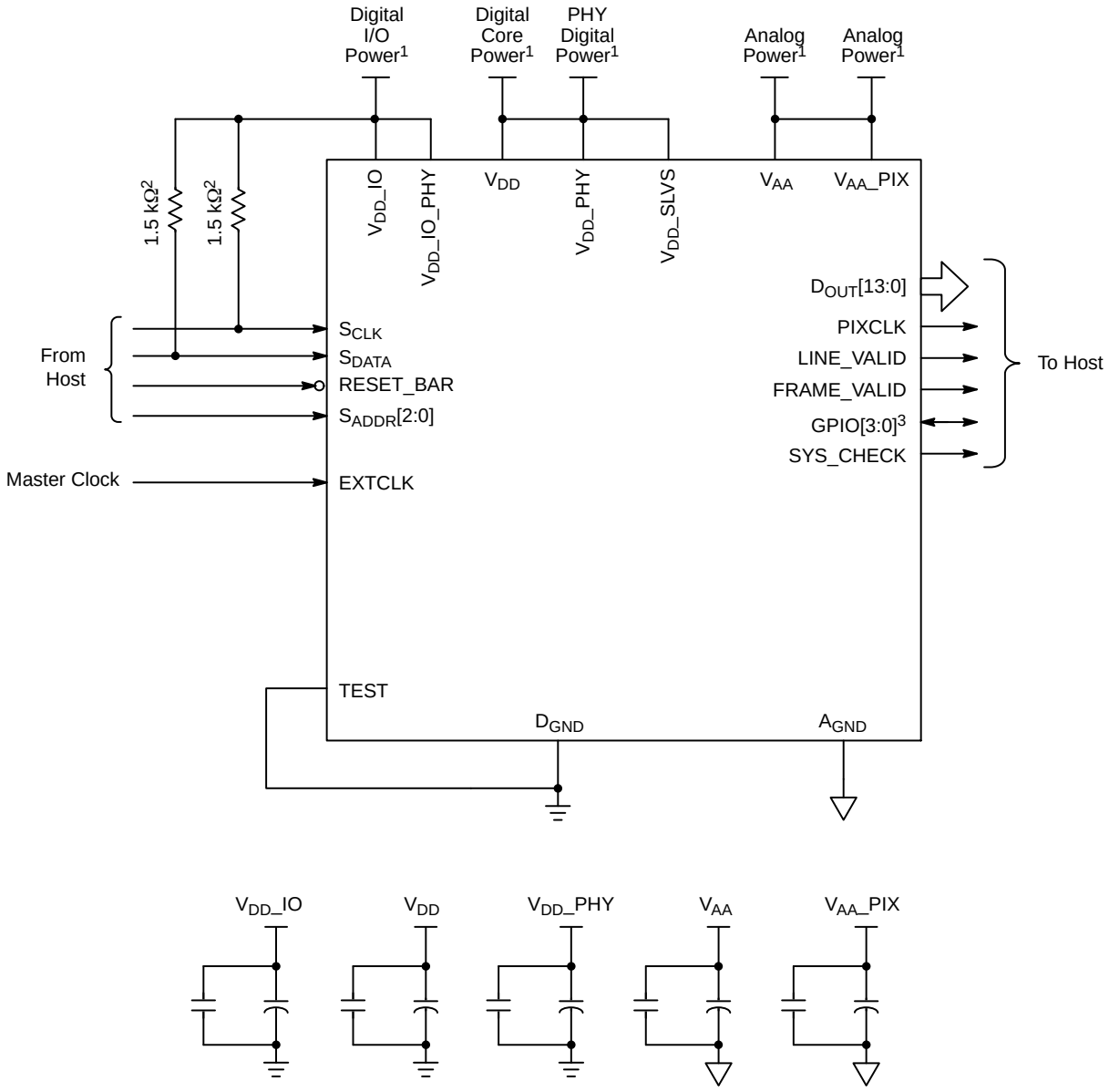


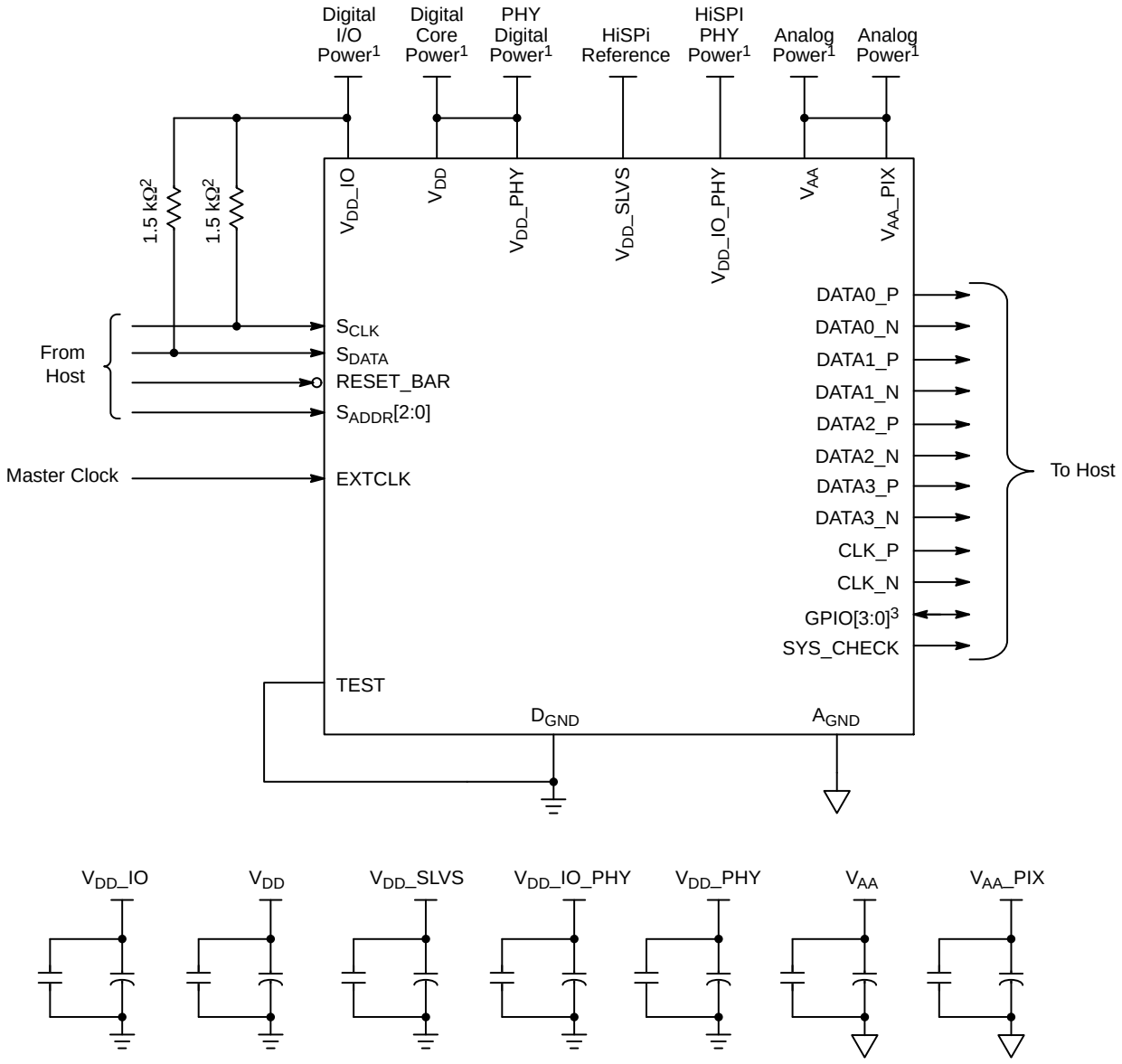
Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 2.3 Mp BSI Active−Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog−to−digital converter (ADC). The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined on−chip to produce a single image at 20−bit per pixel value. A compressing mode is further offered to allow this 20−bit pixel value to be transmitted to the host system as a 12− or 14− or 16−bit value with close to zero loss in image quality.



Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to D_{GND} if not used.
4. The serial interface output pads can be left unconnected when the parallel output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0231AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.

Figure 2. Typical Configuration, Parallel



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1. All power supplies must be adequately decoupled.
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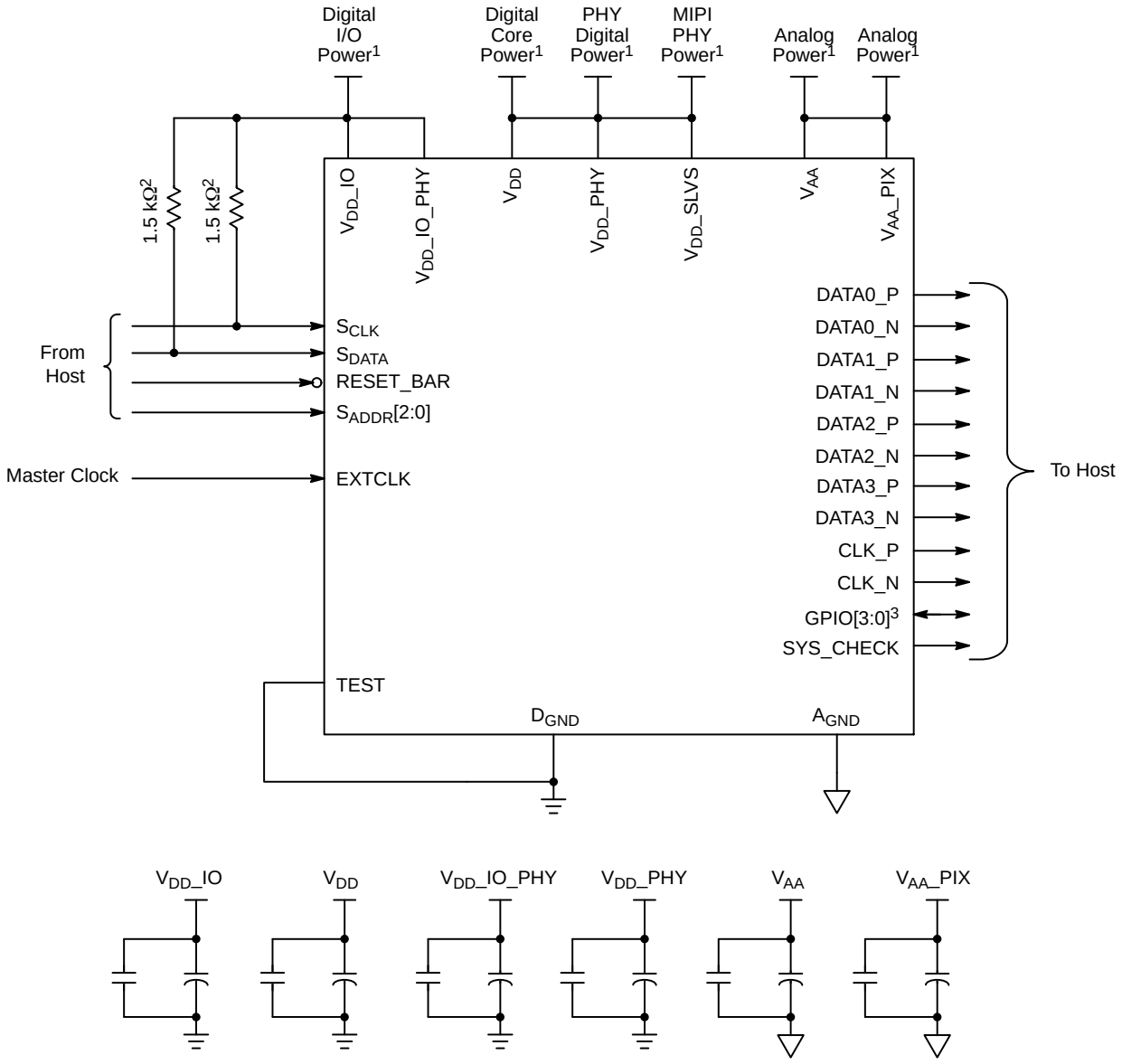
4. The parallel interface output pads can be left unconnected when the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0231AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.
8. If V_{DD}_IO is 1.8 V, then V_{DD}_IO_PHY cannot equal 2.8 V.

Figure 3. Typical Configuration, 4−lane HiSPi



Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to D_{GND} if not used.
4. The parallel interface output pads can be left unconnected when the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0231AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match V_{DD}_IO voltage to minimize any leakage currents.

Figure 4. Typical Configuration, 4−lane MIPI

PIXEL DATA FORMAT

Pixel Array Structure

While the sensor's format is 1928×1208, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for monochrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

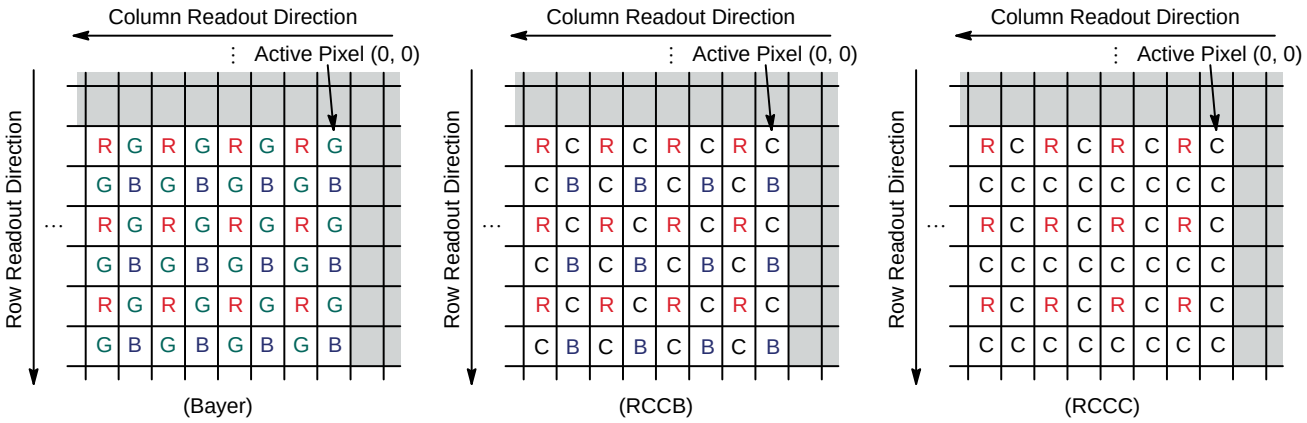


Figure 5. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 5). This reflects the actual layout of the array on the die. Also, the first first readable pixel location of the sensor in default condition is that of physical pixel address (256, 2). This first readable pixel location corresponds to the register X_ADDR_START_ (R0x3004) = 0x0000 and the register Y_ADDR_START_ (R0x3002) = 0x0000.

The optical center of the readable active pixels can be found between X_ADDR 963 and 964, and between Y_ADDR 603 and 604.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 6.

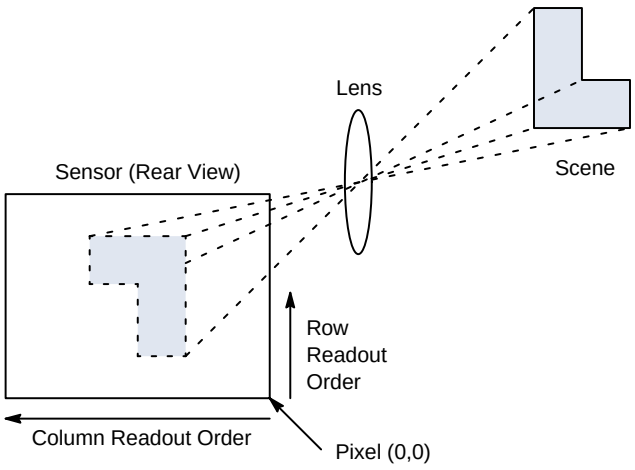


Figure 6. Imaging a Scene

OPERATING MODES AND FEATURES

For a complete description, recommendations, and usage guidelines for product features, refer to the AR0231AT Developer Guide.

3.0 μm Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0 μm) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene. This gain can be switched manually or automatically by an external auto exposure control module.

Dual conversion gain can also be controlled independently for each exposure in HDR mode, allowing a mixture of high conversion gain (HCG) and low conversion gain (LCG) across multiple exposures.

Resolution

The active array supports a maximum of 1928 × 1208 pixels to support 1080p resolution. Utilizing a 3.0 μm pixel will result in an optical format of 1/2.7−inch (approximately 6.82 mm diagonal).

Frame Rate

At full resolution, the AR0231AT is capable of running up to 30 fps in parallel mode and 40 fps in MIPI or HiSPi modes, depending on the number of exposures. The AR0231AT has a maximum frame rate of 60 fps at full resolution in 2−exposure HDR and linear modes.

High Dynamic Range

The AR0231AT can operate in an HDR mode to acquire video data using ON Semiconductor's multi−exposure technology. This allows the sensor to handle > 120 dB of intrascene dynamic range. The sensor also features a linear or standard dynamic range (SDR) mode where a single image is captured. In HDR mode, the sensor sequentially captures up to four exposures by maintaining separate read and reset pointers that are interleaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for all the exposure values to be present. As soon as all exposure values are available, they are combined to create a linearized 20−bit value for each pixel's response. This 20−bit value may be output directly or optionally companded to 16, 14 or 12−bits before output.

The exposure ratios may be set to 4x, 8x, 16x, or 32x, or can be individually controlled per exposure to allow a wide range of flexible exposure ratios. The individual exposure ratio control for T1, T2, T3, and T4 is limited by the number of line buffers allocated to each exposure.

Options to output each individual exposures only, or pixel interleaved data are also available. Individual exposures may be read out in a line interleaved mode as described in the Line Interleaved Mode section.

Motion Compensation and Linearization

In typical multi−exposure HDR systems, motion artifacts can be created when objects move during the integration time of the exposures used to construct the image. When this happens, edge artifacts can potentially be visible and might look like a tearing or ghosting effect. To correct for this issue, the AR0231AT incorporates the digital lateral overflow (DLO) algorithm as implemented in the AR0132, but with the addition of individual color knee points, as well as an additional knee point for the fourth exposure.

LED Flicker Mitigation (LFM)

LED sign flicker causes traffic signs to be incorrectly read in bright daylight conditions as the LEDs may be illuminated when the sensor is not integrating. The AR0231AT includes a new mode, LFM, for reading these signs. In LFM mode, pixels are floating−diffusion (FD) color merged in the vertical direction, and the effective sensitivity of the pixel pairs can be controlled and reduced, enabling exposure times to be extended. On AR0231AT variants with color CFAs, color will be maintained in the sensor output to aid in sign discrimination. HDR output is not available during LFM operation. LFM mode is intended for machine vision applications and should not be used for viewing. A typical use case would be to capture 3 frames of HDR data, context switch to LFM for 1 frame, and then switch back HDR for video captured at 40 fps.

Multi−camera Synchronization

AR0231AT supports multi−camera synchronization Slave modes. The Slave modes support synchronization of multiple cameras within 8 pixel clocks from the beginning of FRAME_VALID/LINE_VALID from sensors without reducing the maximum frame rate. This feature saves the line memory buffer at the host system to combine a multiple of video input streams from the sensors.

Slave Mode

The slave mode feature of the AR0231AT supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which only a subset of registers is available for switching. The AR0231AT supports a highly configurable context switching RAM of size 256 × 16. Within this Context Memory, changes to registers within the chip may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B coarse_integration_time registers in frame n+1 and all other context B registers at the beginning of reading frame n+2. The sensor will show the same behavior when changing from context B to context A. The following registers are context switchable:

Table 3. LIST OF CONFIGURABLE REGISTERS FOR CONTEXT A AND CONTEXT B

Context A Register Description	Context B Register Description
coarse_integration_time	coarse_integration_time_cb
line_length_pck	line_length_pck_cb
frame_length_lines	frame_length_lines_cb
row_bin	row_bin_cb
col_bin	col_bin_cb
fine_gain	fine_gain_cb
coarse_gain	coarse_gain_cb
x_addr_start	x_addr_start_cb
y_addr_start	y_addr_start_cb
x_addr_end	x_addr_end_cb
y_addr_end	y_addr_end_cb
y_odd_inc	y_odd_inc_cb
x_odd_inc	x_odd_inc_cb
green1_gain	green1_gain_cb
blue_gain	blue_gain_cb
red_gain	red_gain_cb
green2_gain	green2_gain_cb
global_gain	global_gain_cb
operation_mode_ctrl	operation_mode_ctrl_cb
bypass_pix_comb	bypass_pix_comb_cb

Embedded Data and Statistics

The AR0231AT has the capability to output image data and statistics within the frame timing. There are two types of information embedded within the frame readout.

Embedded data can be enabled on two rows before the active image pixels are displayed, and shows the current settings for the part.

Embedded statistics can be enabled on the two rows after the active image pixels are displayed, and include frame identifiers and histogram information for that image. This can be used by off−chip auto−exposure blocks to make decisions about exposure adjustment.

Histograms for up to three independent regions of interest (ROIs) can be tracked per frame, with programmable registers determining their size and location. Two compression methods are available for the histogram data, with one being a new logarithmic compression scheme that enables more detailed data for dark portions of the image. Note that histogram information can be output for only one pixel plane at a time.

In addition to histograms, the output image frame can be split into a virtual grid of up to 16 ROIs that can each provide the average pixel value for that region. The grid for ROIs is defined by four offset pointers for each axis (X and Y), as shown in Figure 7. Each of these averages can be included with the statistics embedded in the output image, allowing a simple exposure metric for each region to be generated.

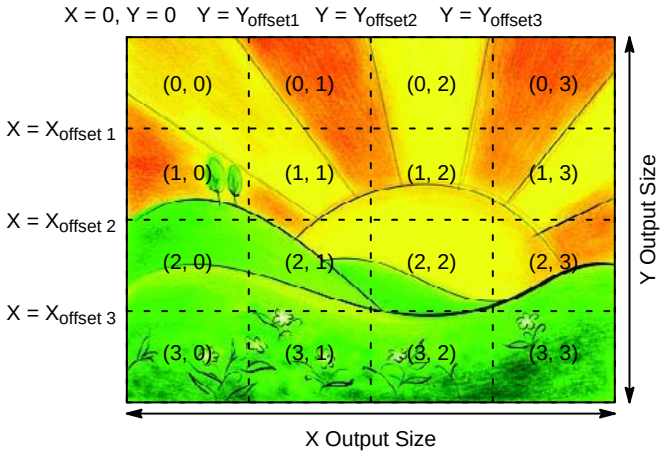


Figure 7. Grid−ROI, Configuration 1; x_grid_status=0x3; y_grid_status=0x3

Black Level Control/Correction

Black level correction can optionally be automatically controlled by the AR0231AT; the default setting is for automatic black level calibration to be enabled. The automatic black level correction measures the average value of pixels from a set of optically black pixel rows in the image sensor. The pixels are averaged as if they were light sensitive and passed through the appropriate gain. This line average is then digitally low−pass filtered over many frames to remove temporal noise and random instabilities associated with this measurement. The optically black lines may be read out, bypassing the datapath, for off−chip analysis. The automatic black level correction can be disabled and the black level set manually via register settings. Manual black level settings are frame synchronized to the next start of frame.

Row and Column Correction

Row and column noise correction is applied automatically by the image sensor on a frame by frame basis. Re−triggering of correction circuits due to settings or temperature changes are not necessary. The digital gain can be applied before HDR linearization for white balancing, and after HDR linearization for increasing scene brightness.

Defective Pixel Tracking/Correction

Defective Pixel Correction (DPC) is intended to compensate or tag defective pixels by replacing their value with a value based on the surrounding pixels, or tagging them by assigning them a ‘0’ value. The defect pixel correction feature supports up to 200 defects. The locations of defective pixels are stored in a table on chip during the manufacturing process; this table is accessible through the two−wire serial interface. There is no provision for later augmenting the defect table entries. The DPC algorithm is one−dimensional, calculating the resulting averaged pixel value based on nearby pixels within a row. The algorithm distinguishes between color and monochrome parts; for color parts, the algorithm uses nearest neighbor in the same color plane. The defect pixel correction algorithm may be disabled. (Note that the outgoing defect specification for the AR0231AT assumes the defect correction is disabled). The defect pixels identified during manufacture can be read from on−chip ROM via the 2−wire control interface.

Analog/Digital Gains

A programmable analog gain of 0.125x to 8x applied simultaneously to all color channels will be featured along with a digital gain of 1x to 16x that may be configured on a per color channel basis. Future releases will have an option to separate the digital gain for use as an AWB function and as a global gain.

Skipping/Binning Modes

The AR0231AT supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor will sample the combined two adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as two rows within the same color plane. Pixel skipping can be configured up to two in both the x−direction and y−direction. Skipping pixels in the x−direction will not reduce the row time. Skipping pixels in the y direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing. The AR0231AT supports row wise vertical binning. Row wise vertical summing is not supported.

CFA Type Identification

CFA type (e.g. RGB, mono, etc.) may be determined by reading an identification register via the 2−wire control interface.

ASIL/ISO26262 Support Features

The AR0231AT incorporates many features to assist ASIL−B system compliance to be achieved by a system that integrates it. Please refer to the AR0231AT Safety Manual for more information.

SYSTEM INTERFACES

This section describes the AR0231AT interfaces. Note that all output port options may not be available on all packaging options.

HiSPi Pixel Output Port

The AR0231AT provides a 4−lane HiSPi pixel output port with support for SLVS and HiVCM modes. Supported configurations are described in Table 4. Additional information is provided in the ON Semiconductor HiSPi Protocol and Physical Layer documents.

Table 4. HISPI PROTOCOL SUPPORT

Lanes	Width	Data Type	Protocols	Max. Mbps/Lane	Notes
1, 2, or 4	20−bit	Bayer/RAW	SP−packetized SP−streaming Streaming−S	750 Mbps	HDR Output Mode (Uncompressed)
1, 2, or 4	16−bit	Bayer/RAW	SP−packetized SP−streaming Streaming−S	750 Mbps	HDR Output Mode (Compressed)
1, 2, or 4	14−bit	Bayer/RAW	SP−packetized SP−streaming Streaming−S	750 Mbps	HDR Output Mode (Compressed)
1, 2, or 4	12−bit	Bayer/RAW	SP−packetized SP−streaming Streaming−S	750 Mbps	SDR (Linear) Mode

MIPI CSI−2 Pixel Output Port

The AR0231AT provides a 4−lane MIPI CSI−2 pixel output port. The data protocol support is per Table 5. Please contact ON Semiconductor for additional information.

Table 5. MIPI PROTOCOL SUPPORT

Lanes	Width	Data Type	Protocols	Max. Mbps/Lane	Notes
1, 2, or 4	20−bit	Bayer/RAW	SP−packetized SP−streaming	520 Mbps	HDR Output Mode (Uncompressed)
1, 2, or 4	16−bit	Bayer/RAW	SP−packetized SP−streaming	520 Mbps	HDR Output Mode (Compressed)
1, 2, or 4	14−bit	Bayer/RAW	SP−packetized SP−streaming	520 Mbps	HDR Output Mode (Compressed)
1, 2, or 4	12−bit	Bayer/RAW	SP−packetized SP−streaming	520 Mbps	SDR (Linear) Mode

Parallel Pixel Output Port

The AR0231AT provides a 14−bit data pixel output port with frame and line valid signals. HDR data is companded to 14−bit or 12−bit, and 12−bit SDR (non−HDR) data may be output via this port.

Note that the parallel port cannot be used to output combinations of individual T1/T2/T3/T4 exposures on a per frame basis.

Line Interleaved Output

The AR0231AT will have the capability to output the T1, T2, T3, and T4 exposures separately, in a line interleaved format. The purpose of this is to enable off chip HDR linear combination and processing.

Embedded data and statistics are also supported in line interleaved mode. See the AR0231AT Developer Guide for more information.

Two−Wire Sensor Control Interface

The two−wire serial interface bus enables read/write access to control and status registers within the AR0231AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (S_{CLK}) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (S_{DATA}). S_{DATA} is pulled up to V_{DD}_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive S_{DATA} LOW−the interface protocol determines which device is allowed to drive S_{DATA} at any given time. The protocols described in the two−wire serial interface specification allow the slave device to drive S_{CLK} LOW; the AR0231AT uses S_{CLK} as an input only and therefore never drives it LOW.

ELECTRICAL SPECIFICATIONS

Table 6. ELECTRICAL SPECIFICATIONS

Symbol	Definition	Min	Nom	Max	Unit
V_{DD}	Core Digital Voltage	1.14	1.2	1.26	V
V_{DD}_IO	I/O Digital Voltage	1.7/2.52	1.8/2.8	1.9/3.0	V
V_{AA}	Analog Voltage	2.6	2.8	3.0	V
V_{AA}_PIX	Pixel Supply Voltage	2.6	2.8	3.0	V
V_{DD}_PHY	PHY Supply Voltage	1.14	1.2	2.16	V
V_{DD}_IO_PHY	Serial PHY Supply Voltage	1.7 /2.52	1.8/2.8	1.9/3.0	V
V_{DD}_SLVS	HiSPi Supply Voltage (SLVS)	0.3	0.4	0.6	V
V_{DD}_SLVS	HiSPi Supply Voltage (HiVCM)	1.14	1.2	2.16	V

8. V_{AA}_PIX must always be equal to V_{AA}.

Power Up

For controlled power up, RESET_BAR pin must be asserted (low) before supplies can be sequenced up in any order (V_{DD}_IO must be brought up before V_{AA} unless all supplies are brought up at the same time). Once all supplies are valid, RESET_BAR is deasserted (high), the part will begin boot−up on EXTCLK.

Power Down

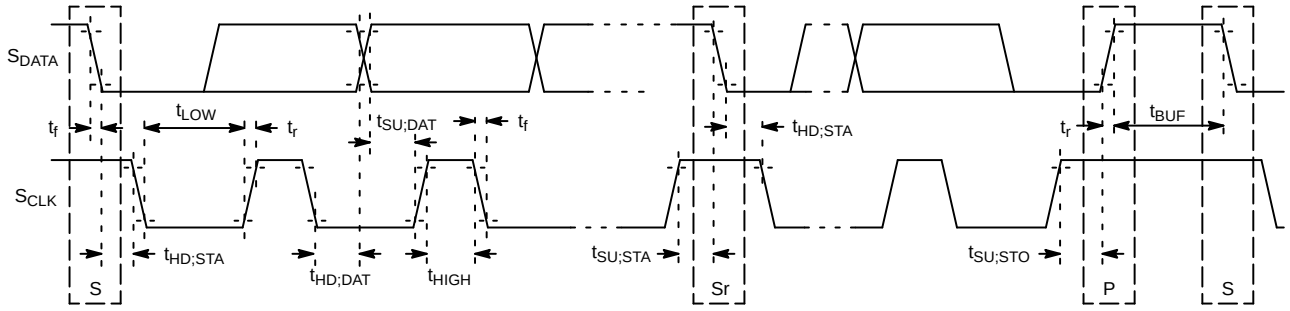
For controlled power down, streaming must be first disabled. The RESET_BAR pin must be asserted (low) before any external supplies are removed. The V_{AA} supply must be sequenced off before the V_{DD}_IO supply, unless all supplies are powered down at the same time.

Typical Power Down Sequence:

1. De−assert Streaming: Set software standby mode (mode_select = 0) register.
2. Wait till the end of the current frame (or end−of−line if so configured).
3. Configure I/O for “hold” if desired. “Hold” state requires maintaining V_{DD}_IO; however.
4. Set RESET_BAR = 0 (Hard Standby, low−leakage state).
5. Wait t_0 power−down delay.
6. Power off supplies in prescribed order. For “hold” I/O state, do not power off V_{DD}_IO supply.

Two−Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 8 and Table 7.



NOTE: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

Figure 8. Two−wire Serial Bus Timing Parameters

Table 7. TWO-WIRE SERIAL BUS CHARACTERISTICS
(f_{EXTCLK} = 27 MHz; V_{DD} = 1.8 V; V_{DD_IO} = 2.8 V; V_{AA} = 2.8 V; V_{AA_PIX} = 2.8 V; V_{DD_PLL} = 2.8 V; T_A = 25°C)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	S_{CLK} Clock Frequency	0	100	0	1000	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition. After this period, the first clock pulse is generated	4.0	−	0.6	−	μs
t_{LOW}	LOW Period of the S_{CLK} Clock	4.7	−	1.3	−	μs
t_{HIGH}	HIGH Period of the S_{CLK} Clock	4.0	−	0.6	−	μs
$t_{SU;STA}$	Set−up Time for a Repeated START Condition	4.7	−	0.6	−	μs
$t_{HD;DAT}$	Data Hold Time	0 (Note 12)	3.45 (Note 13)	0 (Note 14)	0.9 (Note 13)	μs
$t_{SU;DAT}$	Data Set−up Time	250	−	100 (Note 14)	−	ns
t_r	Rise Time of both S_{DATA} and S_{CLK} Signals	−	1000	20 + 0.1 Cb (Note 15)	300	ns
t_f	Fall Time of both S_{DATA} and S_{CLK} Signals	−	300	20 + 0.1 Cb (Note 15)	300	ns
$t_{SU;STO}$	Set−up Time for STOP Condition	4.0	−	0.6	−	μs
t_{BUF}	Bus Free Time between a STOP and START Condition	4.7	−	1.3	−	μs
Cb	Capacitive Load for each Bus Line	−	400	−	400	pF
C_{IN_SI}	Serial Interface Input Pin Capacitance	−	3.3	−	3.3	pF
C_{LOAD_SD}	S_{DATA} Max Load Capacitance	−	30	−	30	pF
R_{SD}	S_{DATA} Pull−up Resistor	1.5	4.7	1.5	4.7	kΩ

9. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
10. Two−wire control is I²C−compatible.
11. All values referred to V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD} levels. Sensor EXCLK = 27 MHz.
12. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
13. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
14. A Fast−mode I²C−bus device can be used in a Standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I²C−bus specification) before the S_{CLK} line is released.
15. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0231AT launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures D_{OUT}[13:0], FV, and LV using the rising edge of PIXCLK.

See Figure 9 below and Table 8 for I/O timing (AC) characteristics.

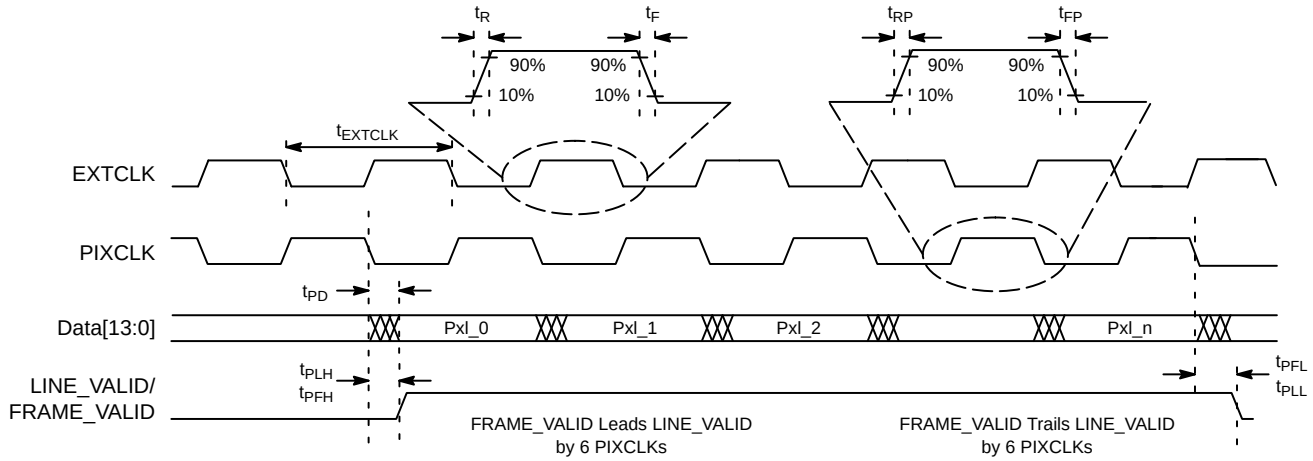


Figure 9. I/O Timing Diagram

Table 8. I/O TIMING CHARACTERISTICS (Note 16)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1s}$	Input Clock Frequency		6 (Note 17)	–	50	MHz
$t_{EXTCLK1}$	Input Clock Period		15.6	–	166	ns
t_R	Input Clock Rise Time		–	3	–	ns
t_F	Input Clock Fall Time		–	3	–	ns
t_{RP}	Pixclk Rise Time		–	4	–	ns
t_{FP}	Pixclk Fall Time		–	4	–	ns
	Clock Duty Cycle		40	50	60	%
$t_{PIX\ JITTER}$	Jitter on PIXCLK		–	1		ns
t_{CP}	EXTCLK to PIXCLK Propagation Delay	Nominal Voltages, PLL Disabled	–	32.4	–	ns
f_{PIXCLK}	PIXCLK Frequency	Default, Nominal Voltages	6		88	MHz
t_{PD}	PIXCLK to Data Valid	Default, Nominal Voltages	–	2.3	–	ns
t_{PFH}	PIXCLK to FV HIGH	Default, Nominal Voltages	–	5.7	–	ns
t_{PLH}	PIXCLK to LV HIGH	Default, Nominal Voltages	–	5.5	–	ns
t_{PFL}	PIXCLK to FV LOW	Default, Nominal Voltages	–	4.3	–	ns
t_{PLL}	PIXCLK to LV LOW	Default, Nominal Voltages	–	4.6	–	ns
C_{LOAD}	Output Load Capacitance		–	< 10	–	pF
C_{IN}	Input Pin Capacitance		–	2.5	–	pF

16. I/O timing characteristics are measured under the following conditions:
    a. Temperature is 25°C ambient
    b. 10 pF load
    c. 1.8 V I/O supply voltage
17. When using a 1 MHz two−wire interface clock, the minimum clock frequency is 16 MHz.

Table 9. PARALLEL 12−BIT 3−EXPOSURE HDR, T_{INT}

(All images taken in mid−level ambient lighting conditions, 2x gain, 1 ms integration time, 25°C)

Current Type	Condition	Symbol	Voltage	Min	Typ	Max
Analog Operating Current	Streaming Full Res	I_{AA}	2.8	42	62.21	85
Digital Operating Current	Streaming Full Res	I_{DD}	1.2	108	148.33	195
I/O Supply Current	Streaming Full Res	$I_{DD_IO}/I_{DD_IO_PHY}$	1.8	5	15.84	30
PHY Supply Current	Streaming Full Res	I_{DD_PHY}	1.2	1.5	3.69	9
Pixel Supply Current	Streaming Full Res	I_{AA_PIX}	2.8	7	10.17	16
SLVS Supply Current	Streaming Full Res	I_{DD_SLVS}	1.2	−0.5	−0.01	0.5

18. Operating currents measured under the following conditions:
    a. V_{AA} and V_{AA_PIX} are tied together
    b. $V_{DD_IO_PHY}$ and V_{DD_IO} are tied together
    c. PLL enabled and PIXLCK set to 88 MHz
    d. 3−exposure 12−bit Parallel mode at 33 fps
    e. T_J = 25°C

Table 10. HISPI HIVCM 16−BIT 3−EXPOSURE HDR

Current Type	Condition	Symbol	Voltage	Min	Typ	Max
Analog Operating Current	Streaming Full Res	I_{AA}	2.8	50	73.1	90
Digital Operating Current	Streaming Full Res	I_{DD}	1.2	100	143.2	200
I/O Supply Current	Streaming Full Res	I_{DD}_IO/I_{DD}_IO_PHY	1.8	25	38.56	55
PHY Supply Current	Streaming Full Res	I_{DD}_PHY	1.2	6	13.27	20
Pixel Supply Current	Streaming Full Res	I_{AA}_PIX	2.8	6	12.9	18
SLVS Supply Current	Streaming Full Res	I_{DD}_SLVS	1.2	−0.5	0.2	1

19. Operating currents measured under the following conditions:
    a. V_{AA} and V_{AA}_PIX are tied together
    b. V_{DD}_IO_PHY and V_{DD}_IO are tied together
    c. PLL enabled and PIXLCK set to 88 MHz
    c. 4−lane 3−exposure 16−bit HiSPi HiVCM mode at 40 fps
    e. T_J = 25°C

Table 11. HISPI SLVS 16−BIT 3−EXPOSURE HDR, 40 FPS, 1 MS T_{INT}, 2X GAIN

Current Type	Condition	Symbol	Voltage	Min	Typ	Max
Analog Operating Current	Streaming Full Res	I_{AA}	2.8	50	73.25	90
Digital Operating Current	Streaming Full Res	I_{DD}	1.2	100	143.29	200
I/O Supply Current	Streaming Full Res	I_{DD}_IO/I_{DD}_IO_PHY	1.8	−2	−0.5	2
PHY Supply Current	Streaming Full Res	I_{DD}_PHY	1.2	6	13.08	20
Pixel Supply Current	Streaming Full Res	I_{AA}_PIX	2.8	12	12.91	18
SLVS Supply Current	Streaming Full Res	I_{DD}_SLVS	0.4	7	10.45	20

20. Operating currents measured under the following conditions:
    a. V_{AA} and V_{AA}_PIX are tied together
    b. V_{DD}_IO_PHY and V_{DD}_IO are tied together
    c. PLL enabled and PIXLCK set to 88 MHz
    c. 4−lane 3−exposure 16−bit HiSPi SLVS mode at 40 fps
    e. T_J = 25°C

Table 12. MIPI 16−BIT 3−EXPOSURE HDR

Current Type	Condition	Symbol	Voltage	Min	Typ	Max
Analog Operating Current	Streaming Full Res	I_{AA}	2.8	40	65.64	100
Digital Operating Current	Streaming Full Res	I_{DD}	1.2	100	143.9	210
I/O Supply Current	Streaming Full Res	I_{DD}_IO/I_{DD}_IO_PHY	1.8	−1	0.375	2
PHY Supply Current	Streaming Full Res	I_{DD}_PHY	1.2	5	10.61	18
Pixel Supply Current	Streaming Full Res	I_{AA}_PIX	2.8	6	12.76	18
SLVS Supply Current	Streaming Full Res	I_{DD}_SLVS	1.2	5	8.196	11

21. Operating currents measured under the following conditions:
    a. V_{AA} and V_{AA}_PIX are tied together
    b. V_{DD}_IO_PHY and V_{DD}_IO are tied together
    c. PLL enabled and PIXLCK set to 88 MHz
    c. 4−lane 3−exposure 16−bit MIPI mode at 40 fps
    e. T_J = 25°C

HiSPi Electrical Specifications

The ON Semiconductor AR0231AT sensor supports both SLVS and HiVCM HiSPi modes. Please refer to the High−Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The V_{DD}_SLVS supply in this data sheet corresponds to V_{DD}_TX in the HiSPi Physical Layer Specification. Similarly, V_{DD} is equivalent to V_{DD}_HiSPi as referenced in the specification. The DLL as implemented on AR0231AT is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

Table 13. CHANNEL SKEW

(Measurement Conditions: V_{DD}_HiSPi = 1.8 V; V_{DD}_HiSPi_TX = 0.4 V; Data Rate = 480 Mbps; DLL set to 0)

Paremeter	Symbol	Value	Unit
Data Lane Skew in Reference to Clock	$t_{CHSKEW1PHY}$	−150	ps

POWER−ON RESET AND STANDBY TIMING

Power−Up Sequence

A typical power−up sequence:

1. Set RESET_BAR low.
2. Power up supplies (except V_{PP} should be kept low).
3. Wait for current to be applied on t_0, t_1, t_2, controlled by external supply slew rate (See Figure 10).
4. When external supplies valid, set RESET_BAR high.
5. HOST config through IIC.
6. Set STREAMING bit.
7. PLL internally enables and locks.
8. AR0231 enters streaming mode.

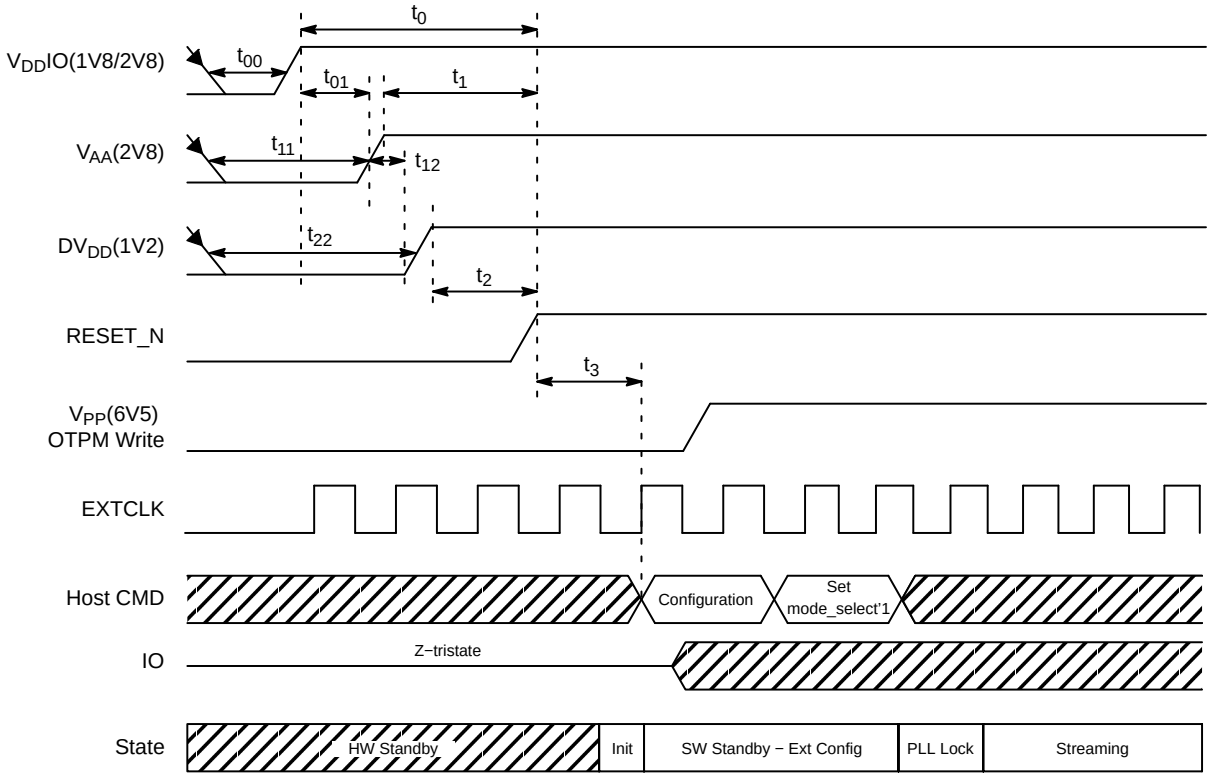


Figure 10. Initial Power−up Sequence

Table 14. POWER−UP SEQUENCE TIMING CONSTRAINTS

Constraint	Label	Min	Max	Unit
V_{DD}IO Recovery Time (1V8)	t_{00}	330	−	μS
V_{DD}IO Recovery Time (2V8)	t_{00}	500	−	μS
V_{AA} Recovery Time (2V8)	t_{11}	330	−	μS
V_{DD} Recovery Time (1V2)	t_{22}	200	−	μS
V_{DD}IO (1V8/2V8) Rising Trigger Voltage		1.11	1.46	V
V_{DD}IO (1V8/2V8) Falling Trigger Voltage		1.04	1.39	V
V_{AA} (2V8) Rising Trigger Voltage		1.81	2.35	V
V_{AA} (2V8) Falling Trigger Voltage		1.65	2.17	V
V_{DD} (1V2) Rising Trigger Voltage		−	0.91	V
V_{DD} (1V2) Falling Trigger Voltage		0.6	−	V
V_{DD}IO (1V8) Rising to RESET_N Rising	t_0	46	−	μS
V_{DD}IO (2V8) Rising to RESET_N Rising	t_0	70	−	μS
V_{DD}IO Rising to V_{AA} Rising	t_{01}	0	−	μS
V_{AA} Rising to RESET_N Rising	t_1	56	−	μS
DV_{DD} Rising to RESET_N Rising	t_2	57	−	μS
PLL Lock Time		1.0		ms

Table 15. AR0231 PIN LIST

Pin Name	iBGA Pin	Type	Description	Comments
EXTCLK	B4	Input	Master input clock. PLL input clock	Connect to clock source. Min and Max frequency depends upon output port and clocking method
RESET_BAR	C5	Input	Asynchronous active−low reset	Connect to host
S_{CLK}	H8	Input	CCI clock for access to control and status registers	Connect to host
S_{DATA}	H9	Input/Output	CCI data for reads from and writes to control and status registers	Connect to host
$S_{ADDR}0$	K9	Input	CCI interface device address select bit 0	Selects CCI address. 000b sets the address to 0x20/0x21. 001b sets the address to 0x30/0x31. Connect to V_{DD}_IO or D_{GND} accordingly
$S_{ADDR}1$	K8	Input	CCI interface device address select bit 1	
$S_{ADDR}2$	K7	Input	CCI interface device address select bit 2	
PIXCLK	F2	Output	Parallel data output pixel clock. Used to qualify the LINE_VALID, FRAME_VALID and DOUT13 to DOUT0 outputs	Connect to host/receiver or can be left floating if not used. Use D_{OUT}[11:0] for 12−bit parallel configuration
FRAME_VALID	G3	Output	Parallel data output FRAME_VALID output. Qualified by PIXCLK	
LINE_VALID	G4	Output	Parallel data output LINE_VALID output. Qualified by PIXCLK	

Table 15. AR0231 PIN LIST (continued)

Pin Name	iBGA Pin	Type	Description	Comments
$D_{OUT}13$	J2	Output	Parallel data output pixel data bit 13. Qualified by PIXCLK	Connect to host/receiver or can be left floating if not used. Use D_{OUT}[11:0] for 12−bit parallel configuration
$D_{OUT}12$	J3	Output	Parallel data output pixel data bit 12. Qualified by PIXCLK	
$D_{OUT}11$	H2	Output	Parallel data output pixel data bit 11. Qualified by PIXCLK	
$D_{OUT}10$	H3	Output	Parallel data output pixel data bit 10. Qualified by PIXCLK	
$D_{OUT}9$	G2	Output	Parallel data output pixel data bit 9. Qualified by PIXCLK	
$D_{OUT}8$	F3	Output	Parallel data output pixel data bit 8. Qualified by PIXCLK	
$D_{OUT}7$	E3	Output	Parallel data output pixel data bit 7. Qualified by PIXCLK	
$D_{OUT}6$	E2	Output	Parallel data output pixel data bit 6. Qualified by PIXCLK	
$D_{OUT}5$	D3	Output	Parallel data output pixel data bit 5. Qualified by PIXCLK	
$D_{OUT}4$	D2	Output	Parallel data output pixel data bit 4. Qualified by PIXCLK	
$D_{OUT}3$	C3	Output	Parallel data output pixel data bit 3. Qualified by PIXCLK	
$D_{OUT}2$	C4	Output	Parallel data output pixel data bit 2. Qualified by PIXCLK	
$D_{OUT}1$	B3	Output	Parallel data output pixel data bit 1. Qualified by PIXCLK	
$D_{OUT}0$	B2	Output	Parallel data output pixel data bit 0. Qualified by PIXCLK	Connect to host/receiver or can be left floating if not used. Use D_{OUT}[11:0] for 12−bit parallel configuration
CLK_P	A8	Output	Differential MIPI/HiSpi serial clock	Connect to host/receiver or can be left floating if not used. Use DATA0 for 1 lane configuration or DATA0 and DATA1 for 2 lane configuration
CLK_N	B8	Output	Differential MIPI/HiSpi serial clock	
DATA3_P	B10	Output	Differential MIPI/HiSpi serial data lane 3	
DATA3_N	A10	Output	Differential MIPI/HiSpi serial data lane 3	
DATA2_P	A9	Output	Differential MIPI/HiSpi serial data lane 2	
DATA2_N	B9	Output	Differential MIPI/HiSpi serial data lane 2	
DATA1_P	B7	Output	Differential MIPI/HiSpi serial data lane 1	
DATA1_N	A7	Output	Differential MIPI/HiSpi serial data lane 1	
DATA0_P	A6	Output	Differential MIPI/HiSpi serial data lane 0	
DATA0_N	B6	Output	Differential MIPI/HiSpi serial data lane 0	
TEST	K2	Input	Enable manufacturing test modes	Tie to D_{GND}

Table 15. AR0231 PIN LIST (continued)

Pin Name	iBGA Pin	Type	Description	Comments
ATEST1	G8	Input/Output	Analog manufacturing test access	Leave unconnected
ATEST2	G9	Input/Output	Analog manufacturing test access	
ATEST3	G10	Input/Output	Analog manufacturing test access	
ATEST4	G11	Input/Output	Analog manufacturing test access	
GPIO0	J9	Input/Output	GPIO Pin 0	GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to D_{GND} if not used
GPIO1	J8	Input/Output	GPIO Pin 1	
GPIO2	K11	Input/Output	GPIO Pin 2	
GPIO3	K10	Input/Output	GPIO Pin 3	
SYS_CHECK	J10	Output	Combined OR of error flags	Leave unconnected if not used
TEMP_FLAG	H10	Output	Temperature monitoring flag	Leave unconnected if not used
D_{GND}	E1, G1, J1, A2, K3, L3, D4, E4, F4, H4, J4, K4, B5, D5, E5, F5, G5, H5, J5, K5, D6, E6, F6, G6, H6, J6, K6, L6, D7, E7, F7, G7, H7, J7, C8, D8, E8, F8, L9, C10	Power	Digital ground	
V_{DD}	B1, F1, K1, L2, A3, A4, L5, L8, L10, B11, J11	Power	Core Digital power	
V_{DD}_PHY	C7	Power	PHY Digital power	Connect to V_{DD}
V_{DD}_IO	A1, D1, H1, L1, L4, A5, L7, A11, H11, L11	Power	Digital I/O power	
A_{GND}	C2, D9, E9, F9, F11	Power	Analog ground	
V_{AA}	C1, D10, E10, F10, E11	Power	Analog power	
V_{AA}_PIX	D11	Power	Analog pixel array power	Connect to V_{AA}
V_{DD}_IO_PHY	C9	Power	Power to MIPI and HiSPi PHYs	Use 1.8V nominal for HiSPi HiVCM or Sub−LVDS. Use 1.8 V or 2.8 V nominal for MIPI or HiSPi SLVS. Tie to V_{DD}_IO when Parallel interface is used
V_{DD}_SLVS	C6	Power	Reference voltage for HiSPi serial interface	Set according to desired HiSPi output common mode voltage. Use 0.4 V nominal for HiSPi SLVS, otherwise use 1.2 V nominal. Tie to V_{DD} when MIPI is being used
V_{PP}	C11	Power	High voltage supply for programming OTPM	Leave unconnected

SPECTRAL CHARACTERISTICS

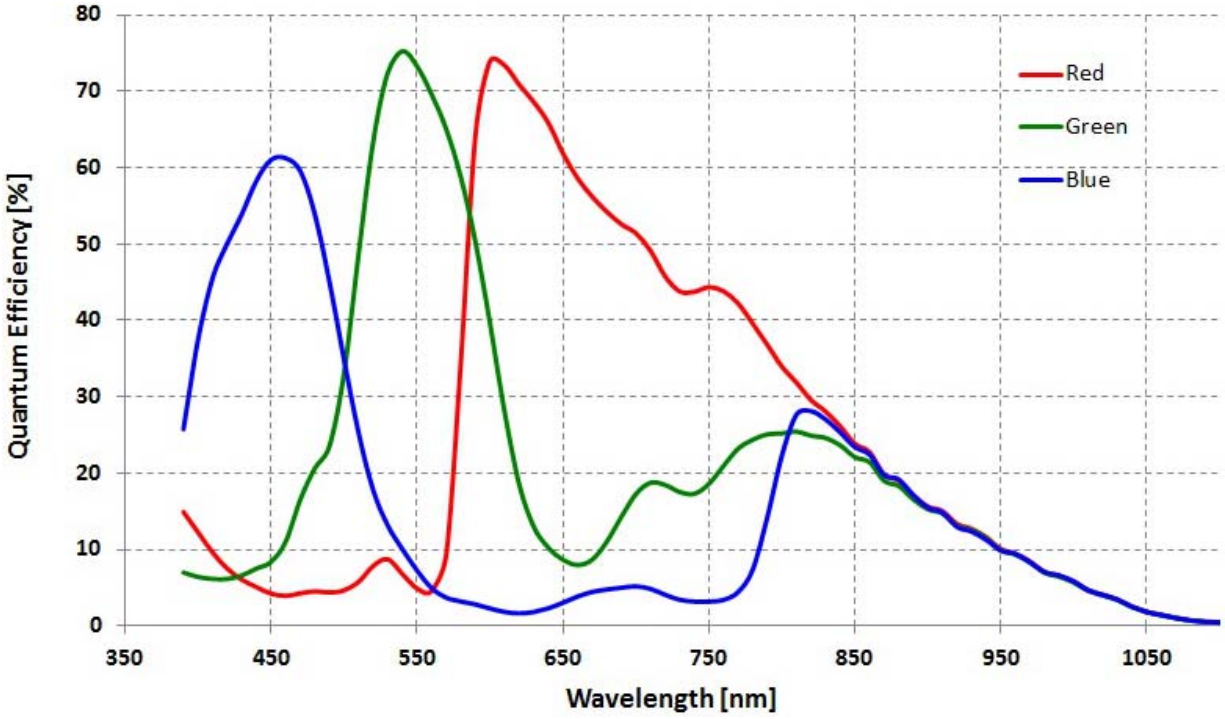


Figure 11. Quantum Efficiency − Color Sensor

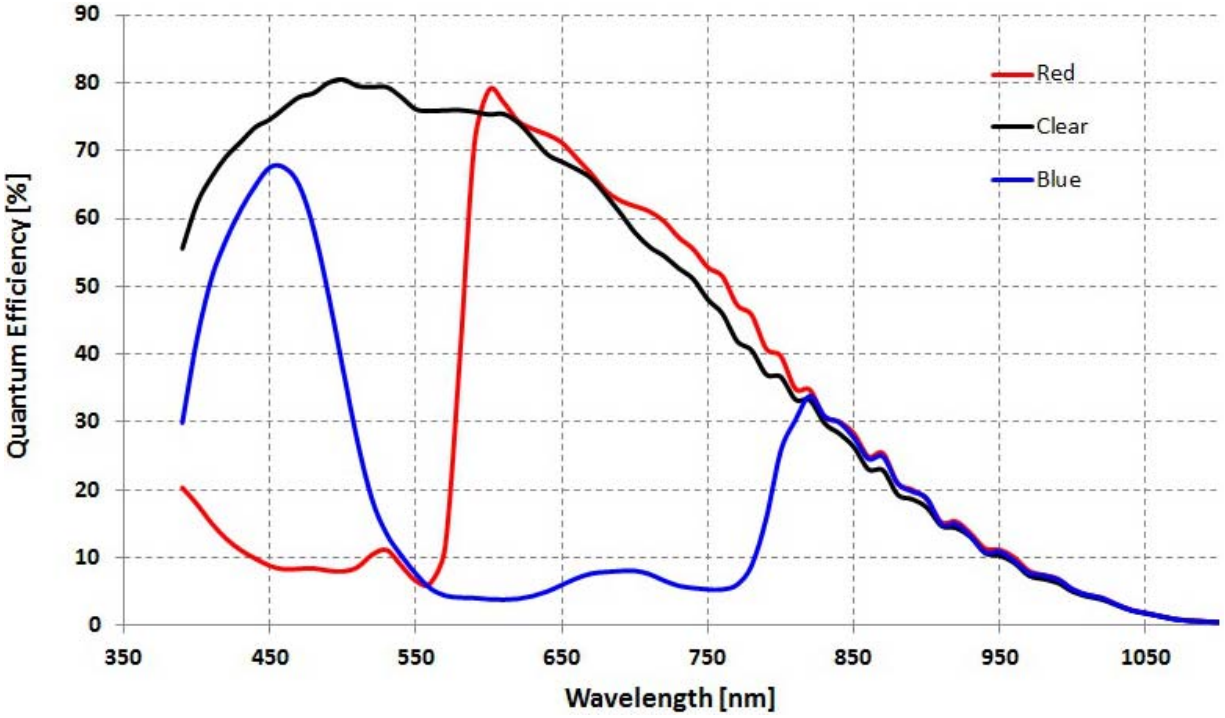
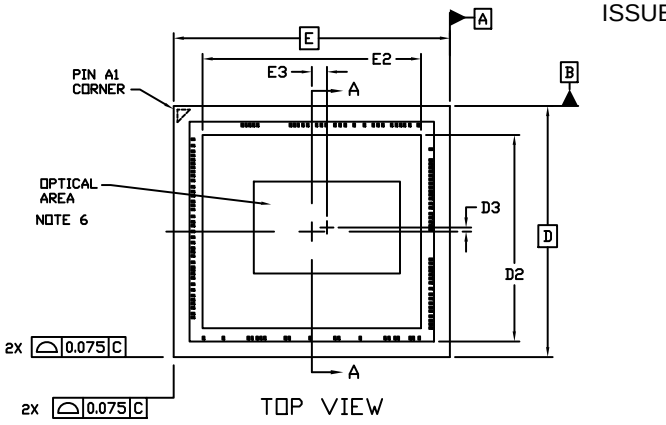
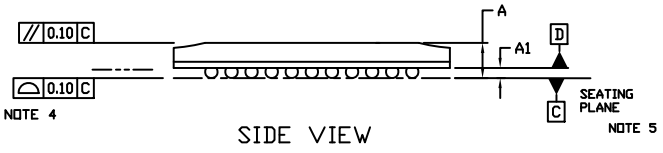


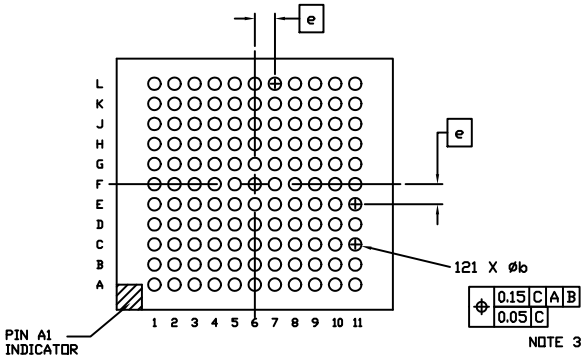
Figure 12. Quantum Efficiency − RCCB Sensor

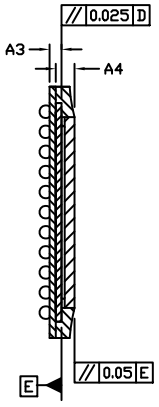
PACKAGE DIMENSIONS

IBGA121 10x11
CASE 503BG
ISSUE O





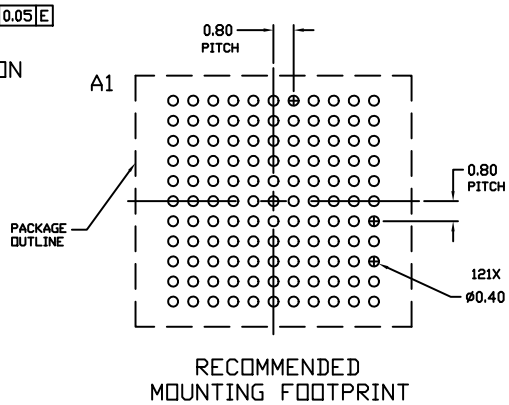




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. DIMENSIONS D3 AND E3 LACATE THE OPTICAL AREA CENTER. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE D AND E WILL BE 1°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY AND IS NOT DELINEATED BY THE LIGHT BLOCK BOUNDARY. REFER TO THE DEVICE DATA SHEET FOR TOTAL ARRAY AND FIRST ACTIVE PIXEL DEFINITIONS.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.55
A1	0.35	0.45
A3	0.425	0.525
A4	0.700	0.800
b	0.45	0.55
D	10.00 BSC	
D2	7.60	7.80
D3	3.66 REF	
E	11.00 BSC	
E2	8.60	8.80
E3	5.82 REF	
e	0.80 BSC	



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