LTC1735 Constant Frequency Synchronous DC/DC Converter

DESCRIPTION

Demonstration Circuit DC247 demonstrates a 1.6V/9A notebook CPU application using the LTC®1735 switching regulator controller. A high performance, constant frequency, current mode architecture generates a precise low voltage CPU core supply. Protection features include an externally defeatable overcurrent latchoff and internal current foldback for overload conditions. A soft-latched crowbar monitors the output voltage for overvoltage protection. The circuit was designed for a 5V to 26V input range but allows a 4.5V to 28V range (limited by the external MOSFETs). Strong output drivers easily handle large power MOSFETs efficiently. Other output voltages, to as low as 0.8V, can be configured by modifying the external resistive divider. External frequency synchronization is provided, as are three modes of operation: Burst Mode™ operation to reduce switching losses and maintain high operating efficiencies, burst inhibit/forced continuous mode and a pulse-skipping mode that provides constant frequency operation down to 1% maximum load currents with low quiescent current. This results in a power supply that has very high efficiency, low ripple and fast transient response. **Gerber files for this circuit board are available. Call the LTC factory.**

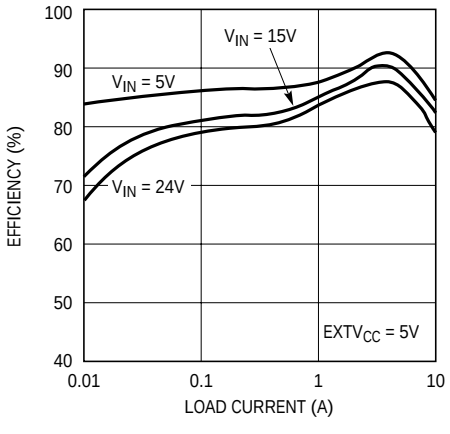
PERFORMANCE SUMMARY

Operating Temperature Range 0°C to 50°C

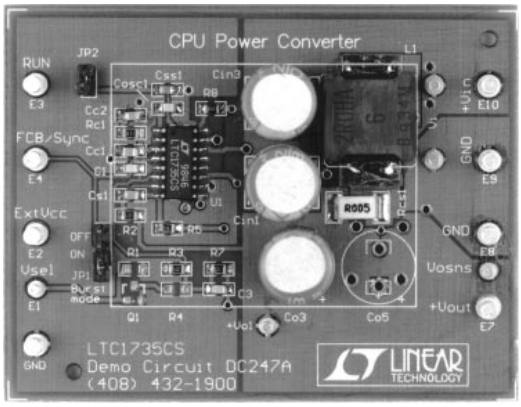
PARAMETER	CONDITIONS	VALUE
Input Voltage Range	(Maximum Input Voltage Limited by External MOSFET and Input Capacitor)	4.5V to 26V
Output	Output Voltage	1.6V
	Max Output Current (Continuous, Thermally Limited)	9A
	Max Output Current (Peak)	10.5A
	Typical Output Ripple at 10MHz Bandwidth (Burst Mode Operation) I_O = 100mA	50mV$_{P-P}$
	Typical Output Ripple at 10MHz Bandwidth (Continuous) I_O = 5A	25mV$_{P-P}$

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Efficiency



Demo Circuit 247A



PERFORMANCE SUMMARY

Operating Temperature Range 0°C to 50°C

PARAMETER	CONDITIONS	VALUE
V_{IN}	Line Regulation 4.5V to 26V	0.002%/V
I_{OUT}	Load Regulation No Load to Full Rated Output	–0.03%
I_Q	Supply Current (Typical) with No Load at 15V Input, FCB = $INTV_{CC}$	500µA
	Supply Current in Shutdown (Typical), V_{IN}=15V, JP2 Open	15µA
I_{EXTVCC}	$EXTV_{CC}$ Pin Current, V_{EXTVCC} = 5V, V_{IN} = 10V, No Load, FCB = $INTV_{CC}$	460µA
V_{RUN}	Run Pin Threshold (Typical)	1.3V
Frequency	Operating Frequency (Typical), C_{OSC} = 47pF	270kHz

PACKAGE AND SCHEMATIC DIAGRAMS

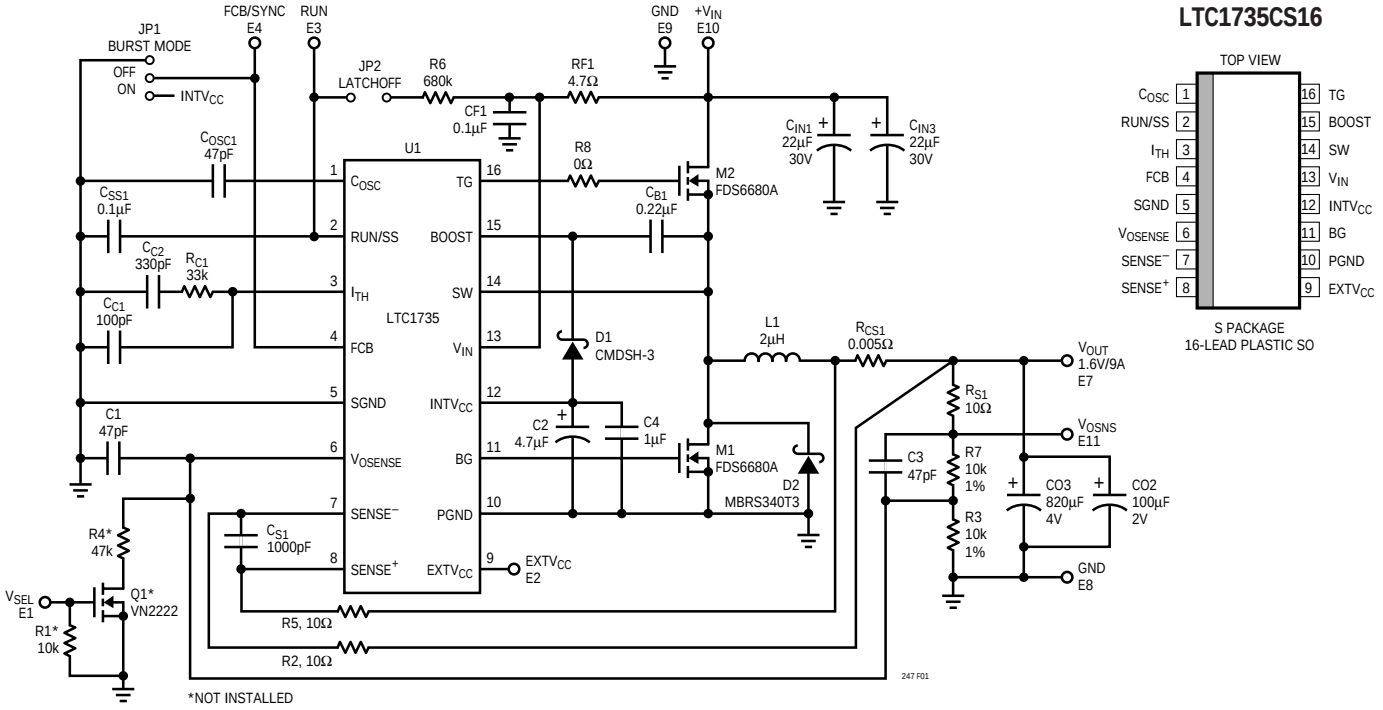


Figure 1. Demo Board Schematic

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1, C3	2	08055A470JAT1A	47pF 50V 5% NPO Capacitor	AVX	(843) 946-0362
C2	1	TACC475M010R	4.7µF 10V 20% Tantalum Capacitor	AVX	(207) 282-5111
C4	1	0805ZC105MAT1A	1µF 10V 20% X7R Capacitor	AVX	(843) 946-0362
C_{C1}	1	08055A101MAT1A	100pF 50V 5% NPO Capacitor	AVX	(843) 946-0362
C_{C2}	1	08055A331MAT1A	330pF 50V 5% NPO Capacitor	AVX	(843) 946-0362
CB1	1	08055A224KAT1A	0.22µF 50V 20% X7R Capacitor	AVX	(843) 946-0362

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
CF1, C_{SS1}	2	08055A104KAT1A	0.1µF 50V 20% X7R Capacitor	AVX	(843) 946-0362
C_{IN1}, C_{IN2}	2	30SC22M	22µF 30V OS-CON Capacitor	SANYO	(619) 661-6835
C_{IN3}, C_{IN4}	ALTERNATE	THCR70E1H2262T	22µF 50V 20% Y5U Capacitor	Marcon	(847) 696-2000
CO1, CO2, CO4	ALTERNATE	TS10X4470JAT1A	470µF 6.3V Low ESR Capacitor	Kemet	(408) 986-0424
CO1, C02, C04	ALTERNATE	EEFUE0G181R	180µF 4V SP Capacitor	Panasonic	(201) 348-7522
CO3	1	4SP820M	820µF 4V OS-CON Capacitor	SANYO	(619) 661-6835
CO2	1	EEFCD0D101R	100µF 2V SP Capacitor	Panasonic	(201) 348-7522
C_{OSC1}	1	08055A470JAT1A	47pF 50V 5% NPO Capacitor	AVX	(843) 946-0362
C_{S1}	1	08055A102MAT1A	1000pF 50V 5% NPO Capacitor	AVX	(843) 946-0362
C4	1	0805ZC105MAT1A	1µF 10V 20% X7R Capacitor	AVX	(843) 946-0362
D1	1	CMDSH-3	0.1A BVR = 30V Schottky Diode	Central	(516) 435-1110
D2	1	MBRS340T3	3A BVR = 40V Schottky Diode	Motorola	(800) 441-2447
E2, E3, E4, E7–E10	7	1502-2	Turret Terminal	Keystone	(718) 956-8900
JP1	1	2802S-03-G2	2mm Pin Header	Comm Con	(626) 301-4200
JP2	1	2802S-02-G2	2mm Pin Header	Comm Con	(626) 301-4200
L1	1	ETQP6F2ROHFA	2µH Inductor	Panasonic	(201) 348-7522
M1, M2	2	FDS6680A	0.013Ω 30V N-Channel MOSFET	Fairchild	(408) 822-2126
Q1	OPTIONAL	VN2222	10Ω 20V N-Channel MOSFET		
R1	OPTIONAL	CR16-103JM	10k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R2, R5, R_{S1}	3	CR16-100FM	10Ω 1/10W 1% Chip Resistor	TAD	(800) 508-1521
R3, R7	2	W0805-03-1002B	10k 1/10W 0.1% Chip Resistor	IRC	(361) 992-7900
R4	OPTIONAL		USER DEF 1/10W 1% Chip Resistor		
R6	1	CR16-684JM	680k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R8	1	CR16-000M	0Ω 1/10W Chip Resistor	TAD	(800) 508-1521
R_{C1}	1	CR16-333FM	33k 1/10W 5% Chip Resistor	TAD	(800) 508-1521
R_{CS1}	1	LRF2010-01-R005J	0.005Ω 1W 5% Resistor	IRC	(512) 992-7900
RF1	1	CR16-470JM	4.7Ω 1/10W 5% Chip Resistor	TAD	(800) 508-1521
U1	1	LTC1735CS16	IC, Switching Regulator Controller	LTC	(408) 432-1900
	2	CCIJ2mm-138-G	Jumper	Comm Con	(626) 301-4200

QUICK START GUIDE

This demonstration board is easily set up to evaluate the performance of the LTC1735. Please follow the procedure outlined below for proper operation. Soldered wire connections are required to properly ascertain the performance of this switching regulator.

- Refer to Figure 2 for proper connection of monitoring and measurement equipment.
- Connect the input power supply to the V_{IN} and GND terminals on the right hand side of the board with soldered connections. Do not increase V_{IN} over 28V or the MOSFET(s) WILL BE DAMAGED.
- Connect the load between the V_{OUT} and GND terminals on the right side of the board with soldered connections.
- The RUN pin can be left unconnected. To shut down the LTC1735, tie this pin to ground.
- If an external 5V supply is used, connect it to $EXTV_{CC}$.

QUICK START GUIDE

- Set the jumper JP1 so that FCB selects the desired mode:

JP1	MODE
On	Burst Mode Operation Enabled
Off	Forced Continuous, Burst Disabled
Open	Apply External Clock to FCB/Sync Pin

- Jumper JP2 determines if the overcurrent latchoff is enabled. With JP2 installed, this function is disabled. Remove JP2 to enable.

JP2	OVERCURRENT LATCHOFF
Installed	Disabled
Removed	Enabled

- Active loads can cause confusing results. Refer to the active load discussion in the operation section.

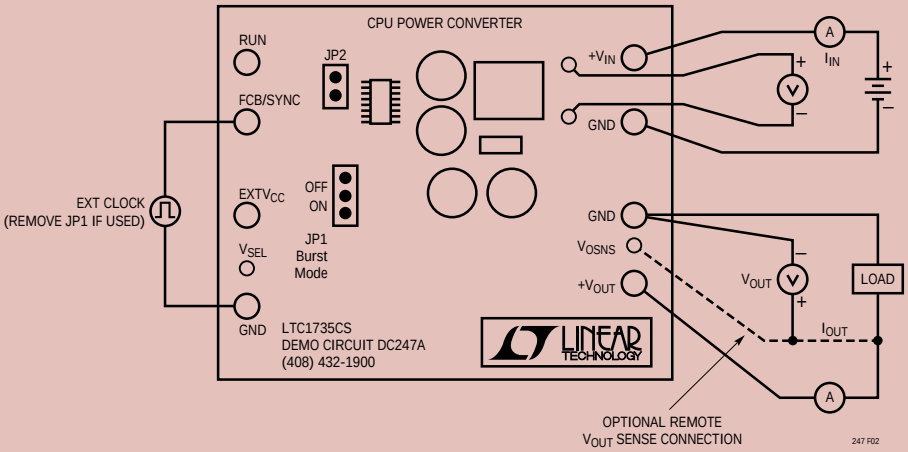


Figure 2. Proper Measurement Setup

INTRODUCTION

The circuit in Figure 1 highlights the capabilities of the LTC1735.

The LTC1735 is a synchronous step-down switching regulator controller that drives external N-channel power MOSFETs using a fixed frequency architecture. Burst Mode operation provides high efficiency at low load currents. Operating efficiencies typically exceed 80% over decades of load current range. A maximum high duty cycle limit of 99% provides low dropout operation, which extends operating time in battery-operated systems.

Do not use spring-clip leads when testing this circuit. Soldered wire connections are required to properly ascertain the performance of the PC board.

This demonstration circuit is intended for the evaluation of the LTC1735 switching regulator IC and was not designed for any other purpose.

OPERATION

The operating frequency is set by an external capacitor, C_{OSC1}, allowing maximum flexibility in optimizing efficiency. In this application, the frequency is set to 270kHz. A multifunction control pin, FCB, inhibits Burst Mode operation, reducing noise and RF interference and allows synchronization to an external oscillator.

Soft-start is provided by an external capacitor, C_{SS1}, which can be used to properly sequence supplies. The operating current level is user-programmable via an external current sense resistor, R_{CS1}, and is set to approximately 10A. Short-circuit current is limited to approximately 3A by internal current foldback.

OPERATION

Main Control Loop

The LTC1735 uses a constant frequency, current mode step-down architecture. Current mode operation was judged to be mandatory for its well known advantages of clean start-up, accurate current limit and excellent line and load regulation in wide input voltage range applications.

During normal operation, the top MOSFET is turned on during each cycle when the oscillator sets a latch and turned off when the main current comparator resets the latch. The peak inductor current is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier EA.

The V_{OSENSE} pin allows the EA to receive an output feedback voltage, V_{FB}, from an external resistive divider. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which, in turn, causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse or the beginning of the next cycle.

The top MOSFET driver is biased from floating bootstrap capacitor C_{B1}, which is normally recharged during each off cycle. However, when V_{IN} decreases to a voltage close to V_{OUT}, the regulator may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the top MOSFET remains on and periodically forces a brief off period to allow C_{B1} to recharge.

HOW TO MEASURE VOLTAGE REGULATION

When trying to measure voltage regulation, remember that all measurements must be taken at the point of regulation. This point is where the LTC1735's control loop looks for the information to keep the output voltage constant. In this demonstration board, it is located between Pin 5 of the LTC1735, the signal ground, and the sense side of R_{S1}. This point corresponds to the V_{OSNS} terminal of the board. Output voltage test leads should be attached directly to this terminal. The load should be placed across $+V_{OUT}$ (E7) and GND (E8). Measurements **should not** be taken at the end of test leads at the load; refer to Figure 2 for the proper monitoring equipment configuration.

This applies to line regulation (input to output voltage regulation) as well as load regulation tests. In doing line regulation tests, always look at the input voltage across the input terminals.

REMOTE OUTPUT VOLTAGE SENSING

Remote output voltage sensing can be accomplished by connecting the V_{OSNS} terminal with another wire directly to the load. A 10Ω resistor, R_{S1}, connects $+V_{OUT}$ to V_{OSNS} to avoid open sense conditions. Never under any circumstance connect the load to V_{OSNS}!

$INTV_{CC}$ Regulator

An internal P-channel, low dropout regulator produces the 5.2V supply that powers the drivers and internal circuitry within the LTC1735. The $INTV_{CC}$ pin can supply up to 50mA (this includes the gate-drive currents). External loading of the $INTV_{CC}$ pin can be thermally limited (allow 10mA to 20mA for gate-drive currents). At high input voltages, the maximum junction temperature rating for the LTC1735 may be exceeded if too large an external load is placed on $INTV_{CC}$. See the LTC1735 data sheet for further details.

$EXTV_{CC}$ CONNECTION

The LTC1735 contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. The switch closes and supplies the $INTV_{CC}$ power whenever the $EXTV_{CC}$ pin is above 4.7V; it remains closed until $EXTV_{CC}$ drops below 4.5V. This allows the MOSFET driver and control power to be derived from the $EXTV_{CC}$ pin instead of V_{IN}. Do not apply greater than 7V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} \leq V_{IN}$.

Significant efficiency gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For 5V output regulators, this simply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 1.6V and other lower voltage regulators, additional circuitry is required to derive $INTV_{CC}$ power from the output.

OPERATION

The following are the most common possible connections for $EXTV_{CC}$ for low output voltage applications:

1. $EXTV_{CC}$ left open (or grounded): this will cause $INTV_{CC}$ to be powered from the internal 5.2V regulator, resulting in an efficiency penalty of up to 10% at high input voltages.

2. $EXTV_{CC}$ connected to an external supply: if an external high efficiency supply is available in the 5V to 7V range ($EXTV_{CC} \leq V_{IN}$), it may be used to power $EXTV_{CC}$, providing an efficiency boost. The typical connection in a notebook CPU power solution is to connect $EXTV_{CC}$ to the main 5V system power.

LOW CURRENT MODES AND SYNCHRONIZATION

The FCB input pin, set by jumper JP1 and FCB/Sync terminal E4, allows the selection of the low current operating mode and external frequency synchronization of the switching regulator.

Tying the FCB pin to ground with JP1 forces the controller into PWM or forced continuous mode. In forced continuous mode, the output MOSFETs are always driven, regardless of output loading conditions. Operating in this mode allows the switching regulator to source or sink current—but be careful; when the output stage sinks current, power is transferred back into the input supply terminals and the input voltage rises.

Burst Mode operation is enabled when the voltage applied to the FCB pin is greater than 0.8V (i.e., JP1 tied to $INTV_{CC}$) or if the pin is left open. A comparator with a precision 0.8V threshold allows the pin to be used to regulate a secondary winding on the switching regulator's output. A small amount of hysteresis is included in the design of the comparator to facilitate clean secondary operation. When the resistively divided secondary output voltage falls below the 0.8V threshold, the controller operates in forced continuous operating mode for as long as it takes to bring the secondary voltage above the 0.8V + hysteresis level.

The internal LTC1735 oscillator can be synchronized to an external oscillator by clocking the FCB pin with a signal above $1.5V_{P-P}$ (remember to remove jumper JP1). When synchronized to an external frequency, Burst Mode operation is disabled but cycle skipping is allowed at low load currents since current reversal is inhibited. The bottom gate will be powered every 10 clock cycles to ensure that the bootstrap capacitor is kept charged. The rising edge of an external clock applied to the FCB pin starts a new cycle.

When synchronized to an external clock, burst inhibit mode allows heavily discontinuous, constant frequency operation down to approximately 1% of maximum designed load current. This mode results in the elimination of switching frequency subharmonics over 99% of the output load range. Switching cycles start to be dropped at approximately 1% of maximum designed load current in order to maintain proper output voltage.

The range of synchronization is from 240kHz to 350kHz, with C_{OSC} = 47pF. Attempting to synchronize to a higher frequency than 350kHz can result in inadequate slope compensation and cause loop instability with high duty cycles (V_{OUT} > 2.5V only). If loop instability is observed while synchronized, additional slope compensation can be obtained by simply decreasing C_{OSC}.

The following table summarizes the possible states available on the FCB/Sync pin:

Table 1

FCB Pin	Condition
DC Voltage: 0V to 0.7V	Burst Disabled/Forced Continuous Current Reversal Enabled
DC Voltage: ≥ 0.9V	Burst Mode Operation, No Current Reversal
Feedback Resistors	Regulating a Secondary Winding
Ext Clock: (0V to $V_{FCBSYNC}$) ($V_{FCBSYNC}$ > 1.5V)	Burst Mode Operation Disabled No Current Reversal

HIGHER CURRENTS AND VOLTAGE PROGRAMMING

The DC247 demo board has various modification provisions for higher output currents and optional output voltages. Additional pad locations for extra output capacitors and footprints for parallel MOSFETs are provided.

Higher current applications with low output voltages may require an additional MOSFET in parallel with M1. When operating at high input voltages, the transition losses of the topside MOSFET (M2) become very significant. Be sure to consider power loss due to transition loss as well as $R_{DS(ON)}$ losses. Don't over specify the topside MOSFET. (Refer to the LTC1735 data sheet for details.)

OPERATION

Uninstalled devices Q1, R1, R4 and the V_{SEL} pin on the demo board allow logic selectable output voltages. With the V_{SEL} pin low, the output voltage is set by R7 and R3. With the V_{SEL} pin high, a higher output voltage is set by R7 and the parallel combination of R3 and R4. This creates a low cost, dynamically programmable mobile processor power supply.

The demonstration board is shipped with the output voltage set to 1.6V but may be modified to produce output voltages as low as 0.8V. Modifications will require changes to the resistive voltage feedback divider (R4, R7) and, in some cases, to the I_{TH} pin compensation components and output capacitors (remember their maximum rated voltage).

Refer to the LTC1735 data sheet for further information on the internal operation and functionality of the IC.

OVERCURRENT AND OVERVOLTAGE PROTECTION

The RUN/SS capacitor, C_{SS1}, is initially used to turn on and limit the inrush current of the controller. After the controller has been started and given adequate time to charge the output capacitor and provide full load current, C_{SS1} is used as a short-circuit time-out circuit. If the output voltage falls to less than 70% of its nominal value, C_{SS1} begins discharging on the assumption that the output is in an overcurrent and/or short-circuit condition. If the condition lasts for a long enough period, as determined by the size of C_{SS1}, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latchoff can be overridden by providing >5µA pullup at a compliance of 4V to the RUN/SS pin by installing jumper JP2. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during an overcurrent and/or short-circuit condition.

Foldback current limiting is activated when the output voltage falls below 70% of its nominal level, whether or not the short-circuit latchoff circuit is enabled.

The output is protected from overvoltage by a "soft-latch." When the output voltage exceeds the regulation value by more than 7.5%, the synchronous MOSFET turns on and remains on for as long as the overvoltage condition is present. If the output voltage returns to a safe level, normal operation resumes. This self-resetting action prevents "nuisance trips" due to momentary transients and eliminates the need for the Schottky diode that is necessary with conventional OVP to prevent V_{OUT} reversal.

With the overcurrent latchoff enabled, a slow ramp on the input voltage may cause the circuit to latch off. Simply recycle the run pin to start. Likewise, if latchoff is disabled and operation with V_{IN} < 5V is anticipated, resistor R6 should be reduced. Refer to the LTC1735 data sheet for details.

ACTIVE LOADS—BEWARE!

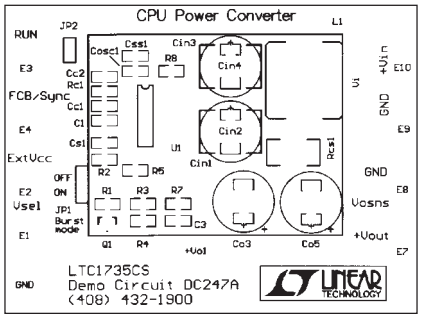
Beware of active loads! They are convenient but problematic. Some active loads do not turn on until the applied voltage rises above 0.1V to 0.8V. The turn-on may be delayed as well. A switching regulator with soft-start may appear to start up, then shut down and eventually reach the correct output voltage. What happens is as follows: at switching regulator turn-on, the output voltage is below the active load's turn-on requirements. The switching regulator's output rises to the correct output voltage level due to the inherent delay in the active load. The active load turns on after its internal delay and now pulls down the switching regulator's output, because the switcher is in its soft-start interval. The switching regulator's output may come up at some later time when the soft-start interval is passed.

A switching regulator with foldback current limit will also have difficulty with the unrealistic I-V characteristic of the active load. Foldback current limiting will reduce the output current available as the output voltage drops below a threshold level (this level is 70% of nominal V_{OUT} for the LTC1735). This reduction in available output current will result in the active load immediately pulling down the output because the active load's current demand remains constant as the output voltage decreases. Most actual loads do not behave like the active load I-V characteristics. Actual loads normally have a $V_{IN} \bullet C \bullet f$ dependency, where C is internal chip capacitance and f is the frequency of operation. To alleviate the active load problem during testing, the active load should be initially programmed to a much lower current value until the switching regulator's soft-start interval has passed and then increased to the

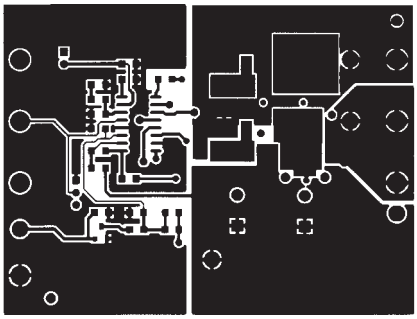
OPERATION

higher level. The switching regulator will supply the increased current required according to the transient response of the switching regulator. Output capacitance needs to be sufficient to accommodate the current step during the transient period, keeping the output voltage at or above the foldback threshold of 70%.

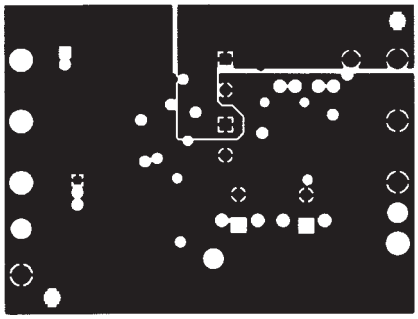
PCB LAYOUT AND FILM



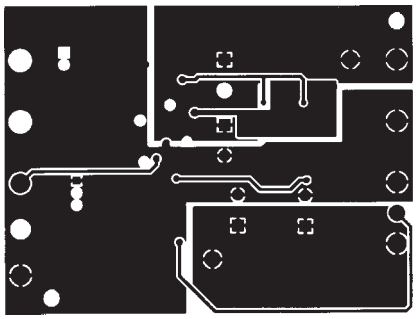
Top Side Silkscreen



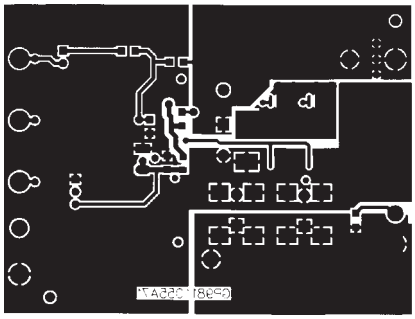
Top Side Copper Layer 1 Top



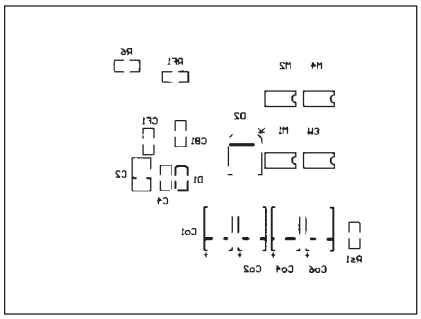
Copper Layer 2



Copper Layer 3

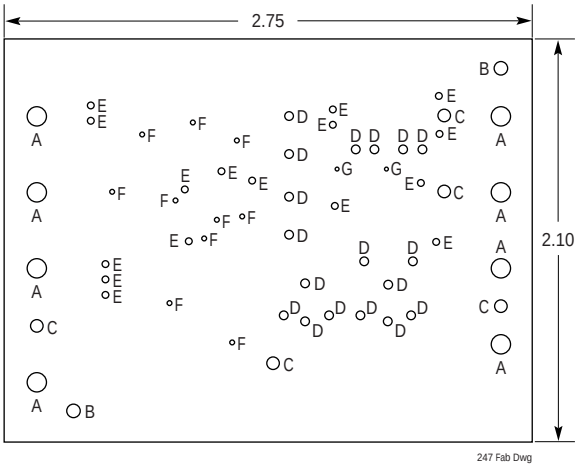


Bottom Side Copper Layer 4



Bottom Side Silkscreen

PC FAB DRAWING



HOLE CHART

SYMBOL	DIAMETER	NUMBER OF HOLES	PLATED
A	100	8	YES
B	70	2	NO
C	65	5	YES
D	45	18	YES
E	35	16	YES
F	25	11	YES
G	20	2	YES
TOTAL		62	

NOTES: UNLESS OTHERWISE SPECIFIED
1. WORKMANSHIP SHALL BE IN ACCORDANCE WITH IPC-A-600E.
2. ALL DIMENSIONS ARE IN INCHES, ±0.003. FINISHED HOLE SIZES ARE +0.003/–0.
3. FINISHED MATERIAL IS FR4, 0.062 THICK, 1 OZ Cu, 4 LAYERS.
   PLATED HOLE WALL THICKNESS 0.001 MIN. INTERNAL LAYERS 1 OZ Cu.
4. PROCESS AND PLATING: SMOBC
5. SOLDERMASK BOTH SIDES USING GLOSSY GREEN LPI.
   SURFACE MOUNT FEATURES EXIST ON BOTH SIDES.
6. SILKSCREEN WHITE NONCONDUCTIVE INK BOTH SIDES.

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