

LTC6430-15

300MHz to 1700MHz Differential ADC Driver/IF/RF Amplifier

DESCRIPTION

Demonstration circuit 2153A features the [LTC6430-15](#) differential ADC/IF Amplifier. The LTC6430-15 has a power gain of 15.2dB and is part of the LTC6430-YY amplifier series.

The DC2153A demo board supports the LTC6430-YY amplifier family. The DC2153A demo board is optimized for the frequency range from 300MHz to 1700MHz and utilizes a minimum of passive external components to configure the amplifier for this application. Because The LTC6430-15

has 100Ω differential input and output impedances, so the demo circuit uses transformers to convert to 50Ω single-ended so that it can be easily evaluated with most RF test equipment.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2153A>

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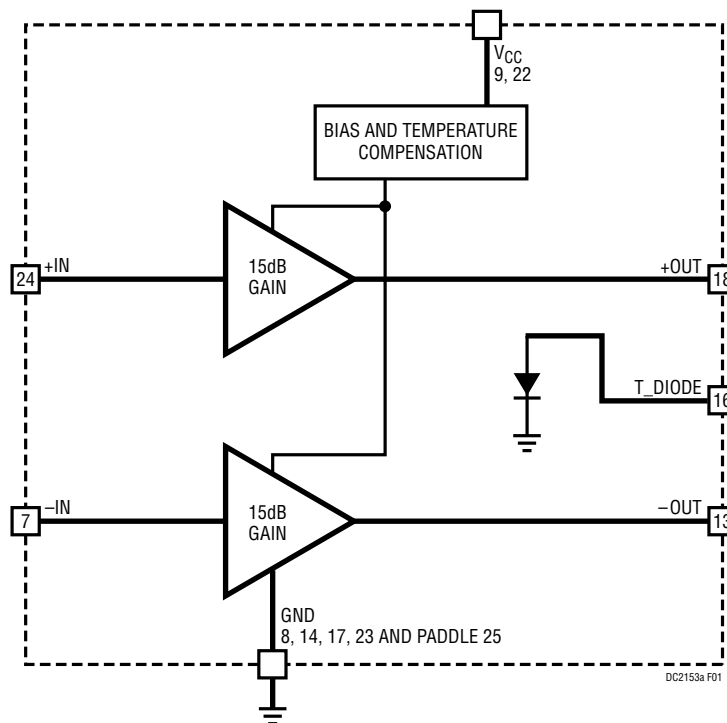


Figure 1. LTC6430-15 Device Block Diagram

DEMO MANUAL DC2153A

PERFORMANCE SUMMARY

Table 1. Typical Demo Board Performance Summary $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$

SYMBOL	PARAMETER	CONDITIONS	UNITS
Power Supply			
V_{CC}	Operating Supply Range	All V_{CC} Pins Plus $\pm\text{OUT}$	4.75V to 5.25V
I_{CC}	Current Consumption	Total Current	165mA

FREQUENCY (MHz)	POWER GAIN $ S_{21} $ (dB)	OUTPUT THIRD-ORDER INTERCEPT POINT ⁽¹⁾ (dBm)	OUTPUT THIRD-ORDER INTERMODULATION POINT ⁽¹⁾ (dBc)	SECOND HARMONIC DISTORTION ^(2, 3) (dBc)	THIRD HARMONIC DISTORTION ^(2, 3) (dBc)	OUTPUT 1dB COMPRESSION POINT (dBm)	NOISE FIGURE ⁽⁴⁾ (dB)
300	11.8	41.6	-79.1	-69.2	-72.4	21.3	4.2
400	12.2	41.9	-79.8	-64.4	-69.3	21.6	4.0
500	12.6	42.1	-80.1	-65.5	-71.6	22.2	4.2
600	12.8	43.6	-83.1	-64.9	-68.7	22.3	4.5
700	13.0	45.0	-86.1	-65.3	-71.5	22.6	4.7
800	13.0	47.2	-90.4	-60.8	-73.1	22.4	4.8
900	12.9	46.8	-89.6	-59.1	-77.1	22.0	4.8
1000	12.8	47.1	-90.2	-58.6	-71.7	21.6	5.1
1100	12.7	46.2	-88.4	-57.9	-67.1	21.6	5.3
1200	12.5	45.6	-87.2	-56.2	-65.6	21.4	5.7
1300	12.4	43.7	-83.3	-56.6	-65.3	21.1	5.9
1400	12.3	43.3	-82.6	-66.7	-63.9	20.8	6.2
1500	12.1	40.0	-76.1	-60.5	-62.2	20.4	6.4
1600	11.9	37.2	-70.3	-56.3	-63.7	20.0	6.6
1700	11.6	34.9	-65.9	-56.1	-66.7	19.7	6.8

Notes: All figures are referenced to J1 (Input Port) and J4 (Output Port).

- Two-tone test conditions: Output power level = 2dBm/tone, tone spacing = 1MHz.
- Single-tone test conditions: Output power level = 6dBm.
- Degraded performance results are due to imbalance from the balun transformers.
- Small signal noise figure.

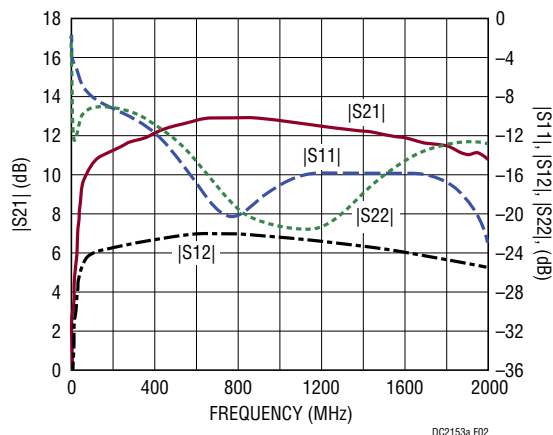


Figure 2. Demo Board S-Parameters

OPERATION

Demo circuit 2153A is a high linearity, fixed gain amplifier. It is designed for ease of use. The LTC6430-15 is internally matched to 100Ω differential source and load impedances from 20MHz to 1400MHz. Due to the unpopularity of 100Ω differential test equipment, transformers have been added to convert these impedances to single-ended 50Ω. The frequency range of the circuit is limited by the balun transformers. Hence, this demo board optimizes the amplifier performance over the frequency range from 300MHz to 1700MHz. Figure 2 shows the two port DC2153A's S-parameters.

The demo circuit's schematic shows a minimum requirement of passive support components. Due to the imbalance from the input and output transformers, the harmonic distortion performance is slightly degraded. The shunt capacitors (C8, C9, C25 and C6) help to balance the input and output signals.

The input and output DC blocking capacitors (C5, C7, C10 and C12) are required because this device is internally DC-biased for optimal operation. The frequency appropriate RF chokes (L2 and L3) and the decoupling capacitors (C2, C3, C15 and C16) provide the proper DC bias to the RF ±OUT ports. A single 5V supply is required for the V_{CC} pins on the device.

L1, L4, C6 and C13 are optional components. They are for additional matching when further optimization to a lower or wider frequency range applications is required.

A pair of stability networks have been added. They consist of a 62pF capacitor (C4 and C11) and 348Ω resistor (R1 and R5) in parallel at the LTC6430-15 input network to ensure low frequency stability.

The T_DIODE pin (Turret E1) can be forward biased to ground with 1mA of current. The measured voltage will be an indicator of the chip junction temperature (T_J).

There is an optional circuit at the upper section of the demo board. This extra circuit can be used to calibrate for the insertion loss of the demo board's input and output components.

Please note that a number of DNC pins are connected on the demo board. These connections are not necessary for normal operation, however, failure to float these pins may impair the operation of the device.

Table 2 shows the function of each input and output on the board.

Table 2. DC2153A Board I/O Descriptions

CONNECTOR	FUNCTION
J1 (IN)	Single-ended input. Impedance matched to 50Ω. Drive from a 50Ω network analyzer or signal source.
J4 (OUT)	Single-ended output. Impedance matched to 50Ω. Drives a 50Ω network analyzer or spectrum analyzer.
E1 (T_DIODE)	The measured voltage will be an indicator of the chip junction temperature.
E2 (V _{CC})	Positive supply voltage source.
E3 (GND)	Supply ground.

ADDITIONAL INFORMATION

As with any RF device, minimizing ground inductance is critical. Care should be taken during the board layout when using these exposed pad packages. A maximum of small-diameter vias should be placed underneath the exposed ground pad. This will ensure a good RF ground and low thermal impedance. Maximizing the copper ground plane will also improve heat spreading and lower the inductance to ground. It is a good idea to cover the via holes with solder mask on the back side of the PCB to prevent solder from wicking away from the critical PCB to the exposed pad interface.

The DC2153A is a wide bandwidth demo board, but it is not intended for operation down to DC. The lower frequency cutoff is limited by on-chip matching elements.

Table 3 shows the LTC643X-YY amplifier series and its associated demo boards. Each demo board lists the typical working frequency range and the input and output impedance of the amplifiers.

Setup Signal Sources and Spectrum Analyzer

The LTC6430-15 is an amplifier with high linearity performance. Therefore, the output intermodulation products are very low. Even using high dynamic range test equipment, third-order intercept (IP3) measurements can drive test setups to their limits. Consequently, accurate measurement of IP3 for a low distortion IC such as the LTC6430-15 requires certain precautions to be observed in the test setup as well as the testing procedure.

Setup Signal Sources

Figure 3 shows a proposed IP3 test setup. This setup has low phase noise, good reverse isolation, high dynamic range, sufficient harmonic filtering and wideband impedance matching. The setup is outlined below:

- a. High performance signal generators one and two (HP8644A) are used. These suggested generators have low harmonic distortion and very low phase noise.
- b. High linearity amplifiers are used to improve the reverse isolation. This prevents cross talk between the two signal generators and provides higher output power.
- c. A low pass filter is used to suppress the harmonic content from interfering with the test signal. Note that second order inputs can mix with the fundamental frequency to form intermodulation (IM) products of their own. We suggest filtering the harmonics to -50dBc or better.
- d. The signal combiner from mini-circuits (ADP-2-9) combines the two isolated input signals. This combiner has a typical isolation of 27dB. For improved VSWR and isolation, the H-9 signal combiner from MA/COM is an alternative which features $>40\text{dB}$ isolation and a wider frequency range. Passive devices (e.g. combiners) with magnetic elements can contribute nonlinearity to the signal chain and should be used cautiously.
- e. The attenuator pads on all three ports of the signal combiner will further support isolation of the two input signal sources. They also reduce reflections and promote maximum power transfer with wideband impedance matching.

Table 3. The LTC643X-YY Amplifier Family and Corresponding Application Demo Boards

DEMO BOARD NUMBER	FREQUENCY RANGE (MHz)	NOTES/ APPLICATIONS	BOARD'S IN/OUT IMPEDANCE	AMPLIFIER	AMPLIFIER'S IMPEDANCE
DC1774A-A	50 to 350	Low Frequency	50Ω	LTC6430-15	Differential 100Ω
DC1774A-B	400 to 1000	Mid Frequency	50Ω	LTC6430-15	Differential 100Ω
DC1774A-C	100 to 1200	Wide Frequency	50Ω	LTC6431-15	Single-Ended 50Ω
DC2032A	50 to 1000	Cable Infrastructure	75Ω	LTC6430-15	Differential 100Ω
DC2077A	100 to 1200	Wide Frequency	50Ω	LTC6431-20	Single-Ended 50Ω
DC2153A	300 to 1700	High Frequency	50Ω	LTC6430-15	Differential 100Ω

ADDITIONAL INFORMATION

Setup the Spectrum Analyzer

- a. Adjust the spectrum analyzer for maximum possible resolution of the intermodulation products' amplitude in dBc. A narrower resolution bandwidth will take a longer time to sweep.
- b. Optimize the dynamic range of the spectrum analyzer by adjusting the input attenuation. First increase the spectrum analyzer's input attenuation (normally in steps of 5dB or 10dB). If the IM product levels decrease when the input attenuation is increased, then the input power level is too high for the spectrum analyzer to make a valid measurement. Most likely, the spectrum analyzer's 1st mixer was overloaded and producing its own IM products. If the IM reading holds constant with increased input attenuation, then a sufficient amount of attenuation was present. Adding too much attenuation will bury the intended IM signal in the noise floor. Therefore, select just enough attenuation to achieve a stable and valid measurement.
- c. In order to achieve this valid measurement result, the test system must have lower total distortion than the DUT's intermodulation. For example, to measure a 47dBm OIP3, the measured intermodulation products will be -90dBc below an -13dBm /tone input level and the test system must have intermodulation products approximately -96dBc or better. For best results, the IM products and noise floor should measure at least -100dBc before connecting the DUT.

QUICK START PROCEDURE

Demo circuit 2153A can be set up to evaluate the performance of the LTC6430-15. Refer to Figure 3 for proper equipment connections and follow the procedure below.

Two-Tone Measurement

Connect all test equipment as suggested in Figure 3.

1. The power labels of V_{CC} 4.75V to 5.25V and GND directly correspond to the power supply. Typical current consumption of the LTC6430-15 is about 165mA.
2. Apply two independent signals f_1 and f_2 from signal generator 1 and signal generator 2 at 1000MHz and 1001MHz, while setting the amplitude to $-13\text{dBm}/\text{tone}$ at the demo board input (J1).
3. Monitor the output tone level on the spectrum analyzer. Adjust the signal generator levels such that the output power measures $2\text{dBm}/\text{tone}$ at the amplifier output J2, after correcting for external cable losses and attenuations.

4. Change the spectrum analyzer's center frequency and observe the two IM3 tones at 1MHz below and above the input frequencies. The frequencies of IM3_LOW and IM3_HIGH are 999MHz and 1002MHz, respectively. The measurement levels should be approximately -90dBc ; 47dBm is typical OIP3 performance for the LTC6430-15 at 1000MHz.

The OIP3 calculation is:

$$\text{OIP3} = P_{\text{OUT}} + \Delta \text{IMD3}/2$$

Where:

P_{OUT} is the lower output signal power of the fundamental products.

$\Delta \text{IMD3} = P_{\text{OUT}} - P_{\text{IM3}}$; P_{IM3} is the higher third-order intermodulation product.

Single-Tone Measurement

5. Continue with step 4 above, turn off one signal source to measure gain and harmonic distortions.

QUICK START PROCEDURE

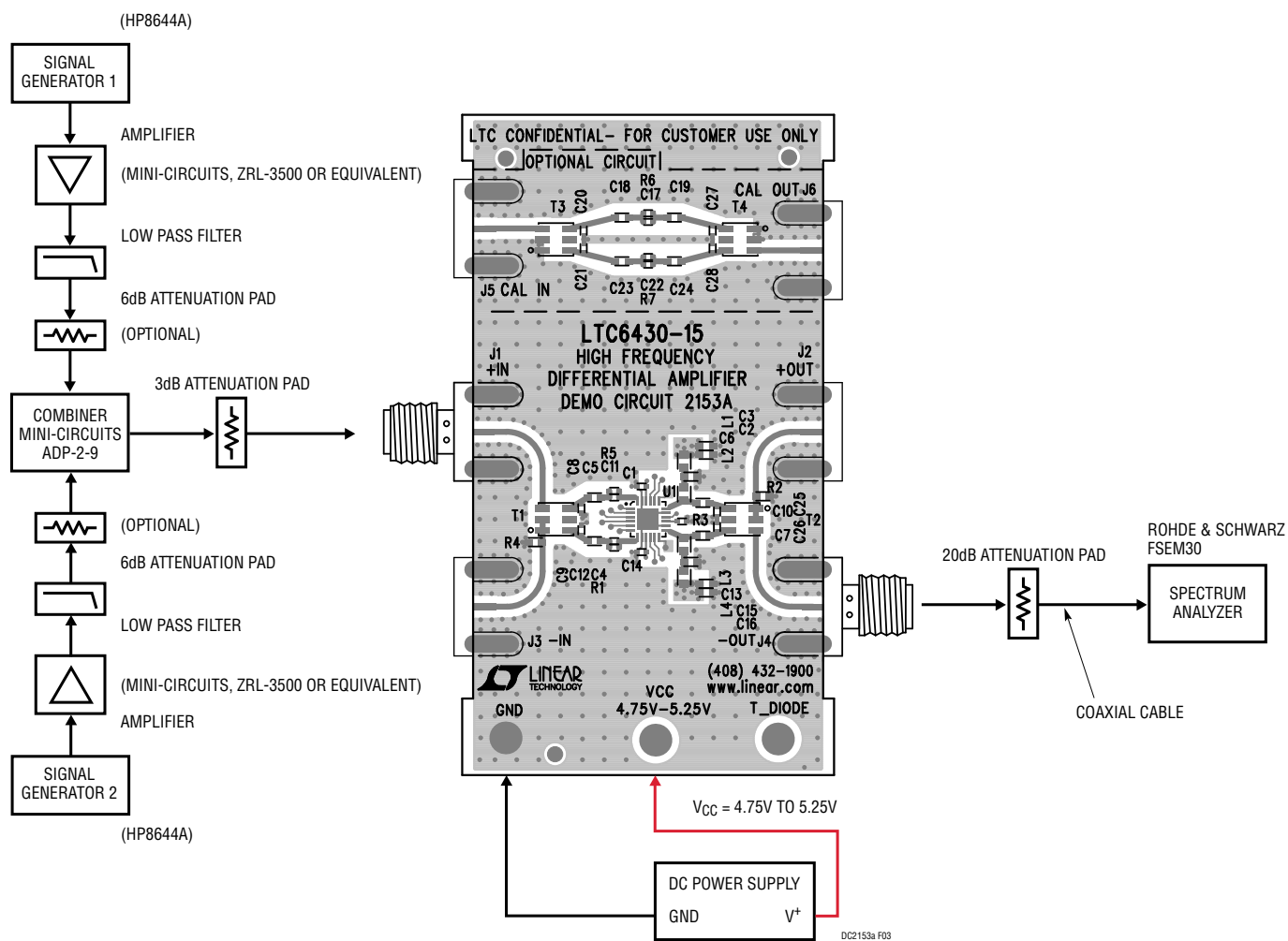


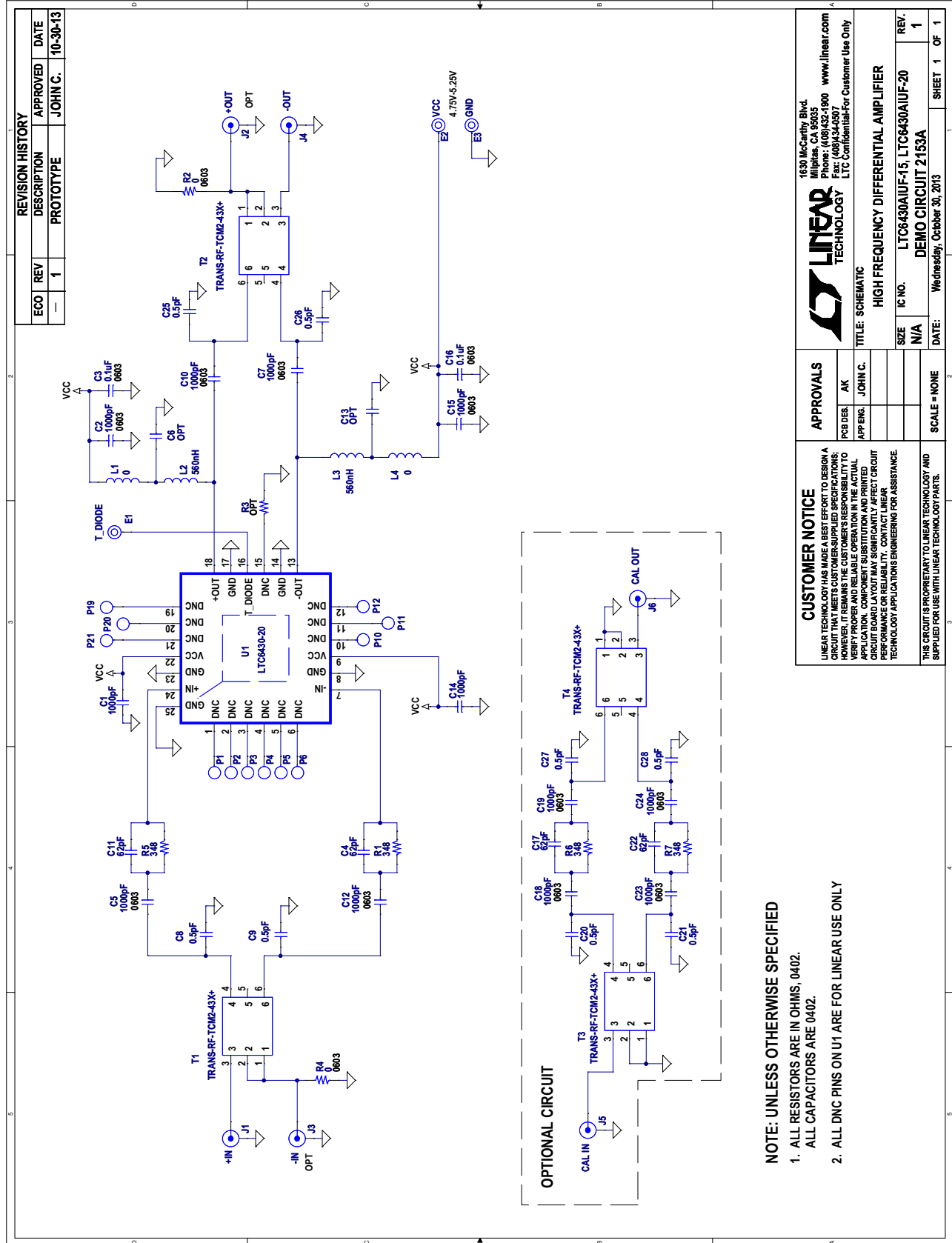
Figure 3. Proper Equipment Setup for IP3 Measurement

DEMO MANUAL DC2153A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, C14	CAP, X7R, 1000pF, 50V 5%, 0402	AVX, 04025C102JAT2A
2	6	C2, C5, C7, C10, C12, C15	CAP, X7R, 1000pF, 50V 5%, 0603	AVX, 06035C102JAT2A
3	0	C18, C19, C23, C24	CAP, 0603, OPT	
4	2	C3, C16	CAP, X5R, 0.1µF, 10V, 10%, 0603	AVX, 0603ZD104KAT2A
5	2	C4, C11	CAP, NPO, 62pF, 25V, 5%, 0402	AVX, 04023A620JAT
6	0	C17, C22	CAP, 0402, OPT	
7	2	C6, C13	CAP, OPT, 0603	
8	4	C8, C9, C25, C26,	CAP, COG, 0.5pF, ±0.1pF 50V, 0402	AVX, 04025A0R7BAT2A
9	0	C20, C21, C27, C28	CAP, 0402, OPT	
10	3	E1 TO E3	TESTPOINT, TURRET, 0.093"	MILL-MAX, 2501-2-00-80-00-00-07-0
11	2	J1, J4	CONN, SMA 50Ω EDGE-LAUNCH	E.F. JOHNSON, 142-0701-851
12	0	J2, J3, J5, J6	CONN, SMA 50Ω EDGE-LAUNCH, OPT	
13	2	L1, L4	RES, CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0ED
14	2	L2, L3	INDUCTOR, CHIP, 560nH, 5%, 0603LS-1608	COILCRAFT, 0603LS-561XJLB
15	2	R1, R5	RES, CHIP, 348, 1%, 0402	VISHAY, CRCW0402348RFKED
16	0	R6, R7	RES, 0402 OPT	
17	2	R2, R4	RES, CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0ED
18	1	R3	RES, 0402 OPT	
19	2	T1, T2	TRANS-RF-TCM2-43X+, CASE STYLE DB1627	MINI-CIRCUITS, TCM2-43X+
20	0	T3, T4	TRANS-RF-TCM2-43X+, CASE STYLE DB1627, OPT	
21	1	U1	BALANCED AMPLIFIER LTC6430AIUF-15, QFN24UF-4X4	LINEAR TECHNOLOGY CORPORATION, LTC6430AIUF-15

SCHEMATIC DIAGRAM



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APPROVALS		TITLE: SCHEMATIC	
PCB DES	AK	IC NO.	LTC6430AUF-15, LTC6430AUF-20
APP ENGR.	JOHN C.	SIZE	N/A
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		SCALE	NONE
		DATE	Wednesday, October 30, 2013
		SHEET	1 OF 1

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