

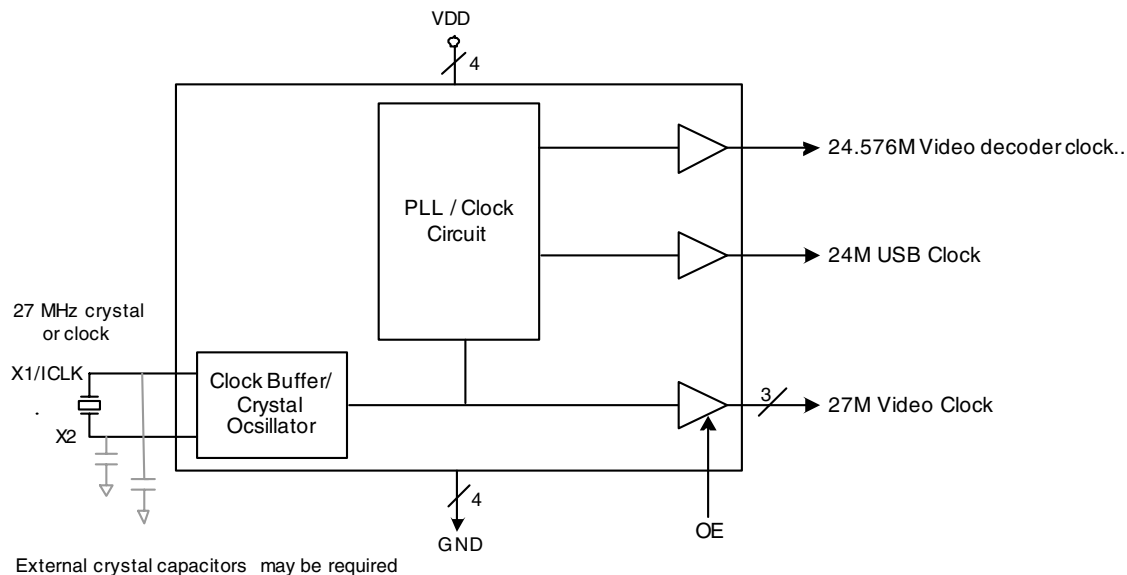
USB-DVR CLOCK SOURCE
MK2746-01
Description

The MK2746-01 is a low cost, low jitter, high performance clock synthesizer for USB-DVR based applications. Using analog Phase Locked Loop (PLL) techniques, the device accepts a 27 MHz fundamental mode crystal or clock input to produce multiple output clocks for USB and Video applications.

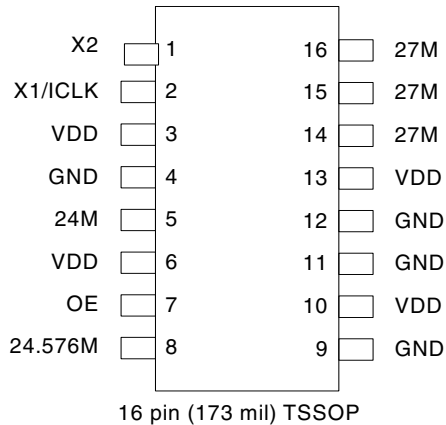
IDT manufactures the largest variety of DVD, set top box, and multimedia clock synthesizers for all applications.

Features

- Packaged in 16 pin TSSOP
- Operating voltage of 3.3 V
- Provides three fixed outputs of 27 MHz, 24.576 MHz (Video), and 24 MHz (USB).
- Advanced, low power, sub-micron CMOS process
- RoHS 5 (green) or RoHS 6 (green and lead free) compliant package

Block Diagram


Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X2	Input	Connect to a 27 MHz fundamental mode crystal. Leave open for clock input.
2	X1/ICLK	Input	Connect to a 27 MHz fundamental mode crystal or clock.
3	VDD	Power	Connect to +3.3 V.
4	GND	Power	Connect to ground.
5	24M	Output	24MHz USB clock output . Internal pull-down to low when OE is low.
6	VDD	Power	Connect to +3.3 V.
7	OE	Input	Output enable (OE high enables outputs). Internal pull-up.
8	24.576M	Output	24.576 MHz clock output. Internal pull-down to low when OE is low.
9	GND	Power	Connect to ground.
10	VDD	Power	Connect to +3.3 V.
11	GND	Power	Connect to ground.
12	GND	Power	Connect to ground.
13	VDD	Power	Connect to +3.3 V.
14	27M	Output	27 MHz clock output. Internal pull-down to low when OE is low.
15	27M	Output	27 MHz clock output. Internal pull-down to low when OE is low.
16	27M	Output	27 MHz clock output. Internal pull-down to low when OE is low.

External Component Selection

The MK2746-01 requires a minimum number of external components for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μ F should be connected between VDD and GND as close to the MK2746-01 as possible. For optimum device performance, the decoupling

capacitors should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB traces between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace

impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Tuning Load Capacitors

For a crystal input, a parallel resonant fundamental mode crystal should be used. Crystal capacitors must be connected between each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should equal $(CL-6)*2$. In this equation CL is equal to the crystal load capacitance in pF. As an example, for a crystal with an 18pF load capacitance, each crystal capacitor would be 24pF $[(18-6)*2]=24$.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should

be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK2746-01-01. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2746-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

VDD=3.3V ±10% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V _{IH}		2.0			V
Input Low Voltage	V _{IL}				0.8	V
Input High Voltage	V _{IH}	ICLK	(VDD/2)-1	VDD/2		V
Input Low Voltage	V _{IL}	ICLK		VDD/2	(VDD/2)+1	V
Output High Voltage	V _{OH}	I _{OH} = -20 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 20 mA			0.4	V
Output High Voltage (CMOS Level)	V _{OH}	I _{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, OE=1		21		mA
		No load, OE=0		15		mA
Short Circuit Current	I _{OS}			±50		mA
Input Capacitance	C _{IN}			5		pF
Nominal Output Impedance	Z _{OUT}			20		Ω
On Chip Pull Up Resistor	R _{PU}			510		kΩ
On Chip Pull Down Resistor	R _{PD}			240		kΩ

AC Electrical Characteristics

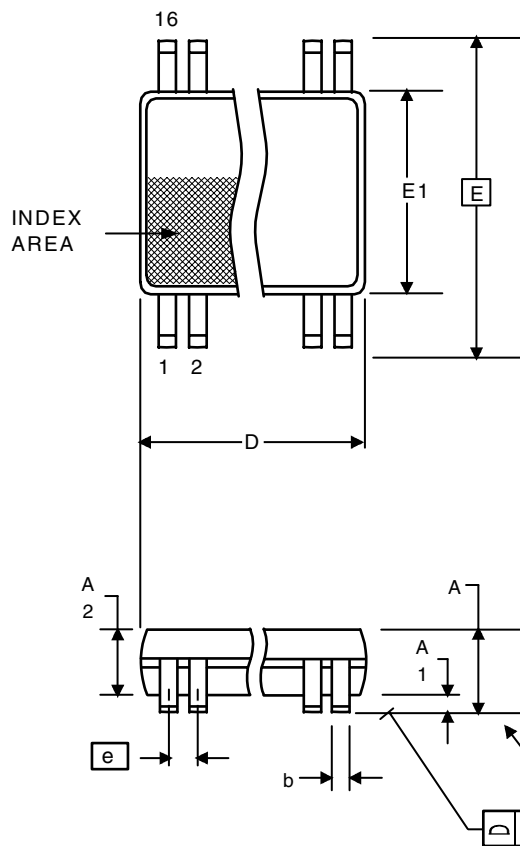
VDD = 3.3V ±10%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				27		MHz
Output Rise Time	t _{OR}	20% to 80% of VDD, Note 1		1.2	1.8	ns
Output Fall Time	t _{OF}	80% to 20% of VDD, Note 1		1.2	1.8	ns
Output Clock Duty Cycle	t _D	at VDD/2, Note 1	45	50	55	%
Maximum Output Jitter, short term	t _J	All clocks, except REF clocks Note 1		±75		ps
		REF clocks, Note 1		±150		ps
Output Enable time		OE high to valid output (PLL running)			20	ns
Output Disable time		OE low to output disable			20	ns

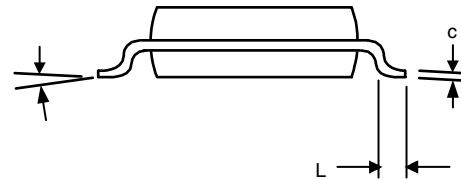
Note 1: Measured with 15pF load.

Package Outline and Package Dimensions (16 pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK2746-01GLF	274601GL	Tubes	16 pin TSSOP	0 to +70° C
MK2746-01GLFT	274601GL	Tape and Reel	16 pin TSSOP	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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