

74LVC16374A; 74LVCH16374A

16-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

Rev. 07 — 23 March 2010

Product data sheet

1. General description

The 74LVC16374A and 74LVCH16374A are 16-bit edge-triggered flip-flops featuring separate D-type inputs with bus hold (74LVCH16374A only) for each flip-flop and 3-state outputs for bus oriented applications. It consists of two sections of eight positive edge-triggered flip-flops. A clock input (nCP) and an output enable (nOE) are provided for each octal.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition.

When pin nOE is LOW, the contents of the flip-flops are available at the outputs. When pin nOE is HIGH, the outputs go to the high-impedance OFF-state. Operation of input nOE does not affect the state of the flip-flops.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pin-out architecture
- Low inductance multiple supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16374A only)
- High-impedance outputs when $V_{CC} = 0$ V
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ CDM JESD22-C101D exceeds 1000 V
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

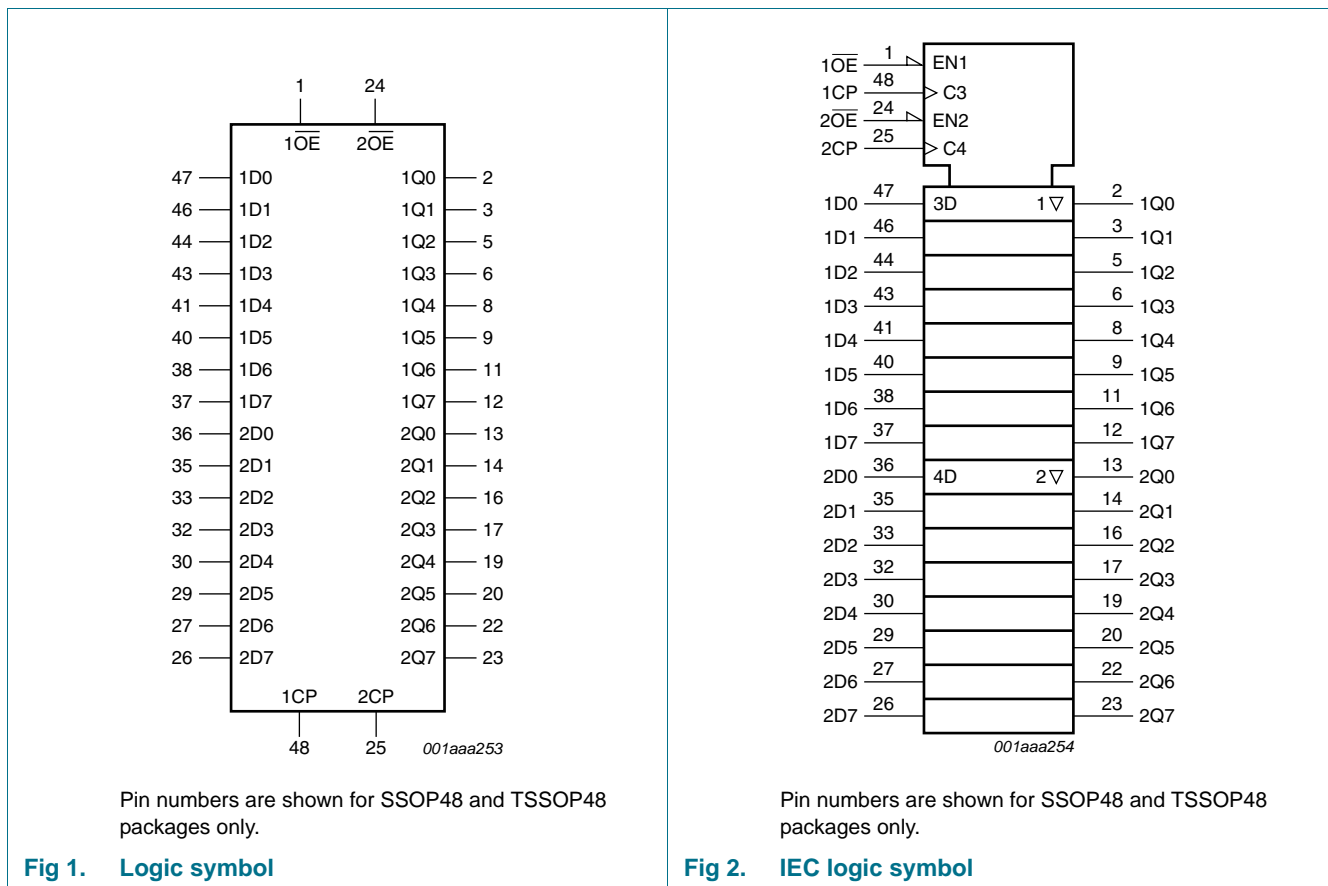


3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC16374ADL 74LVCH16374ADL	-40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVC16374ADGG 74LVCH16374ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVC16374ABQ 74LVCH16374ABQ	-40 °C to +125 °C	HXQFN60U	plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 4 x 6 x 0.5 mm	SOT1134-1

4. Functional diagram



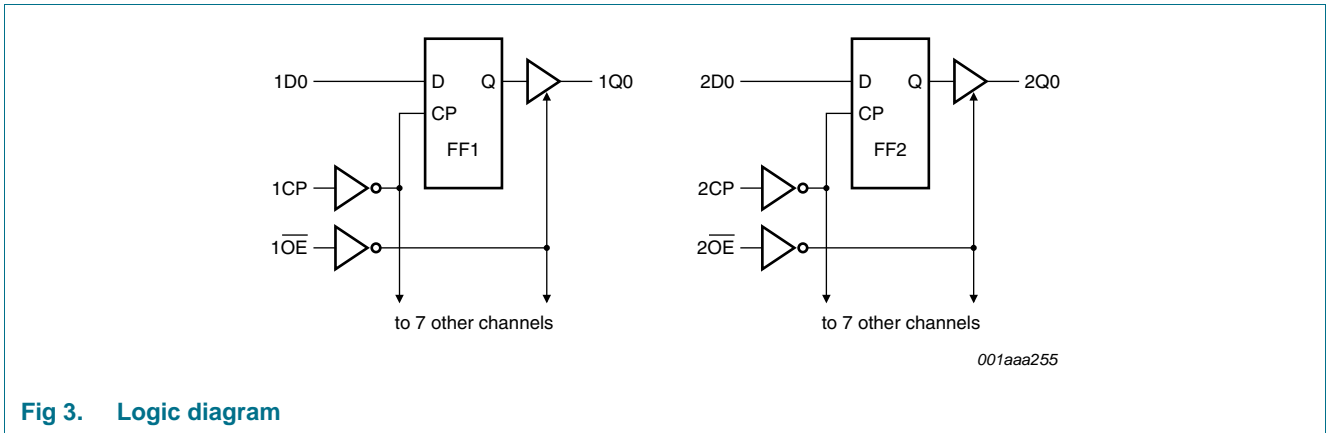


Fig 3. Logic diagram

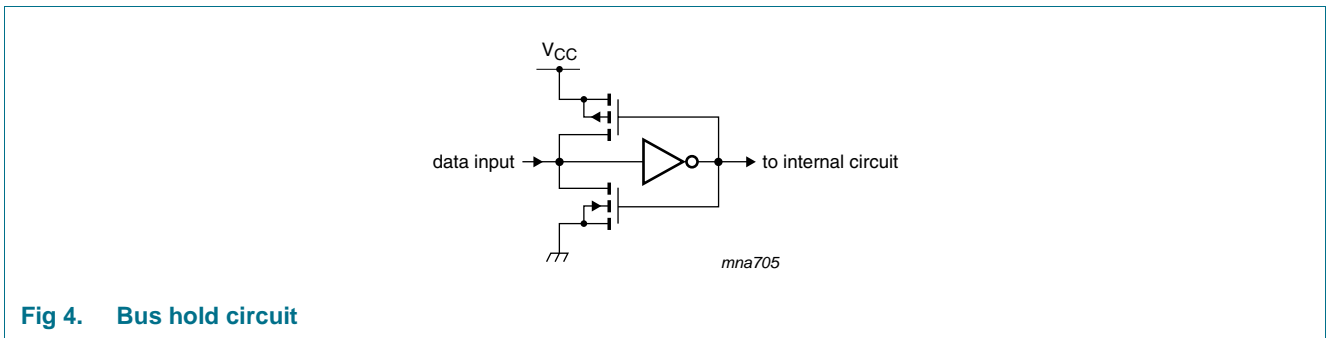
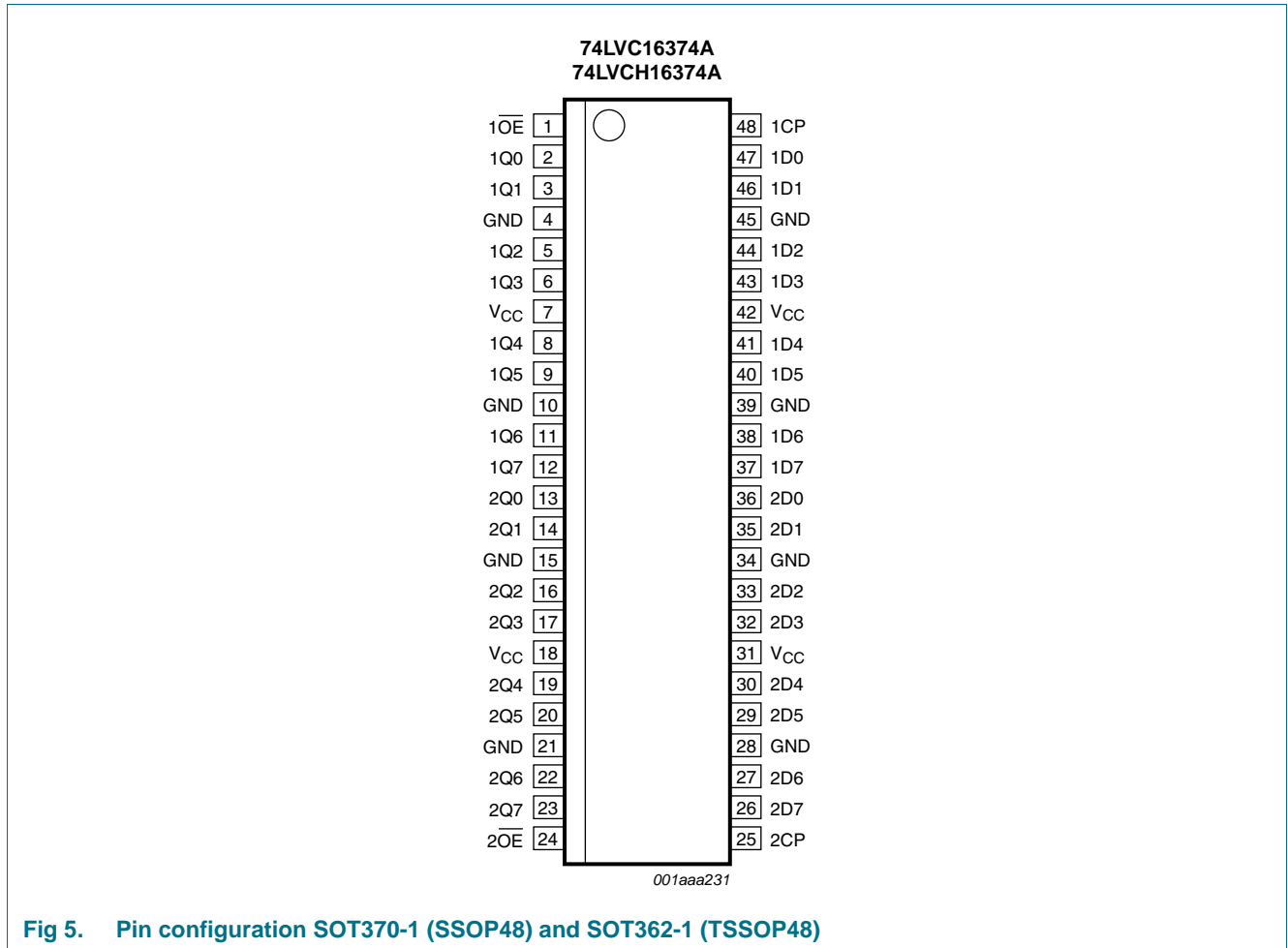
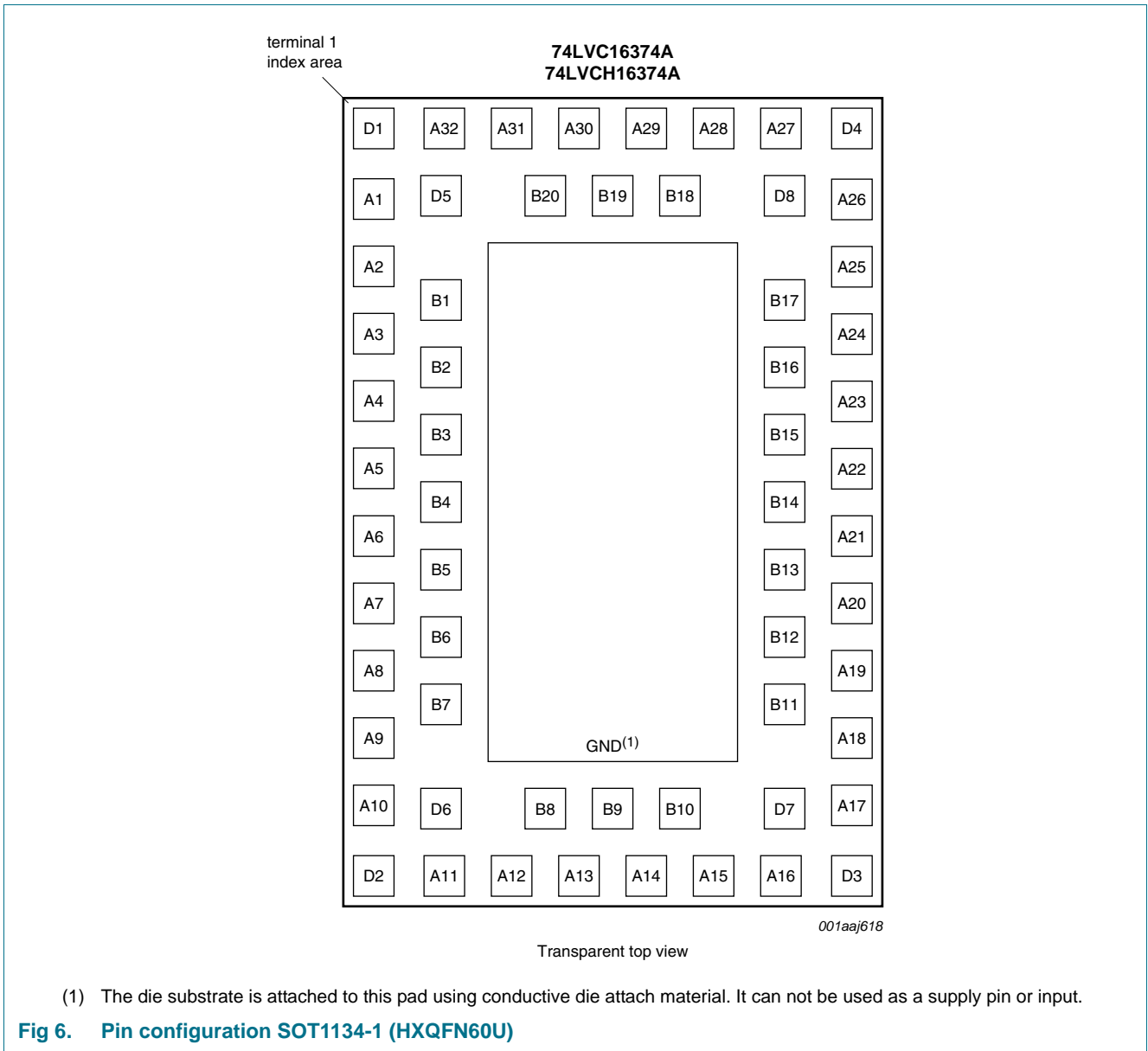


Fig 4. Bus hold circuit

5. Pinning information

5.1 Pinning





5.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT370-1 and SOT362-1	SOT1134-1	
$\overline{1OE}, 2\overline{OE}$	1, 24	A30, A13	output enable input (active LOW)
GND	4, 10, 15, 21, 28, 34, 39, 45	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)
V _{CC}	7, 18, 31, 42	A1, A10, A17, A26	supply voltage
1Q0 to 1Q7	2, 3, 5, 6, 8, 9, 11, 12	B20, A31, D5, D1, A2, B2, B3, A5	data output
2Q0 to 2Q7	13, 14, 16, 17, 19, 20, 22, 23	A6, B5, B6, A9, D2, D6, A12, B8	data output
1D0 to 1D7	47, 46, 44, 43, 41, 40, 38, 37	B18, A28, D8, D4, A25, B16, B15, A22	data input
2D0 to 2D7	36, 35, 33, 32, 30, 29, 27, 26	A21, B13, B12, A18, D3, D7, A15, B10	data input
1CP, 2CP	48, 25	A29, A14	clock input

6. Functional description

Table 3. Function selection^[1]

Operating mode	Input			Internal flip-flop	Output nQ0 to nQ7
	\overline{nOE}	nCP	nDn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition;
 ↑ = LOW-to-HIGH transition;
 Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	output HIGH-or LOW-state	[2] -0.5	V _{CC} + 0.5	V
		output 3-state	[2] -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		(T)SSOP48 package	[3] -	500	mW
		HXQFN60U package	[4] -	1000	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
- [2] The output voltage ratings may be exceeded if the output current ratings are observed.
- [3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
- [4] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	active mode	0	-	V _{CC}	V
		power-down mode; V _{CC} = 0 V	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	V _{CC}	-	-	V _{CC}	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	GND	-	GND	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 2.7 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	-	-	V _{CC} - 0.65	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	V _{CC} - 0.6	-	-	V _{CC} - 0.75	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	V _{CC} - 0.8	-	-	V _{CC} - 1.0	-	V

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ ^[1]	Max	Min	Max		
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA; V _{CC} = 2.7 V to 3.6 V	-	-	0.2	-	0.3	V	
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V	
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V	
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	[2]	-	±0.1	±5	-	±20	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND;	[2]	-	±0.1	±5	-	±20	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	μA	
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	20	-	80	μA	
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	[3]	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF	
I _{BHL}	bus hold LOW current	V _{CC} = 3.0 V; V _I = 0.8 V	[4][5]	75	-	-	60	-	μA
I _{BHH}	bus hold HIGH current	V _{CC} = 3.0 V; V _I = 2.0 V	[4][5]	-75	-	-	-60	-	μA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V	[4][6]	500	-	-	500	-	μA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V	[4][6]	-500	-	-	-500	-	μA

- [1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
- [2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input pin.
- [3] For non bus hold parts only (74LVC16374A).
- [4] Valid for data inputs only. Control inputs do not have a bus hold circuit.
- [5] The specified sustaining current at the data input holds the input below the specified V_I level.
- [6] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

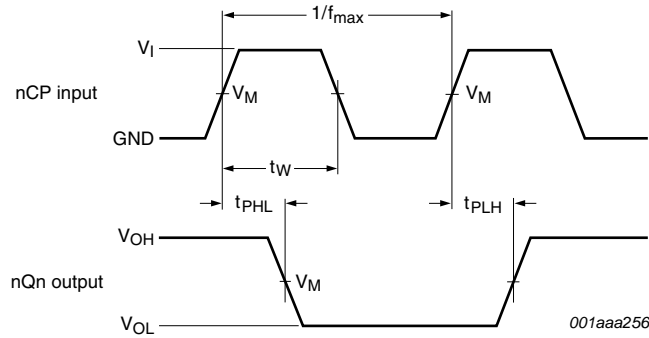
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nCP to nQn; see Figure 7 ^[2]						
		V _{CC} = 1.2 V	-	14	-	-	-	ns
		V _{CC} = 2.7 V	1.5	-	6.0	1.5	7.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.4	5.4	1.5	7.0	ns
t _{en}	enable time	nOE to nQn; see Figure 9 ^[2]						
		V _{CC} = 1.2 V	-	20	-	-	-	ns
		V _{CC} = 2.7 V	1.5	-	6.0	1.5	7.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.5	5.2	1.0	6.5	ns
t _{dis}	disable time	nOE to nQn; see Figure 7 ^[2]						
		V _{CC} = 1.2 V	-	12	-	-	-	ns
		V _{CC} = 2.7 V	1.5	-	5.1	1.5	6.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.9	4.9	1.5	6.5	ns
t _w	pulse width	nCP HIGH; see Figure 7						
		V _{CC} = 1.2 V	-	-	-	-	-	ns
		V _{CC} = 2.7 V	3.0	-	-	3.0	-	ns
		V _{CC} = 3.0 V to 3.6 V	3.0	1.5	-	3.0	-	ns
t _{su}	set-up time	nDn to nCP; see Figure 8						
		V _{CC} = 1.2 V	-	-	-	-	-	ns
		V _{CC} = 2.7 V	1.9	-	-	1.9	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.9	0.3	-	1.9	-	ns
t _h	hold time	nDn to nCP; see Figure 8						
		V _{CC} = 1.2 V	-	-	-	-	-	ns
		V _{CC} = 2.7 V	1.1	-	-	1.1	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	-0.3	-	1.5	-	ns
f _{max}	maximum frequency	see Figure 7						
		V _{CC} = 2.7 V	80	-	-	80	-	MHz
		V _{CC} = 3.0 V to 3.6 V	100	150	-	100	-	MHz
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V ^[3]	-	-	1.0	-	1.5	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
 t_{en} is the same as t_{PZL} and t_{PZH}.
 t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

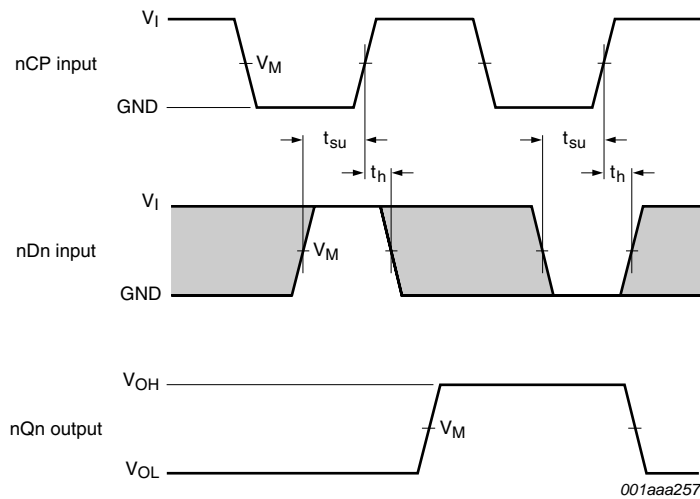
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 7. Clock (nCP) to output (nQn) propagation delays, clock pulse width, and the maximum frequency

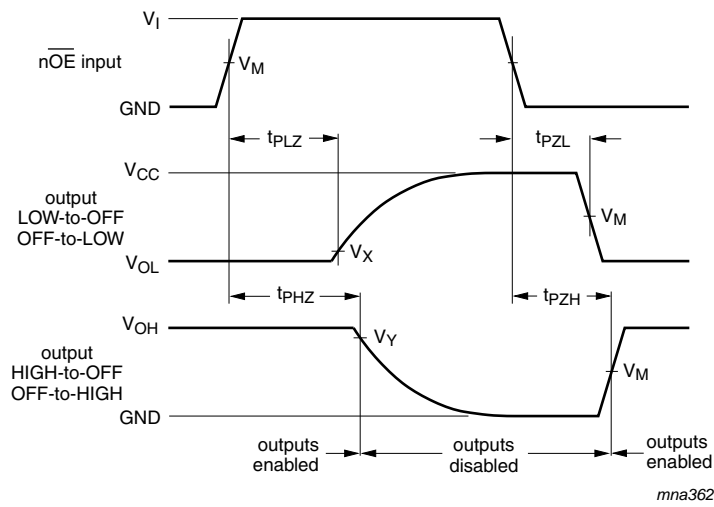


Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable performance.

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 8. Data set-up and hold times for the nDn input to the nCP input



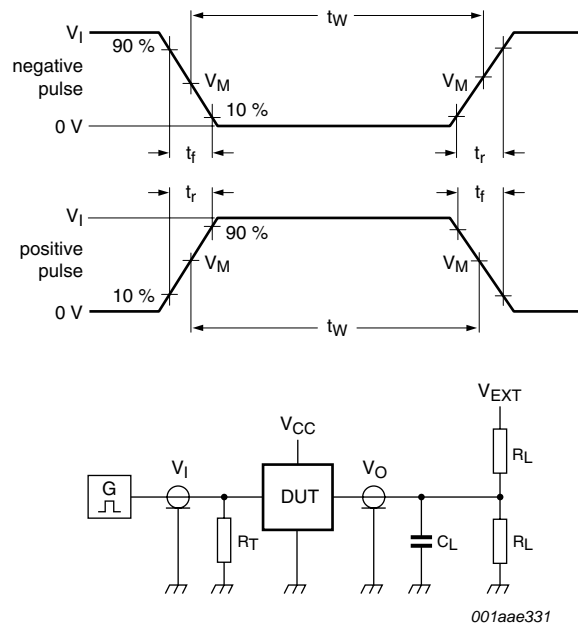
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 9. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1 \text{ V}$	$V_{OH} - 0.1 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω [1]	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

[1] The circuit performs better when $R_L = 1$ k Ω .

12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

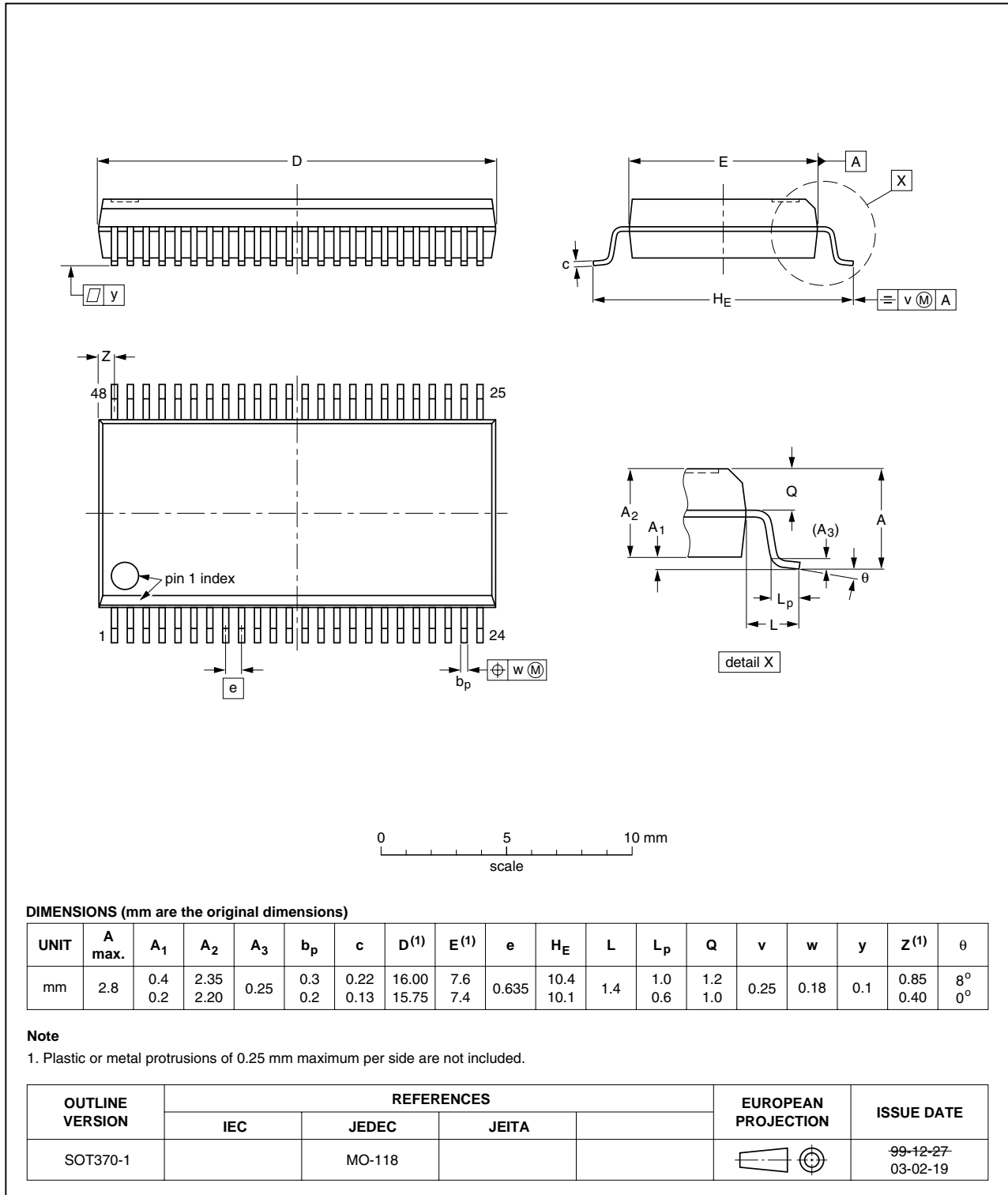


Fig 11. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

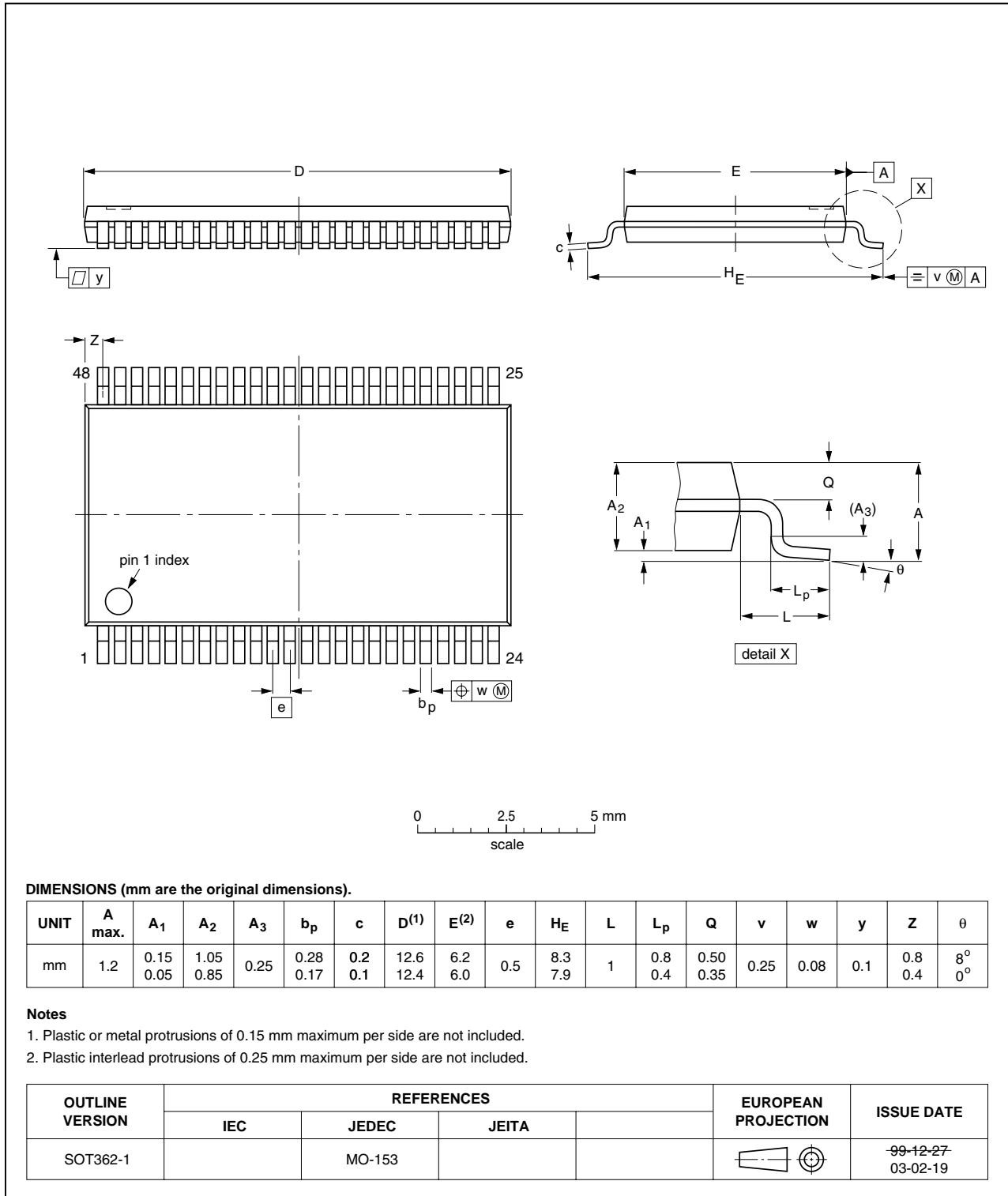


Fig 12. Package outline SOT362-1 (TSSOP48)

HXQFN60U: plastic thermal enhanced extremely thin quad flat package; no leads;
60 terminals; UTLP based; body 4 x 6 x 0.5 mm

SOT1134-1

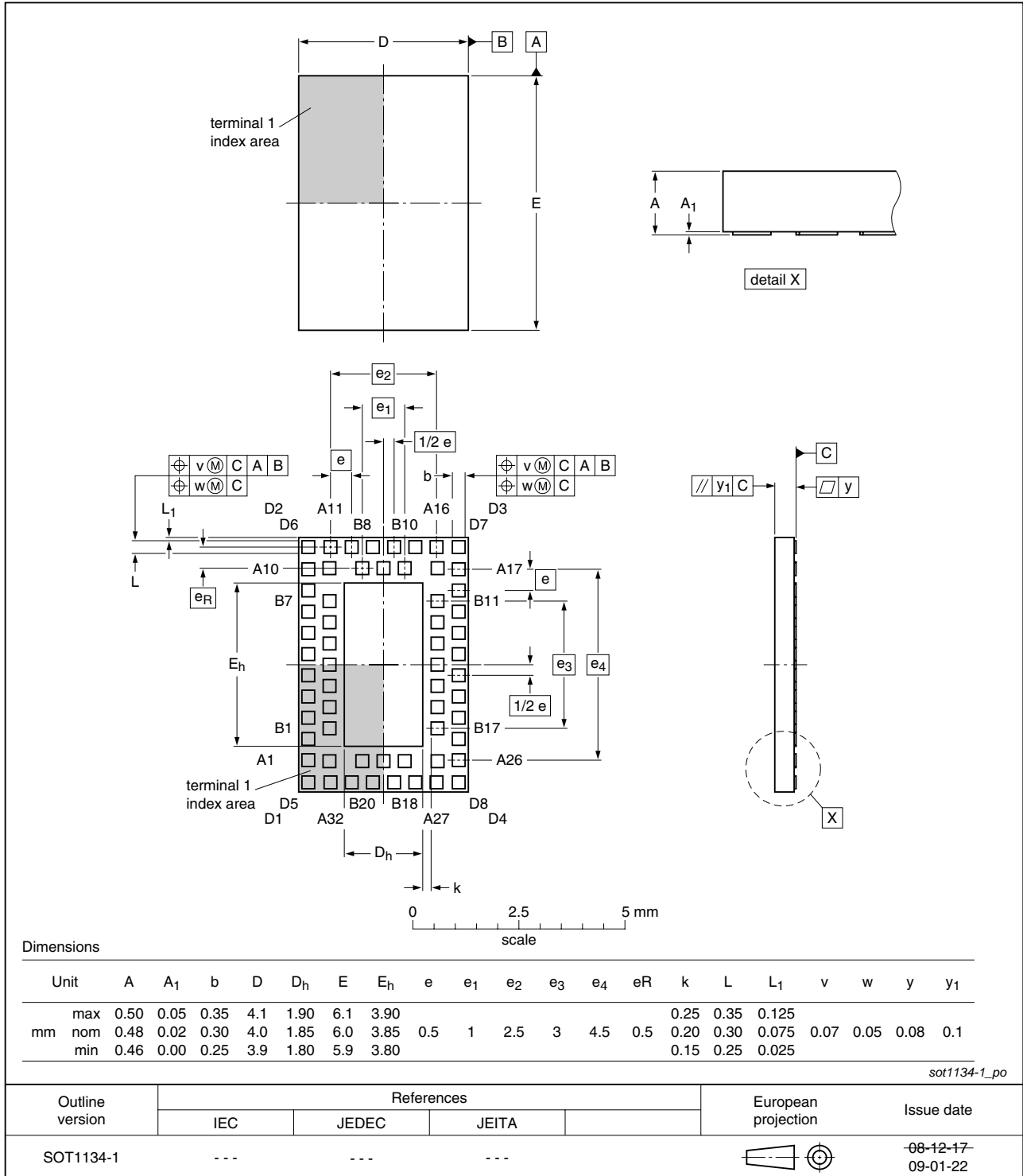


Fig 13. Package outline SOT1134-1 (HXQFN60U)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16374A_7	20100323	Product data sheet	-	74LVC_LVCH16374A_6
Modifications:	<ul style="list-style-type: none"> 74LVC16374ABQ and 74LVCH16374ABQ changed from HUQFN60U (SOT1025-1) to HXQFN60U (SOT1134-1) package. 			
74LVC_LVCH16374A_6	20090212	Product data sheet	-	74LVC_LVCH16374A_5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Added: type numbers 74LVC16374ABQ and 74LVCH16374ABQ (HUQFN60U package). 			
74LVC_LVCH16374A_5	20031212	Product specification	-	74LVC_H16374A_4
74LVC_H16374A_4	19980317	Product specification	-	74LVC16374A_74LVCH16374A_3
74LVC16374A_74LVCH16374A_3	19980317	Product specification	-	74LVC16374A_2
74LVC16374A_2	19970822	Product specification	-	74LVC16374A_1
74LVC16374A_1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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