LC87F6AC8A

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CMOS LSI

8-bit Withstand Voltage Microcontroller

128K-byte Flash ROM / 4096-byte RAM / 100pin

Overview

The LC87F6AC8A is an 8-bit microcontroller that, centered around a CPU running at a minimum bus cycle time of 83.3 ns, integrates on a single chip a number of hardware features such as 128K-byte flash ROM (onboard programmable), 4096-byte RAM, on-chip debugging function, a vacuum fluorescent display (VFD) automatic display controller/driver, a 16-bit timer/counter (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timer/counter or 8-bit PWMs), four 8-bit timers with a prescaler, a 16-bit timer with a prescaler (may be divided into 8-bit timers), a base timer used as a time-of-day clock, a high-speed clock counter, a system clock frequency divider, two synchronous SIO* with automatic transfer capability, an asynchronous/synchronous SIO, two channels of 12-bit PWM modules*, an 8-bit 15-channel AD converter, a small signal detector, and a 27-source 10-vector interrupt feature*.

(* can be supported with the LC876A00 or LC876B00 series by selecting "User Options.")

Features

■Flash ROM
- Capable of onboard programming with a single 5V power supply
- On-chip debugging function
- Block erasable in 128-byte units
- 131072×8 bits

■RAM
- 4096×9 bits

■Minimum bus cycle time
- 83.3s (at 12 MHz) $V_{DD} = 2.8$ to 5.5[V]
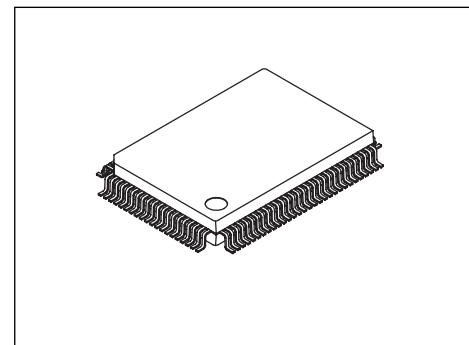- 250ns (at 4 MHz) $V_{DD} = 2.5$ to 5.5[V]
  Note: The bus cycle time refers to the ROM read speed.

■Minimum instruction cycle time (Tcyc)
- 249.9ns (at 12 MHz) $V_{DD} = 2.8$ to 5.5[V]
- 750ns (at 4 MHz) $V_{DD} = 2.5$ to 5.5[V]

■Package form
- QIP100E (lead/Halogen free type)

QIP100E(14X20)

ORDERING INFORMATION

See detailed ordering and shipping information on page 34 of this data sheet.

■Ports
- Normal withstand voltage I/O ports

User Option Selection	Ports Whose Input/Output Can Be Specified in 1-bit Units
For LC876A00 series	32 (P1n, P70 to P73, P8n, P30 to P37, PAn)
For LC876B00 series	32 (P1n, P70 to P73, P8n, P32 to P35, SI2Pn, PAn)

    Port that can also be used for oscillation   1 (XT2)
- 12V max. withstand voltage I/O ports

    Ports whose input/output can be specified in 4-bit units   8 (P0n)
    (in 1- bit units when configured for N-channel open drain output)
- Normal withstand voltage input-only port (also used for oscillation)   1 (XT1)
- Vacuum fluorescent display (VFD) driver ports

    Large current outputs for digits   9 (S0/T0 to S8/T8)
    Large current outputs for digits/segments   7 (S9/T9 to S15/T15)
    Outputs for digits/segments   8 (S16 to S23)
    Outputs for segments   24 (S24 to S47)

Multiplexed pin function
    I/O ports   8 (PFn)
    Input ports   24 (PCn, PDn, PEn)
- Dedicated oscillator pins   2 (CF1, CF2)
- Reset pin   1 ($\overline{\text{RES}}$)
- Power pins   6 ($V_{SS}1$ to $V_{SS}2$, $V_{DD}1$ to $V_{DD}4$)
- Dedicated vacuum fluorescent display driver power pin   1 (VP)

■VFD automatic display controller
  <1> Programmable segment/digit output patterns
    Waveform output can be switched between segment and digit output. (number of pins available for digit waveform output: 9 to 24)
    Capable of driving large current VFDs in parallel
  <2> Provides 16-step dimmer function

■Small signal detection (microphone signals, etc.)
  <1> Counts pulses with amplitudes greater than a preset level
  <2> 2-bit counter

■Timers
- Timer 0: 16-bit timer/counter with two capture registers
    Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
    Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
    Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
    Mode 3: 16-bit counter (with two 16-bit capture registers)
- Timer 1: 16-bit timer/counter with PWM/toggle output capability
    Mode 0: 8-bit timer with an 8-bit prescaler (with toggle output) + 8-bit timer/counter with an 8-bit prescaler (with toggle output)
    Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
    Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle output) (toggle output also possible from the low-order 8 bits)
    Mode 3: 16-bit timer with an 8-bit prescaler (with toggle output) (The low-order 8 bits can be used as PWM.)

- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 8: 16-bit timer
    - Mode 0: 8-bit timer with an 8-bit prescaler $\times$ 2 channels
    - Mode 1: 16-bit timer with an 8-bit prescaler

*Timer 8 is not supported by emulator. An on-chip debugger must be used to develop software for timer 8.

- Base timer
    - <1> The clock can be selected from among the subclock (32.768kHz crystal oscillator), system clock, and timer 0 prescaler output.
    - <2> Interrupts are programmable in 5 different time schemes.

■High-speed clock counter
- <1> Capable of counting clocks with a maximum clock rate of 20MHz (when 10MHz main clock is used)
- <2> Real-time output

■Serial interface
- SIO0: 8-bit synchronous serial interface
    - <1> LSB first/MSB first is selectable.
    - <2> Built-in 8-bit baudrate generator (maximum transfer clock cycle: 4/3 tCYC)
    - <3> Automatic continuous data communication (1 to 256 bits, selectable in 1-bit units) (suspension and resumption of data transfer controllable in byte units)

- SIO1: 8-bit asynchronous/synchronous serial interface
    - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clock)
    - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrate)
    - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clock)
    - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

- SIO2: 8-bit synchronous serial interface *Available in LC876B00 series compatible configuration
    - <1> LSB first
    - <2> Built-in 8-bit baudrate generator (maximum transfer clock cycle: 4/3 tCYC)
    - <3> Automatic continuous data communication (1 to 32 bytes, selectable in byte units)

■ADC: 8 bits $\times$ 15 channels
- Reference voltage can be selected from the $V_{DD}1$ or $V_{DD}2$ pin.

■PWM *Available in LC876A00 series compatible configuration
- Multifrequency 12-bit PWM $\times$ 2 channels

■Remote control receiver circuit (multiplexed with the P73/INT3/T0IN pin)
- <1> Noise rejection function (noise filter time constant selectable from 1/32/128 tCYC)

■Watchdog timer
- <1>External RC watchdog timer
- <2>Interrupt and reset signals selectable

■Interrupts: 27 sources, 10 vector addresses (LC876A00 compatible)

26 sources, 10 vector addresses (LC876B00 compatible)

<1> Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.

<2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address is given priority.

* <u>LC876A00 series compatible configuration</u>

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2 / T0L / INT4
4	0001BH	H or L	INT3 / base timer / INT5
5	00023H	H or L	T0H / INT6
6	0002BH	H or L	T1L / T1H / INT7
7	00033H	H or L	SIO0 / T8L / T8H
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC / MIC / T6 / T7 / PWM4 / PWM5
10	0004BH	H or L	VFD / port 0 / T4 / T5

* <u>LC876B00 series compatible configuration</u>

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2 / T0L / INT4
4	0001BH	H or L	INT3 / base timer / INT5
5	00023H	H or L	T0H / INT6
6	0002BH	H or L	T1L / T1H / INT7
7	00033H	H or L	SIO0 / T8L / T8H
8	0003BH	H or L	SIO1 / SIO2
9	00043H	H or L	ADC / MIC / T6 / T7
10	0004BH	H or L	VFD / port 0 / T4 / T5

• Priority levels X > H > L

• When interrupts of the same level occur at the same time, the interrupt with the smallest vector address is given priority.

■Subroutine stack levels: Up to 2048 levels (The stack is allocated in RAM.)

■High-speed multiplication division instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillator circuits
- RC oscillator circuit (internal)   : For system clock
- CF oscillator circuit   : For system clock with internal Rf
- Crystal oscillator circuit   : For low-speed system clock with external Rd and Rf
- Multifrequency oscillator circuit (internal)   : For system clock

■System clock divider function
- Capable of run
  The minimum instruction cycle time can be selected from among 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).ning on low current.

■Clock output function
  <1> Capable of generating 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source clock that is selected as the system clock.
  <2> Capable of generating the source clock for the subclock.

■Standby function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation. (The VFD display function and part of the serial transfer functions are disabled.)
  <1> Oscillation is not halted automatically.
  <2> Released by system reset or occurrence of an interrupt.

- HOLD mode: Suspends instruction execution and operation of the peripheral circuits.
  <1> The CF oscillator, RC oscillator, crystal oscillator, and multifrequency RC oscillator automatically stop operation.
  <2> There are three ways of releasing HOLD mode:
    1) Setting the reset pin to a low level
    2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    3) Establishing an interrupt source at port 0

- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  <1> The CF oscillator, RC oscillator, and multifrequency RC oscillator automatically stop operation.
  <2> The crystal oscillator retains the state when X'tal HOLD mode is entered.
  <3> There are four ways of releasing X'tal HOLD mode:
    1) Setting the reset pin to a low level
    2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    3) Establishing an interrupt source at port 0
    4) Establishing an interrupt source in the base timer circuit

■On-chip debugger function
- Supports software debugging with the microcontroller mounted on the target device

■Development tools
- Evaluation chip: LC87EV690
- Flash ROM programming board: W87FQ100

User Option Selection	Emulator
LC876A00 series compatible	EVA62S + ECB876600D + SUB876A00 + POD100QFP
	ICE-B877300 + SUB876A00 + POD100QFP
LC876B00 series compatible	EVA62S + ECB876600D + SUB876B00 + POD100QFP
	ICE-B877300 + SUB876B00 + POD100QFP

■Same package and pin assignment as mask ROM version
- The LC87F6AC8A allows the user to specify the optional functions of the LC876A00 or LC876B00 series microcontrollers in the form of flash ROM data (note, however, that pins S32 to S47 are not provided with an internal pull-down resistor). This makes it possible to conduct sample tests using the production model circuit board.
- When a program that is designed for the mask ROM version is applied to the LC87F6AC8A, the size of ROM and RAM that can be used is the same as that of the mask ROM version of the microcontrtoller.
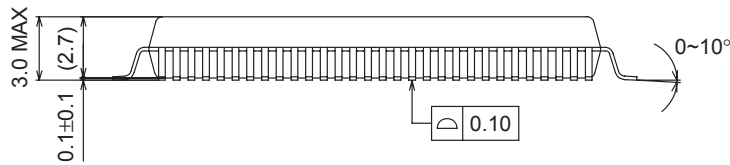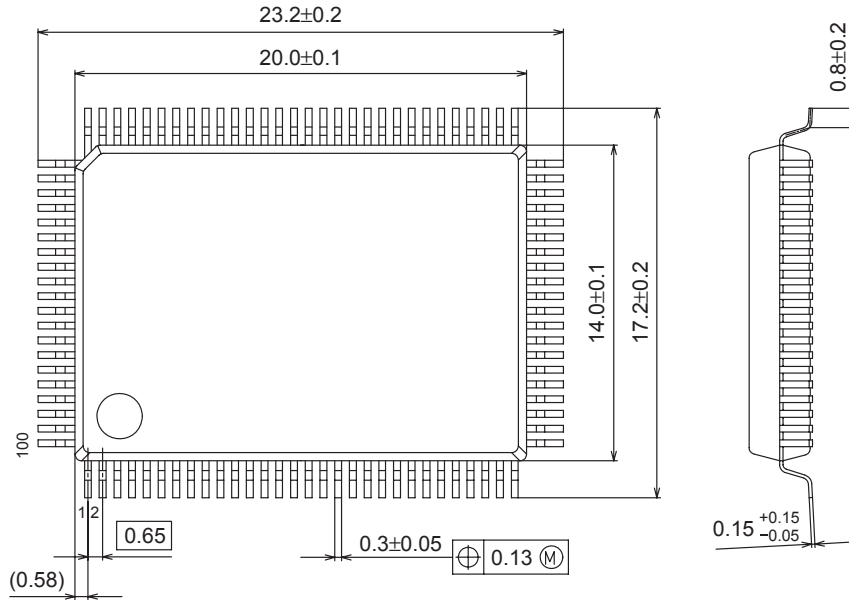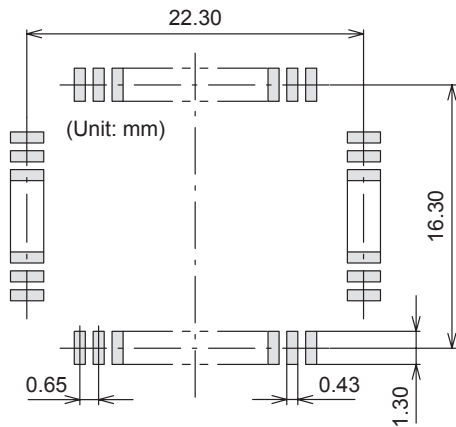
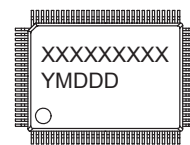## Package Dimensions

unit : mm

PQFP100 14x20 / QIP100E
CASE 122BV
ISSUE A

23.2±0.2

20.0±0.1

0.8±0.2

14.0±0.1

17.2±0.2

100

1 2

0.65

(0.58)

0.3±0.05

⊕ | 0.13 Ⓜ

0.15 $^{+0.15}_{-0.05}$

3.0 MAX

(2.7)

0.1±0.1

0~10°

△ | 0.10

SOLDERING FOOTPRINT*
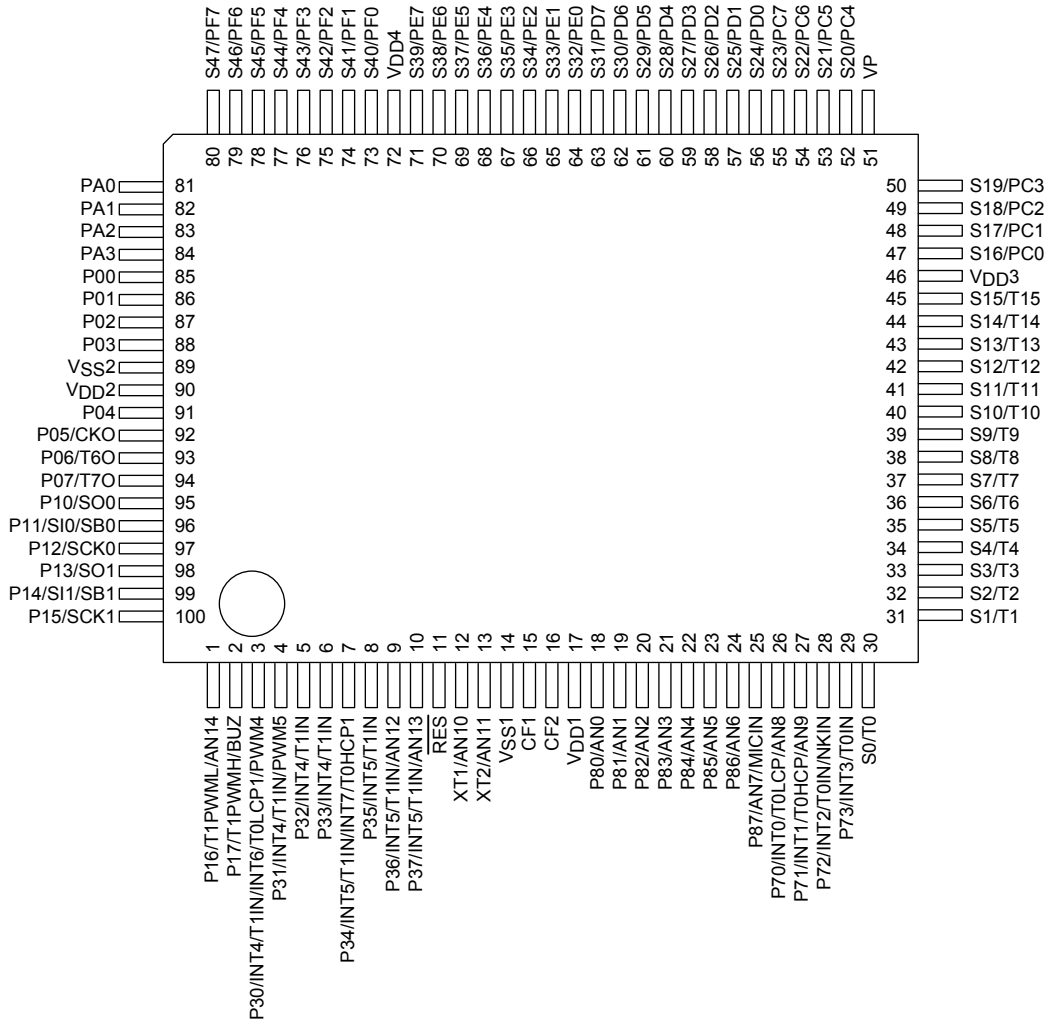
22.30

(Unit: mm)

16.30

0.65

0.43

1.30

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering
 details, please download the ON Semiconductor Soldering and
 Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***

XXXXXXXXX
YMDDD

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to
 device data sheet for actual part marking.
 Pb−Free indicator, "G" or microdot "■",
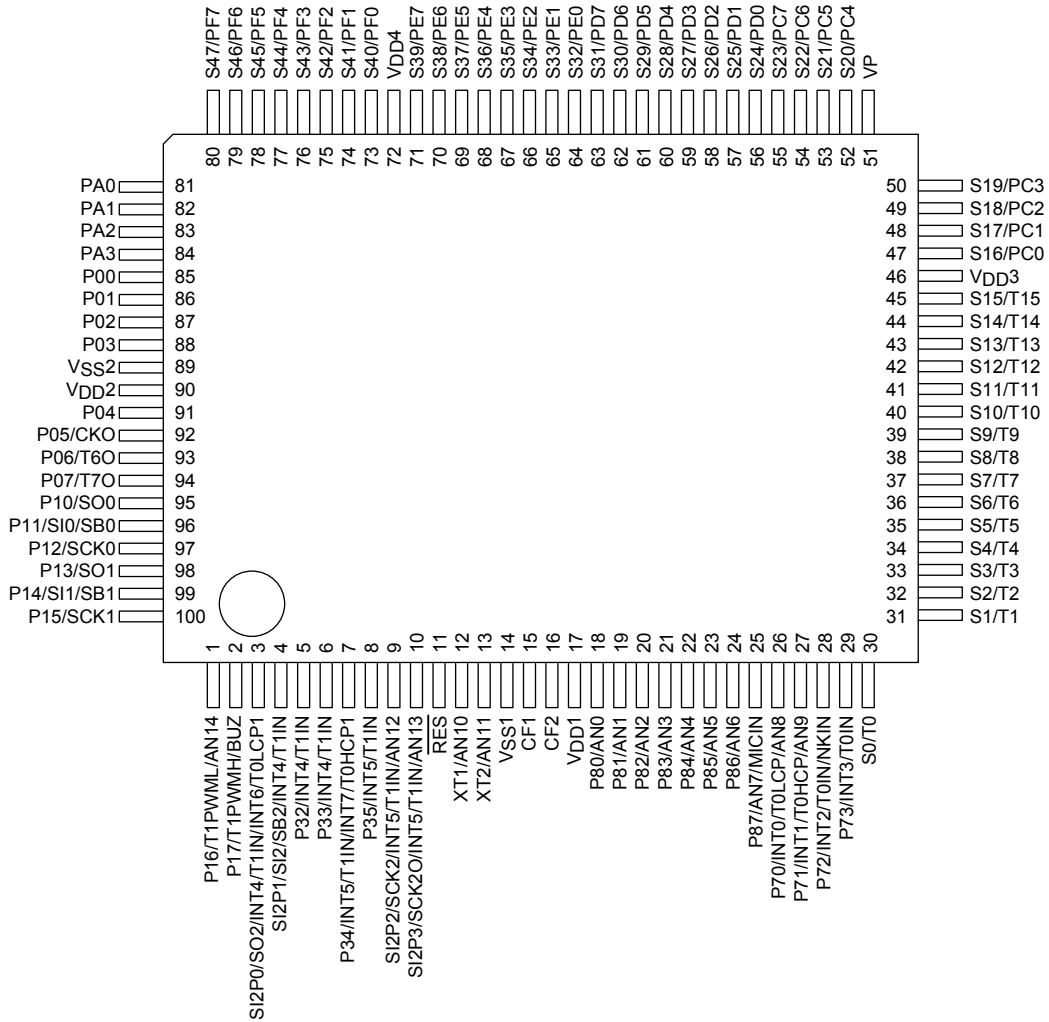 may or may not be present.

LC87F6AC8A

Pin Assignment　* <u>LC876A00 series compatible configuration</u>

Top pins (80–51, left to right):

S47/PF7 (80), S46/PF6 (79), S45/PF5 (78), S44/PF4 (77), S43/PF3 (76), S42/PF2 (75), S41/PF1 (74), S40/PF0 (73), VDD4 (72), S39/PE7 (71), S38/PE6 (70), S37/PE5 (69), S36/PE4 (68), S35/PE3 (67), S34/PE2 (66), S33/PE1 (65), S32/PE0 (64), S31/PD7 (63), S30/PD6 (62), S29/PD5 (61), S28/PD4 (60), S27/PD3 (59), S26/PD2 (58), S25/PD1 (57), S24/PD0 (56), S23/PC7 (55), S22/PC6 (54), S21/PC5 (53), S20/PC4 (52), VP (51)

Left pins (81–100, top to bottom):

PA0 (81), PA1 (82), PA2 (83), PA3 (84), P00 (85), P01 (86), P02 (87), P03 (88), VSS2 (89), VDD2 (90), P04 (91), P05/CKO (92), P06/T6O (93), P07/T7O (94), P10/SO0 (95), P11/SI0/SB0 (96), P12/SCK0 (97), P13/SO1 (98), P14/SI1/SB1 (99), P15/SCK1 (100)

Right pins (50–31, top to bottom):

S19/PC3 (50), S18/PC2 (49), S17/PC1 (48), S16/PC0 (47), VDD3 (46), S15/T15 (45), S14/T14 (44), S13/T13 (43), S12/T12 (42), S11/T11 (41), S10/T10 (40), S9/T9 (39), S8/T8 (38), S7/T7 (37), S6/T6 (36), S5/T5 (35), S4/T4 (34), S3/T3 (33), S2/T2 (32), S1/T1 (31)

Bottom pins (1–30, left to right):

P16/T1PWML/AN14 (1), P17/T1PWMH/BUZ (2), P30/INT4/T1IN/INT6/T0LCP1/PWM4 (3), P31/INT4/T1IN/PWM5 (4), P32/INT4/T1IN (5), P33/INT4/T1IN (6), P34/INT5/T1IN/INT7/T0HCP1 (7), P35/INT5/T1IN (8), P36/INT5/T1IN/AN12 (9), P37/INT5/T1IN/AN13 (10), RES (11), XT1/AN10 (12), XT2/AN11 (13), VSS1 (14), CF1 (15), CF2 (16), VDD1 (17), P80/AN0 (18), P81/AN1 (19), P82/AN2 (20), P83/AN3 (21), P84/AN4 (22), P85/AN5 (23), P86/AN6 (24), P87/AN7/MICIN (25), P70/INT0/T0LCP/AN8 (26), P71/INT1/T0HCP/AN9 (27), P72/INT2/T0IN/NKIN (28), P73/INT3/T0IN (29), S0/T0 (30)

QIP100E (lead/Halogen free type)

Pin Assignment * <u>LC876B00 series compatible configuration</u>

Top pins (left to right, 80 to 51):
S47/PF7, S46/PF6, S45/PF5, S44/PF4, S43/PF3, S42/PF2, S41/PF1, S40/PF0, VDD4, S39/PE7, S38/PE6, S37/PE5, S36/PE4, S35/PE3, S34/PE2, S33/PE1, S32/PE0, S31/PD7, S30/PD6, S29/PD5, S28/PD4, S27/PD3, S26/PD2, S25/PD1, S24/PD0, S23/PC7, S22/PC6, S21/PC5, S20/PC4, VP

Left pins (81–100):
- 81 PA0
- 82 PA1
- 83 PA2
- 84 PA3
- 85 P00
- 86 P01
- 87 P02
- 88 P03
- 89 V$_{SS}$2
- 90 V$_{DD}$2
- 91 P04
- 92 P05/CKO
- 93 P06/T6O
- 94 P07/T7O
- 95 P10/SO0
- 96 P11/SI0/SB0
- 97 P12/SCK0
- 98 P13/SO1
- 99 P14/SI1/SB1
- 100 P15/SCK1

Right pins (50–31):
- 50 S19/PC3
- 49 S18/PC2
- 48 S17/PC1
- 47 S16/PC0
- 46 VDD3
- 45 S15/T15
- 44 S14/T14
- 43 S13/T13
- 42 S12/T12
- 41 S11/T11
- 40 S10/T10
- 39 S9/T9
- 38 S8/T8
- 37 S7/T7
- 36 S6/T6
- 35 S5/T5
- 34 S4/T4
- 33 S3/T3
- 32 S2/T2
- 31 S1/T1

Bottom pins (left to right, 1 to 30):
- 1 P16/T1PWML/AN14
- 2 P17/T1PWMH/BUZ
- 3 SI2P0/SO2/INT4/T1IN/INT6/T0LCP1
- 4 SI2P1/SI2/SB2/INT4/T1IN
- 5 P32/INT4/T1IN
- 6 P33/INT4/T1IN
- 7 P34/INT5/T1IN/INT7/T0HCP1
- 8 P35/INT5/T1IN
- 9 SI2P2/SCK2/INT5/T1IN/AN12
- 10 SI2P3/SCK2O/INT5/T1IN/AN13
- 11 RES
- 12 XT1/AN10
- 13 XT2/AN11
- 14 VSS1
- 15 CF1
- 16 CF2
- 17 VDD1
- 18 P80/AN0
- 19 P81/AN1
- 20 P82/AN2
- 21 P83/AN3
- 22 P84/AN4
- 23 P85/AN5
- 24 P86/AN6
- 25 P87/AN7/MICIN
- 26 P70/INT0/T0LCP/AN8
- 27 P71/INT1/T0HCP/AN9
- 28 P72/INT2/T0IN/NKIN
- 29 P73/INT3/T0IN
- 30 S0/T0

QIP100E (lead/Halogen free type)

System Block Diagram * <u>LC876A00 series compatible configuration</u>

System Block Diagram * LC876B00 series compatible configuration

Pin Description

* Common to <u>LC876A00 and LC876B00 compatible series</u>

Pin Name	I/O	Description	Option
$V_{SS}1$, $V_{SS}2$	–	– power supply pin	No
$V_{DD}1$, $V_{DD}2$ $V_{DD}3$, $V_{DD}4$	–	+ power supply pin	No
VP	–	– VFD power supply pin	No

Port 0 P00 to P07	I/O	• 8-bit input/output port
		• Input/output can be specified in 4-bit units.
		• Pull-up registers can be turned on and off in 4-bit units.
		• HOLD release input
		• Port 0 interrupt input
		• 12V maximum withstand voltage in N-channel open drain output mode
		• Multiplexed pin functions
		   P05: Clock output (system clock/subclock selectable)
		   P06: Timer 6 toggle output
		   P07: Timer 7 toggle output
			Yes

Port 1 P10 to P17	I/O	• 8-bit input/output port
		• Input/output can be specified in 1-bit units.
		• Pull-up registers can be turned on and off in 1-bit units.
		• Multiplexed pin functions
		   P10: SIO0 data output
		   P11: SIO0 data input / bus input/output
		   P12: SIO0 clock input/output
		   P13: SIO1 data output
		   P14: SIO1 data input / bus input/output
		   P15: SIO1 clock input/output
		   P16: Timer 1 PWML output AD converter input port (AN14)
		   P17: Timer 1 PWMH output/buzzer output
			Yes

Port 7 P70 to P73	I/O	• 4-bit input/output port
		• Input/output can be specified in 1-bit units.
		• Pull-up registers can be turned on and off in 1-bit units.
		• Multiplexed pin functions
		   P70: INT0 input/HOLD release input/timer 0L capture input/watchdog timer output
		   P71: INT1 input/HOLD release input/timer 0H capture input
		   P72: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input/
		      high-speed clock counter input
		   P73: INT3 input (input with noise filter)/timer 0 event input/timer 0H capture input
		AD converter input port: AN8(P70), AN9(P71)
		• Interrupt acknowledge type
		
		table below
			No

Port 8 P80 to P87	I/O	• 8-bit input/output port
		• Input/output can be specified in 1-bit units.
		• Multiplexed pin functions
		  AD converter input port: AN0 to AN7
		  Small signal detector input port: MICIN (P87)
			No

Interrupt acknowledge type (Port 7):

	Rising	Falling	Falling & Rising	H level	L level
INT0	○	○	×	○	○
INT1	○	○	×	○	○
INT2	○	○	○	×	×
INT3	○	○	○	×	×

Pin Name	I/O	Description	Option
S0/T0 to S8/T8	O	• Large current output for vacuum fluorescent display (VFD) controller digits (also can be used as segment outputs)	No
S9/T9 to S15/T15	O	• Large current output for vacuum fluorescent display (VFD) controller segments/digits	No
S16 to S23	I/O	• Output for vacuum fluorescent display (VFD) controller segments/digits • Multiplexed pin functions High withstand voltage input port: PC0 to PC7	No
S24 to S31	I/O	• Output for vacuum fluorescent display (VFD) controller segments • Multiplexed pin functions High withstand voltage input port: PD0 to PD7	No
S32 to S39	I/O	• Output for vacuum fluorescent display (VFD) controller segments • Multiplexed pin functions High withstand voltage input port: PE0 to PE7	Yes (Not available for flash ROM version)
S40 to S47	I/O	• Output for vacuum fluorescent display (VFD) controller segments • Multiplexed pin functions High withstand voltage input/output port: PF0 to PF7	Yes (Not available for flash ROM version)
Port PA0 to PA3	I/O	• 4-bit input/output port • Input/output can be specified in 1-bit units • Pull-up registers can be turned on and off in 1-bit units. • Multiplexed pin functions On-chip debugger control function: PA01 to PA03	Yes
RES	I	Reset pin	No

XT1	I	• 32.768kHz crystal resonator input pin
		• Multiplexed pin functions
		  General-purpose input port
		  Must be connected to VDD1 when not to be used.
		  AD converter input port: AN10
			No

XT2	I/O	• 32.768kHz crystal resonator output pin
		• Multiplexed pin functions
		  General-purpose input/output port
		  Must be configured for oscillation and held open when not to be used.
		  AD converter input port: AN11
			No

CF1	I	Ceramic resonator input pin	No
CF2	O	Ceramic resonator output pin	No

* <u>LC876A00 series compatible configuration</u>

Pin Name	I/O	Description	Option

Port 3
P30 to P37
	I/O	• 8-bit input/output port
		• Input/output can be specified in 1-bit units.
		• Pull-up registers can be turned on and off in 1-bit units.
		• Multiplexed pin functions
		  P30: PWM4 output/INT6 input
		  P31: PWM5 output
		  P30 to P33: INT4 input/HOLD release input/timer 1 event input/
		        timer 0L capture input/timer 0H capture input
		  P34: INT7 input
		  P34 to P37: INT5 input/HOLD release input/timer 1 event input/
		        timer 0L capture input/timer 0H capture input
		  AD converter input port: AN12 (P36), AN13(P37)
		• Interrupt acknowledge type
		
		(see table below)
			Yes

	Rising	Falling	Falling & Rising	H level	L level
INT4	○	○	○	×	×
INT5	○	○	○	×	×
INT6	○	○	○	×	×
INT7	○	○	○	×	×

* <u>LC876B00 series compatible configuration</u>

Pin Name	I/O	Description	Option

Port 3
P30 to P37
	I/O	• 4-bit input/output port
		• Input/output can be specified in 1-bit units
		• Pull-up registers can be turned on and off in 1-bit units.
		• Multiplexed pin functions
		  P32 to P33: INT4 input/HOLD release input/timer 1 event input/
		        timer 0L capture input/timer 0H capture input
		  P34: INT7 input
		  P34 to P35: INT5 input/HOLD release input/timer 1 event input/
		        timer 0L capture input/timer 0H capture input
		• Interrupt acknowledge type
		
		(see table below)
			Yes

	Rising	Falling	Falling & Rising	H level	L level
INT4	○	○	○	×	×
INT5	○	○	○	×	×
INT6	○	○	○	×	×
INT7	○	○	○	×	×

Pin Name	I/O	Description	Option

SIO2 port
SI2P0 to SI2P3
	I/O	• 4-bit input/output port
		• Input/output can be specified in 1-bit units
		• Multiplexed pin functions
		  SI2P0: SIO2 data output/INT6 input
		  SI2P1: SIO2 data input / bus input/output
		  SI2P2: SIO2 clock input/output
		  SI2P3: SIO2 clock output
		  SI2P0 to SI2P1: INT4 input/HOLD release input/timer1 event input/
		        timer 0L capture input/timer 0H capture input
		  SI2P2 to SI2P3: INT5 input/HOLD release input/timer1 event input/
		        timer 0L capture input/timer 0H capture input
		  AD converter input port: AN12 (SI2P2), AN13(SI2P3)
		• See the table above for Port 3 for the interrupt acknowledge type for SIO2 ports.
			Yes

Port Output Types

The tables below list the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input/output port even if it is in output mode.

* Common to the LC876A00 and LC876B00 compatible series

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor	Pull-down Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)	–
		2	12V withstand voltage N-channel open drain	No	–
P10 to P17	1 bit	1	CMOS	Programmable	–
		2	N-channel open drain	Programmable	–
P70	–	No	N-channel open drain	Programmable	–
P71 to P73	–	No	CMOS	Programmable	–
P80 to P87	–	No	N-channel open drain	No	–
S0/T0 to S15/T15 S16 to S31	–	No	High withstand voltage P-channel open drain	–	Fixed
S32 to S47 (Note 2)	1 bit	1	High withstand voltage P-channel open drain	–	Fixed
		2	High withstand voltage P-channel open drain	–	No
PA0 to PA3	1 bit	1	CMOS	Programmable	–
		2	N-channel open drain	Programmable	–
XT1	–	No	Input only	No	–
XT2	–	No	32.768kHz crystal resonator output (N-channel open drain when selecting general-purpose output port)	No	–

* LC876A00 series compatible configuration

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor	Pull-down Resistor
P30 to P37	1 bit	1	CMOS	Programmable	–
		2	N-channel open drain	Programmable	–

* LC876B00 series compatible configuration

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor	Pull-down Resistor
P32 to P35	1 bit	1	CMOS	Programmable	–
		2	N-channel open drain	Programmable	–
SI2P0 to SI2P3	–	No	CMOS (SI2P1: N-channel open drain when selecting SIO2 data)	No	–

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 is exercised in 4-bit units (P00 to P03, P04 to P07).

Note 2: A built-in internal pull-down resistor can be connected to S32 to S47 in 1-bit units (with a mask option) only for the mask ROM version of product.
The flash ROM version (LC87F6AC8A) does not include the internal pull-down resistor.

*1 Make the following connection to minimize the noise input to the $V_{DD}1$ pin and prolong the backup time. Be sure to electrically short the $V_{SS}1$ and $V_{SS}2$ pins.
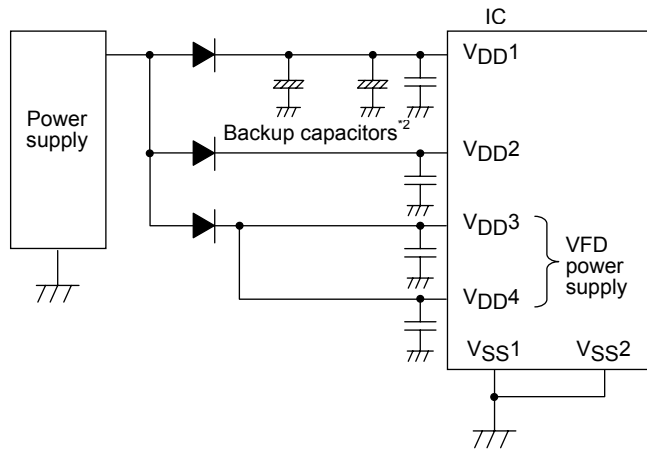
*2 The internal memory is sustained by $V_{DD}1$. If $V_{DD}2$ is not backed up, the high-level output at the ports are unstable in HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time. Make sure that the port outputs are held at a low level in HOLD backup mode.

1. Absolute Maximum Ratings at $Ta = 25°C$, $V_{SS}1 = V_{SS}2 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min.	typ.	max.	unit
Maximum supply voltage		V_{DD} MAX	V_{DD}, $V_{DD}2$, $V_{DD}3$, $V_{DD}4$	$V_{DD}1=V_{DD}2=V_{DD}3$ $=V_{DD}4$		-0.3	to	+6.5	V
Input voltage		$V_I(1)$	•XT1 •CF1 •$\overline{RES}$			-0.3	to	V_{DD}+0.3	
		$V_I(2)$	VP			V_{DD}-45	to	V_{DD}+0.3	
Output voltage		$V_O(1)$	S0/T0 to S15/T15			V_{DD}-45	to	V_{DD}+0.3	
Input/output voltage		$V_{IO}(1)$	•CMOS output P0 •P1, P7, P8, PA •P30 to P37 (LC876A00 compatible) •P32 to P35 / SI2P0 to SI2P3 (LC876B00 compatible) •XT2			-0.3	to	V_{DD}+0.3	
		$V_{IO}(2)$	Open drain output P0			-0.3	to	12	
		$V_{IO}(3)$	S16 to S47			V_{DD}-45	to	V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	•P0, P1, PA •P30 to P37 (LC876A00 compatible) •P32 to P35 / SI2P0 to SI2P3 (LC876B00 compatible)	•CMOS output •Per 1 applicable pin		-10			mA
		IOPH(2)	P71 to P73	Per 1 applicable pin		-3			
		IOPH(3)	S0/T0 to S15/T15	Per 1 applicable pin		-30			
		IOPH(4)	S16 to S47	Per 1 applicable pin		-15			
	Total output current	ΣIOAH(1)	•P00 to P03 •PA	Total current of all applicable pins		-30			
		ΣIOAH(2)	•P04 to P07 •P1 •P30 to P37 (LC876A00 compatible) •P32 to P35 / SI2P0 to SI2P3 (LC876B00 compatible)	Total current of all applicable pins		-30			
		ΣIOAH(3)	P71 to P73	Total current of all applicable pins		-5			
		ΣIOAH(4)	S0/T0 to S15/T15	Total current of all applicable pins		-65			
		ΣIOAH(5)	S16 to S27	Total current of all applicable pins		-60			
		ΣIOAH(6)	S28 to S39	Total current of all applicable pins		-60			
		ΣIOAH(7)	S40 to S47	Total current of all applicable pins		-60			

Continued from preceding page.

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification			unit
						min.	typ.	max.	

Low level output current	Peak output current	IOPL(1)	•P0, P1, PA
			•P30 to P37
			  (LC876A00 compatible)
			•P32 to P35 / SI2P0 to SI2P3
			  (LC876B00 compatible)
				Per 1 applicable pin				20	mA

		IOPL(2)	•P7, P8 •XT2	Per 1 applicable pin				5	
	Total output current	ΣIOAL(1)	•P00 to P03, PA	Total current of all applicable pins				50	

		ΣIOAL(2)	•P04 to P07
			•P1
			•P30 to P37
			  (LC876A00 compatible)
			•P32 to P35 / SI2P0 to SI2P3
			  (LC876B00 compatible)
				Total current of all applicable pins				50	

		ΣIOAL(3)	•P7, P8 •XT2	Total current of all applicable pins				20	
Allowable power dissipation		Pd max	QIP100E	Ta=-20 to +70°C				508	mW
Operating ambient temperature		Topr				-20	to	+70	°C
Storage ambient temperature		Tstg				-55	to	+125	

Note: The applicable pins (SI2Pn or P30, P31, P36, and P37) vary depending on the user options selected.
 Check the pin assignment diagram of the selected product type (LC876A00 or LC876B00).

2. Allowable Operating Range at Ta = -20 to +70°C, $V_{SS1} = V_{SS2} = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
				V_{DD}[V]	min.	typ.	max.	unit
Operating supply voltage (Note 1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3=V_{DD}4$	0.250μs ≤ tCYC ≤ 200μs		2.8		5.5	V
	$V_{DD}(2)$		0.735μs ≤ tCYC ≤ 200μs		2.5		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	•In HOLD mode •RAM and register contents sustained		2.0		5.5	
Pull-down supply voltage	VP	VP			-35		V_{DD}	
High level input voltage	$V_{IH}(1)$	•CMOS output P0 •P8, PA	Output disabled	2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Open drain output type P0	Output disabled	2.5 to 5.5	$0.3V_{DD}$ +0.7		11	
	$V_{IH}(3)$	•P1 •P30 to P37 (LC876A00 compatible) •P32 to P35 / SI2P0 to SI2P3 (LC876B00 compatible) •P71, 72, 73 •P70 port input/ interrupt side	Output disabled	2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(4)$	S16 to S47	Output P-channel Tr off	2.5 to 5.5	$0.33V_{DD}$ +1.0		V_{DD}	
	$V_{IH}(5)$	•P87 small signal input side	Output disabled	2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
	$V_{IH}(6)$	•P70 watchdog timer side	Output disabled	2.5 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(7)$	•XT1, XT2 •CF1, $\overline{RES}$		2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	•P0, P8, PA	Output disabled	2.5 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
	$V_{IL}(2)$	•P1 •P30 to P37 (LC876A00 compatible) •P32 to P35 / SI2P0 to SI2P3 (LC876B00 compatible) •P71 to P73 •P70 port input/interrupt side	Output disabled	2.5 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
	$V_{IL}(3)$	S16 to S47	Output P-channel Tr off	2.5 to 5.5	-35		$0.2V_{DD}$	
	$V_{IL}(4)$	•P87small signal input side	Output disabled	2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
	$V_{IL}(5)$	•P70 watchdog timer side	Output disabled	2.5 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(6)$	•XT1, XT2 •CF1, $\overline{RES}$		2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 1)	tCYC			3.0 to 5.5	0.250		200	μs
				2.5 to 5.5	0.735		200	

Continued from preceding page.

Parameter	Symbol	Pin/Remarks	Conditions	V$_{DD}$[V]	Specification min.	Specification typ.	Specification max.	unit
External system clock frequency	FEXCF(1)	CF1	•CF2 pin open •System clock frequency division ratio=1/1 •External system clock duty= 50±5%	2.8 to 5.5	0.1		12	MHz
				2.5 to 5.5	0.1		4	
			•CF2 pin open •System clock frequency division ratio=1/2 •External system clock duty= 50±5%	2.8 to 5.5	0.2		24	
				2.5 to 5.5	0.2		8	
Oscillation frequency range (Note 2)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation mode See Fig. 1.	2.8 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	4MHz ceramic oscillation mode See Fig. 1.	2.5 to 5.5		4		
	FmRC		Internal RC oscillation	2.5 to 5.5	0.3	1.0	2.0	
	FmMRC		Multifrequency RC oscillator source oscillation	2.5 to 5.5		18		
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation mode See Fig. 2.	2.5 to 5.5		32.768		kHz

Note 1: Onboard programming is possible when V$_{DD}$≥4.5[V].

Note 2: See Table 1 and Table 2 for the oscillation constant.

3. Electrical Characteristics at Ta = -20 to +70°C, $V_{SS1} = V_{SS2} = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min.	typ.	max.	unit
High level input current	$I_{IH}(1)$	Open drain output type P0	•Output disabled •V_{IN}=11V (including output TR's off leakage current)	2.5 to 5.5			5	μA
	$I_{IH}(2)$	•P0, P1, P7, P8, PA •P30 to P37 (LC876A00 compatible) •P32 to P35, SI2P0 to SI2P3 (LC876B00 compatible)	•Output disabled •Pull-up resistor off •V_{IN}=V_{DD} (including output TR's off leakage current)	2.5 to 5.5			1	
	$I_{IH}(3)$	S16 to S47 (PC, PD, PE, PF)	•In input port mode •V_{IN}=V_{DD}	2.5 to 5.5			60	
	$I_{IH}(4)$	$\overline{RES}$	V_{IN}=V_{DD}	2.5 to 5.5			1	
	$I_{IH}(5)$	XT1, XT2	•In input port mode •V_{IN}=V_{DD}	2.5 to 5.5			1	
	$I_{IH}(6)$	CF1	V_{IN}=V_{DD}	2.5 to 5.5			15	
	$I_{IH}(7)$	P87/AN7/MICIN small signal input side	V_{IN}=VBIS+0.5V (VBIS is a bias voltage.)	4.5 to 5.5	4.2	8.5	15	
				2.5 to 4.5	1.5	5.5	10	
Low level input current	$I_{IL}(1)$	•P0, P1, P7, P8, PA •P30 to P37 (LC876A00 compatible) •P32 to P35, SI2P0 to SI2P3 (LC876B00 compatible)	•Output disabled •Pull-up resistor off •V_{IN}=V_{SS} (including output TR's off leakage current)	2.5 to 5.5	-1			
	$I_{IL}(2)$	$\overline{RES}$	V_{IN}=V_{SS}	2.5 to 5.5	-1			
	$I_{IL}(3)$	XT1, XT2	•In input port mode •V_{IN}=V_{SS}	2.5 to 5.5	-1			
	$I_{IL}(4)$	CF1	V_{IN}=V_{SS}	2.5 to 5.5	-15			
	$I_{IL}(5)$	P87/AN7/MICIN small signal input side	V_{IN}=VBIS-0.5V (VBIS is a bias voltage.)	4.5 to 5.5	-15	-8.5	-4.2	
				2.5 to 4.5	-10	-5.5	-1.5	
High level output voltage	$V_{OH}(1)$	•CMOS output type P0 •P1 •P30 to P37 (LC876A00 compatible) •PWM4, PWM5 (LC876A00 compatible) •P32 to P35, SI2P0 to SI2P3 (LC876B00 compatible)	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.5mA	3.0 to 5.5	V_{DD}-1			
	$V_{OH}(3)$		I_{OH}=-0.1mA	2.5 to 5.5	V_{DD}-0.5			
	$V_{OH}(4)$	P71 to P73	I_{OH}=-0.4mA	2.5 to 5.5	V_{DD}-1			
	$V_{OH}(5)$	S0/T0 to S15/T15	I_{OH}=-20mA	4.5 to 5.5	V_{DD}-1.8			
	$V_{OH}(6)$		I_{OH}=-10mA	3.0 to 5.5	V_{DD}-1.8			
	$V_{OH}(7)$		•I_{OH}=-1.0mA •When per pin I_{OH} of all pins is 1mA or less	2.5 to 5.5	V_{DD}-1			
	$V_{OH}(8)$	S16 to S47	I_{OH}=-5.0mA	4.5 to 5.5	V_{DD}-1.8			
	$V_{OH}(9)$		I_{OH}=-2.5mA	3.0 to 5.5	V_{DD}-1.8			
	$V_{OH}(10)$		•I_{OH}=-1.0mA •When per pin I_{OH} of all pins is 1mA or less	2.5 to 5.5	V_{DD}-1			

Continued from preceding page.

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	unit
Low level output voltage	V_{OL}(1)	•P0, P1, PA •P30 to P37 (LC876A00 compatible)	I_{OL}=10mA	4.5 to 5.5			1.5	V
	V_{OL}(2)		I_{OL}=5mA	3.0 to 5.5			1.5	
	V_{OL}(3)	•P32 to P35, SI2P0 to SI2P3 (LC876B00 compatible)	I_{OL}=1.6mA	2.5 to 5.5			0.4	
	V_{OL}(4)	•P30 to P31 (LC876A00 compatible: when PWM4/5 is used)	I_{OL}=1.0mA	4.5 to 5.5			1.0	
	V_{OL}(5)		I_{OL}=0.5mA	3.0 to 5.5			1.0	
	V_{OL}(6)		I_{OL}=0.1mA	2.5 to 5.5			0.5	
	V_{OL}(7)	• Ports 7, 8 •XT2	I_{OL}=1mA	2.5 to 5.5			0.4	
Pull-up MOS-Tr resistance	Rpu	Ports 0, 1, 7, A •P30 to P37 (LC876A00 compatible) •P32 to P35 (LC876B00 compatible)	V_{OH}=0.9V_{DD}	4.5 to 5.5	15	40	70	kΩ
				2.5 to 4.5	25	70	150	
Output off leakage current	IOFF (1)	•S0/T0 to S15/T15 •S16 to S47	•Output P-channel Tr off •V_{OUT}=V_{SS}	2.5 to 5.5	-1			µA
	IOFF (2)		•Output P-channel Tr off •V_{OUT}=V_{DD}-40V	2.5 to 5.5	-30			
High withstand voltage input pin L level hold Tr.	Rinpd	S16 to S47	Output P-channel Tr off	2.5 to 5.5		200		kΩ
High withstand voltage pull-down resistance	Rpd	Pull-down resistor present •S0/T0 to S15/T15 •S16 to S47	•Output P-channel Tr off •V_{OUT}=3V •Vp=-30V	5.0	60	100	200	
Hysteresis voltage	VHIS(1)	•P1, P3, P7 •P30 to P37 (LC876A00 compatible) •P32 to P35, SI2P0 to SI2P3 (LC876B00 compatible) •$\overline{RES}$		2.5 to 5.5		0.1V_{DD}		V
	VHIS(2)	•P87 small signal input side		2.5 to 5.5		0.1V_{DD}		
Pin capacitance	CP	All pins	•f=1MHz •For the pin other than that under test V_{IN}=V_{SS} •Ta=25°C	2.5 to 5.5		10		pF
Input sensitivity	Vsen	•P87 small signal input side		2.5 to 5.5	0.12V_{DD}			Vpp

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Serial I/O Characteristics at Ta = -20 to +70°C, $V_{SS1} = V_{SS2} = 0V$

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min.	typ.	max.	unit
Serial clock	Input clock	Period	tSCK(1)	SCK0(P12)	See Fig. 6.	2.5 to 5.5	4/3			tCYC
		Low level pulse width	tSCKL(1)	SCK2(SI2P2) (LC876B00 compatible)		2.5 to 5.5	2/3			
			tSCKLA(1)			2.5 to 5.5	2/3			
		High level pulse width	tSCKH(1)			2.5 to 5.5	2/3			
			tSCKHA(1)			2.5 to 5.5	5			
		Period	tSCK(2)	SCK1(P15)	See Fig. 6.	2.5 to 5.5	2			
		Low level pulse width	tSCKL(2)			2.5 to 5.5	1			
		High level pulse width	tSCKH(2)			2.5 to 5.5	1			
	Output clock	Period	tSCK(3)	SCK0(P12)	•CMOS output type selected •See Fig. 6.	2.5 to 5.5	4/3			
		Low level pulse width	tSCKL(3)	SCK2(SI2P2), SCK2O(SI2P3) (LC876B00 compatible)		2.5 to 5.5		1/2		tSCK
			tSCKLA(2)		SCK(P12) For SIO0	2.5 to 5.5		3/4		
					SI2P2, SI2P3 For SIO2			1		
		High level pulse width	tSCKH(3)			2.5 to 5.5		1/2		
			tSCKHA(2)		SCK(P12) For SIO0	2.5 to 5.5		2		
					SI2P2, SI2P3 For SIO2			7/4		
		Period	tSCK(4)	SCK1(P15)	•CMOS output type selected •See Fig. 6.	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(4)			2.5 to 5.5		1/2		tSCK
		High level pulse width	tSCKH(4)			2.5 to 5.5		1/2		
Serial input		Data setup time	tsDI	SI0(P11), SI1(P14), SB0(P11), SB1(P14)	•Specified with respect to the rising edge of SIOCLK. •See Fig. 6.	4.5 to 5.5	0.03			μs
						3.0 to 4.5	0.05			
						2.5 to 3.0	0.1			
		Data hold time	thDI	SI2(SI2P1), SB2(SI2P1) (LC876B00 compatible)		4.5 to 5.5	0.03			
						3.0 to 4.5	0.05			
						2.5 to 3.0	0.1			
Serial output		Output delay time	tdDO	SO0(P10), SO1(P13), SB0(P11), SB1(P14)	•Specified with respect to the falling edge of SIOCLK. •Specified as the time up to the beginning of output change in open drain output mode. •See Fig. 6.	3.0 to 5.5			1/3 tCYC +0.05	
				SO2(SI2P0), SB2(SI2P1) (LC876B00 compatible)		2.5 to 3.0			1/3 tCYC +0.15	

Note: The SIO2 function is available only when the LC876B00 series compatible configuration is selected as a user option.

5. Pulse Input Conditions at Ta = -20 to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72)	•Interrupt source flag can be set. •Event input to timers 0 and 1 is enabled.	2.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	•INT4(P30 to P33) •INT5(P34 to P37) •INT6(P30) •INT7(P34) (LC876A00 compatible) •INT4(SI2P0, SI2P1, P32, P33) •INT5(P34, P35, SI2P2, SI2P3) •INT6(SI2P0) •INT7(P34) (LC876B00 compatible)	•Interrupt source flag can be set. •Event input to timers 0 and 1 is enabled.	2.5 to 5.5	1			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/1	•Interrupt source flag can be set. •Event input to timer 0 is enabled.	2.5 to 5.5	2			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/32	•Interrupt source flag can be set. •Event input to timer 0 is enabled.	2.5 to 5.5	64			
	tPIH(5) tPIL(5)	INT3(P73) when noise filter time constant is 1/128	•Interrupt source flag can be set. •Event input to timer 0 is enabled.	2.5 to 5.5	256			
	tPIH(6) tPIL(6)	MICIN(P87)	Small signal detection counter counted	2.5 to 5.5	1			
	tPIH(7) tPIL(7)	NKIN(P72)	High-speed clock counter counted	2.5 to 5.5	1/12			
	tPIL(8)	$\overline{RES}$	Reset is enabled.	2.5 to 5.5	200			µs

6. AD Converter Characteristics at Ta = -20 to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min.	typ.	max.	unit
Resolution	N	•AN0(P80) to AN7(P87), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2) •AN12, AN13(P36, P37) (LC876A00 compatible) •AN12, AN13 (SI2P2, SI2P3) (LC876B00 compatible) •AN14 (P16)		3.0 to 5.5		8		bit
Absolute precision	ET		(Note 3)	3.0 to 5.5			±1.5	LSB
Conversion time	tCAD		AD conversion time=32 × tCYC (when ADCR2=0) (Note 4)	4.5 to 5.5	15.62 (tCYC= 0.488µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	23.52 (tCYC= 0.735µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64 × tCYC (when ADCR2=1) (Note 4)	4.5 to 5.5	18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 5.5	47.04 (tCYC= 0.735µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 3: The quantization error (±1/2LSB) is excluded from the absolute accuracy.

Note 4: The conversion time refers to the interval from the time a conversion starting instruction is issued until the time the complete digital value corresponding to the analog input value is loaded in the register.

7. Consumption Current Characteristics at Ta = -20 to +70°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min.	typ.	max.	unit
Normal mode consumption current (Note 5)	IDDOP(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ =$V_{DD}4$	•FmCF=12MHz ceramic oscillation •FsX'tal=32.768kHz crystal oscillation •System clock set to 12MHz side •Internal RC oscillation stopped •Frequency division ratio set to 1/1	4.5 to 5.5		7.9	24	mA
				2.8 to 4.5		3.8	14	
	IDDOP(2)		•CF1=20MHz external clock •FsX'tal=32.768kHz crystal oscillation •System clock set to CF1 side •Internal RC oscillation stopped •Frequency division ratio set to 1/2	4.5 to 5.5		7.8	22	
				2.8 to 4.5		3.5	12	
	IDDOP(3)		•FmCF=4MHz ceramic oscillation •FsX'tal=32.768kHz crystal oscillation •System clock set to 4MHz side •Internal RC oscillation stopped •Frequency division ratio set to 1/1	4.5 to 5.5		4.8	14	
				2.5 to 4.5		2.4	6	
	IDDOP(4)		•FmCF=0Hz (oscillation stopped) •FsX'tal=32.768kHz crystal oscillation •Internal RC oscillation stopped •System clock set to internal multifrequency oscillator RC oscillator set to 1MHz •Frequency division ratio set to 1/2	4.5 to 5.5		1.6	10	
				2.5 to 4.5		0.7	4	
	IDDOP(5)		•FmCF=0Hz (oscillation stopped) •FsX'tal=32.768kHz crystal oscillation •System clock set to internal RC oscillator •Frequency division ratio set to 1/2	4.5 to 5.5		0.85	4	
				2.5 to 4.5		0.35	3	
	IDDOP(6)		•FmCF=0Hz (oscillation stopped) •FsX'tal=32.768kHz crystal oscillation •System clock set to 32.768kHz side •Internal RC oscillation stopped •Frequency division ratio set to 1/2	4.5 to 5.5		290	1100	μA
				2.5 to 4.5		96.0	400	

Continued on next page.

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Parameter	Symbol	Pin/Remarks	Conditions	V$_{DD}$[V]	Specification min.	typ.	max.	unit
HALT mode consumption current (Note 5)	IDDHALT(1)	V$_{DD}$1 =V$_{DD}$2 =V$_{DD}$3 =V$_{DD}$4	•HALT mode •FmCF=12MHz ceramic oscillation •FsX'tal=32.768kHz crystal oscillation •System clock set to 12MHz side •Internal RC oscillation stopped •Frequency division ratio set to 1/1	4.5 to 5.5		3.4	10	mA
				2.8 to 4.5		1.3	6	
	IDDHALT(2)		•HALT mode •CF1=20MHz external clock •FsX'tal=32.768kHz crystal oscillation •System clock set to CF1 side •Internal RC oscillation stopped •Frequency division ratio set to 1/2	4.5 to 5.5		3.9	10	
				2.8 to 4.5		1.5	6	
	IDDHALT(3)		•HALT mode •FmCF=4MHz ceramic oscillation •FsX'tal=32.768kHz crystal oscillation •System clock set to 4MHz side •Internal RC oscillation stopped •Frequency division ratio set to 1/1	4.5 to 5.5		1.6	4	
				2.5 to 4.5		0.7	3	
	IDDHALT(4)		•HALT mode •FmCF=0Hz (oscillation stopped) •FsX'tal=32.768kHz crystal oscillation •Internal RC oscillation stopped •System clock is internal multifrequency RC oscillator set to 1MHz •Frequency division ratio set to 1/2	4.5 to 5.5		1000	3000	μA
				2.5 to 4.5		440	2500	
	IDDHALT(5)		•HALT mode •FmCF=0Hz (oscillation stopped) •FsX'tal=32.768kHz crystal oscillation •System clock set to internal RC oscillator •Frequency division ratio set to 1/2	4.5 to 5.5		300	1200	
				2.5 to 4.5		130	750	
	IDDHALT(6)		•HALT mode •FmCF=0Hz (oscillation stopped) •FsX'tal=32.768kHz crystal oscillation •System clock set to 32.768kHz side •Internal RC oscillation stopped •Frequency division ratio set to 1/2	4.5 to 5.5		25	80	
				2.5 to 4.5		7.4	45	
HOLD mode consumption current	IDDHOLD(1)	V$_{DD}$1	•HOLD mode •CF1=V$_{DD}$ or open (external clock mode)	4.5 to 5.5		0.04	20	
				2.5 to 4.5		0.01	15	
Timer HOLD mode consumption current	IDDHOLD(2)	V$_{DD}$1	•Timer HOLD mode •CF1=V$_{DD}$ or open (external clock mode) •FsX'tal=32.768kHz crystal oscillation	4.5 to 5.5		22	65	
				2.5 to 4.5		5.7	40	

Note 5: The consumption current value does not include the currents that flow into the output transistors and internal pull-up resistors.

8. F-ROM Programming Characteristics at Ta = +10 to +55°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min.	typ.	max.	unit
					Specification			
Onboard programming current	IDDFW(1)	$V_{DD}1$	•128-byte write •Including erase current	3.0 to 5.5		25	40	mA
Programming time	tFW(1)		•128-byte write •Including erase current •Excluding the time for setting up 128-byte data	3.0 to 5.5		22.5	45	ms

9. Power Pin Treatment Conditions 1 (V$_{DD}$1, V$_{SS}$1)

It is necessary to place capacitors between V$_{DD}$1 and V$_{SS}$1 as described below.

- Trace length from V$_{DD}$1, V$_{SS}$1 pins to capacitors C1, C2 should be as short as possible and of the same length (L1=L1', L2=L2') wherever possible.
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
  Capacitance of C2 must be 0.1μF or more.
- V$_{DD}$1 and V$_{SS}$1 wiring traces must be thicker than other traces.
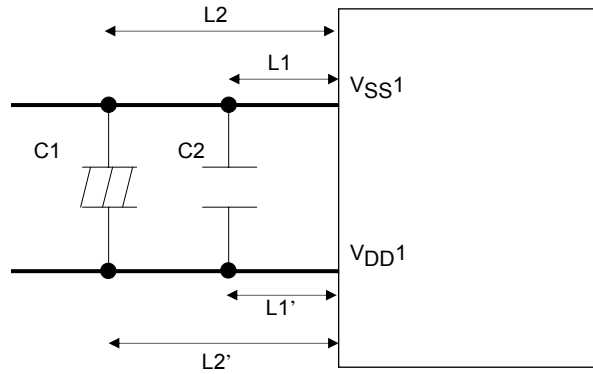
10. Power Pin Treatment Conditions 2 (V$_{DD}$2, V$_{SS}$2)

It is necessary to place capacitors between V$_{DD}$2 and V$_{SS}$2 as described below.

- Trace length from V$_{DD}$2, V$_{SS}$2 pins to capacitor C3 should be as short as possible and of the same length (L3=L3') wherever possible.
- Capacitance of C3 must be 0.1μF or more.
- The V$_{DD}$2 and V$_{SS}$2 wiring traces must be thicker than other traces.
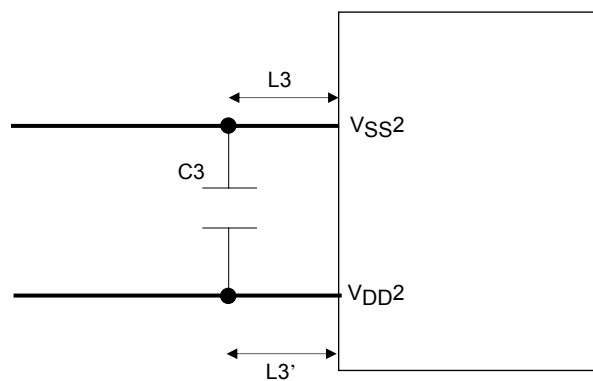
Characteristics of a Sample Main System Clock Oscillator Circuit

Given below are the characteristics of a sample main system clock oscillator circuit that are measured using our company-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constants			Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rd1 [Ω]		Typ [ms]	Max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	470	2.8 to 5.5	0.05	0.15	C1, C2 integrated type
4MHz	MURATA	CSTLS4M00G53-B0	(15)	(15)	2.2k	2.5 to 5.5	0.05	0.15	C1, C2 integrated type
		CSTCR4M00G53-R0	(15)	(15)	2.2k	2.5 to 5.5	0.07	0.2	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the lower limit level of the operating voltage range (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillator circuit that are measured using our company-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constants				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		Typ [S]	Max [S]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	10M	0	2.5 to 5.5	1.5	3	Applicable CL value 12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed or the time interval that is required for the oscillation to get stabilized after HOLD mode is released (see Figure 4).

Note: The components for oscillation should be placed and routed as close to the IC as possible because they are vulnerable to the influences of the circuit pattern.
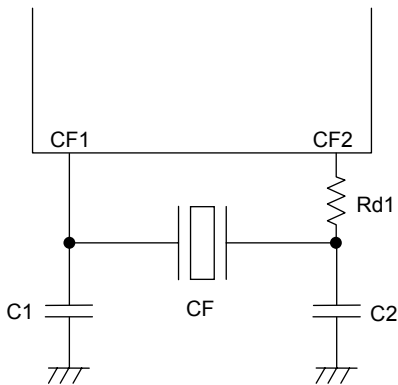
Figure 1 CF Oscillator Circuit
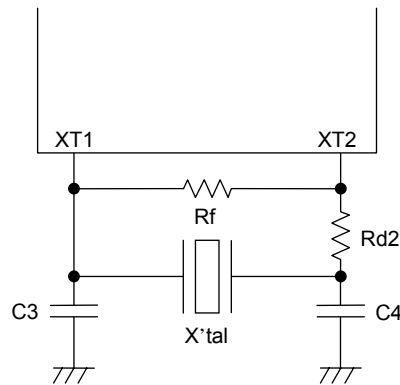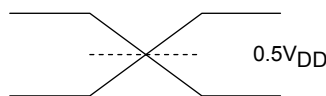

Figure 2 XT Oscillator Circuit

Figure 3 AC Timing Measurement Point

Reset Time and Oscillation Stabilization Time

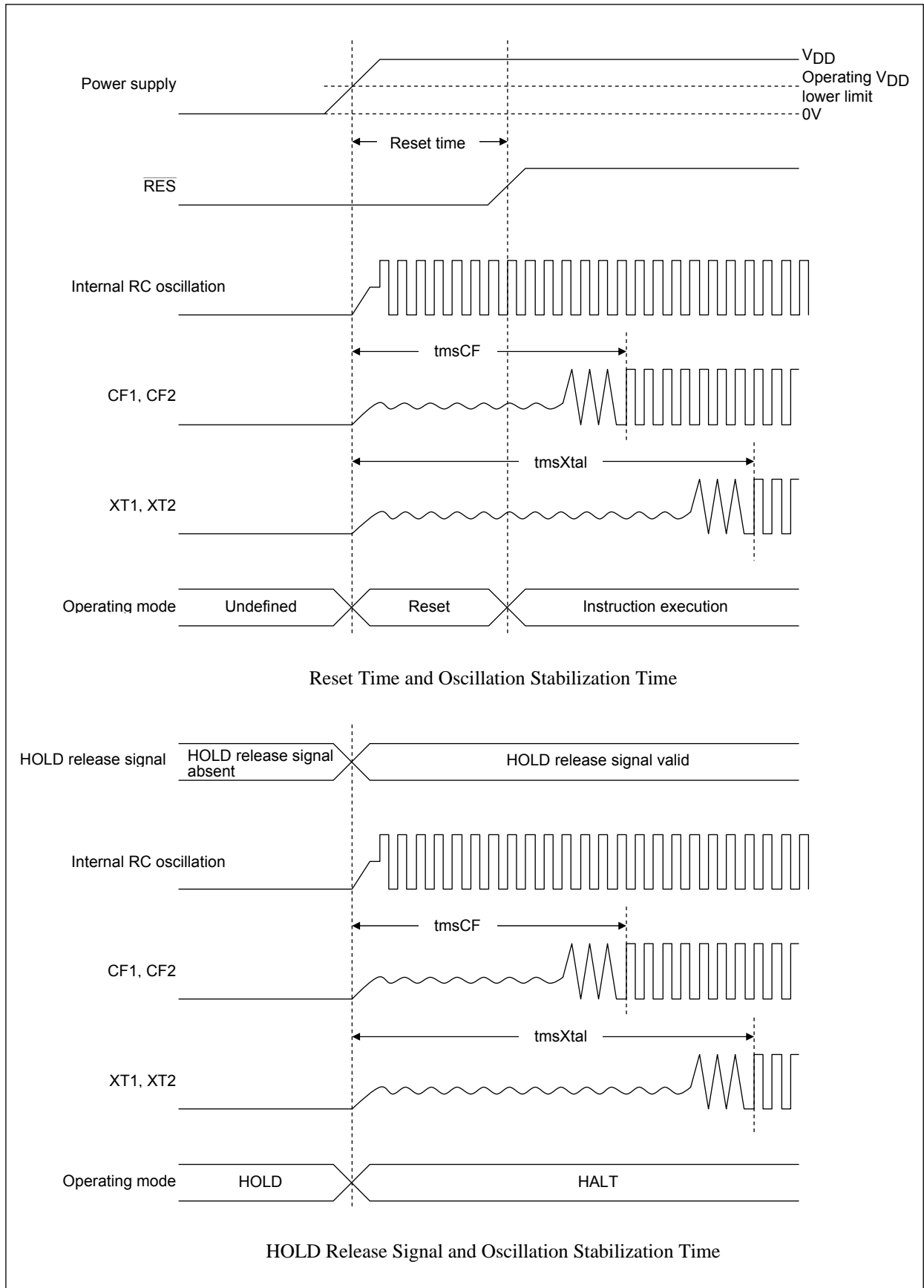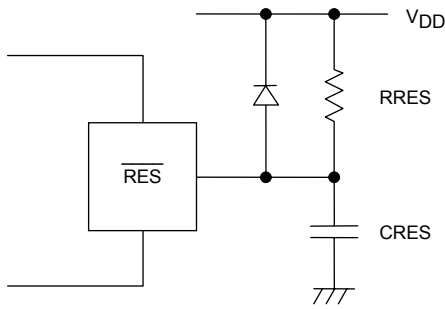HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time

Figure 5 Reset Circuit

Note: Determine the value of CRES and RRES so that the reset signal is clearly present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage range.

Figure 6 Serial I/O Waveforms
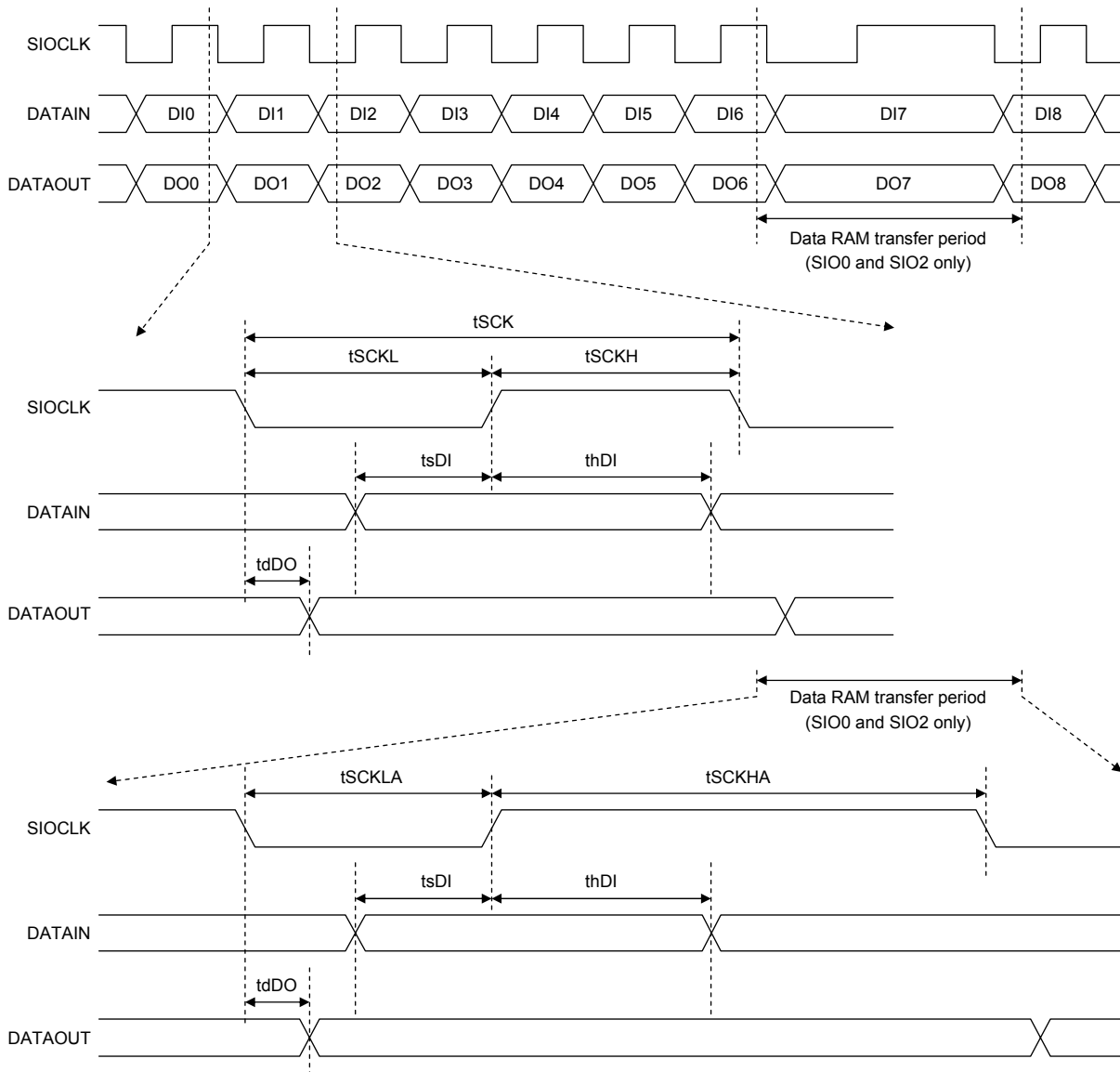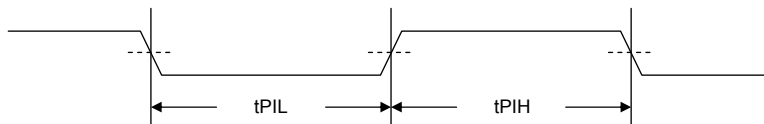

Figure 7 Pulse Input Timing Signal Waveform

LC87F6AC8A

■ Difference between the LC876A00 and LC876900 Series

Function	LC876A00 Series	LC876900 Series
ADC	8 bits ×15 channels Conversion time: 32/64/128/256 tCYC	8 bits ×14 channels Conversion time: 32/64 tCYC
PWM	PWM4/PWM5 (P30/P31multiplexed pin functions)	PWM2/PWM3 (dedicated pin)
Port3	P30 to P37: 8 bits (No middle withstand voltage port)	P32 to P37: 6 bits (P32 to P35: Medium withstand voltage input support ports)
No. of VFD pins	48	52
Middle withstand voltage input voltage	12V max. (P0)	14V max. (P0, P32 to 35)
Timer 0 capture registers	2 (T0CAH/T0CAL, T0CAH1/T0CAL1)	1 (T0CAH/T0CAL)
Timer 8	8-bit timer with 8-bit prescaler × 2 channels 16-bit timer with 8-bit prescaler × 2 channels	Not supported
External interrupt INT6/INT7	INT6 is assigned to P30 and INT7 to P34.	
No. of Port A bits	PA0 to PA3: 4 bits	
Multifrequency RC oscillator	Built-in	
IFLG	List of interrupt source flag function	

Pin Assignment	LC876A00 Series	LC876900 Series
Pin 1	P16/T1PWML/AN14	P16/T1PWML
Pin 3	P30/INT4/T1IN/INT6/T0LCP1/PWM4	PWM2/INT4/T1IN
Pin 4	P31/INT4/T1IN/PWM5	PWM3/INT4/T1IN
Pin 7	P34/INT5/T1IN/INT7/T0HCP1	P34/INT5/T1IN
Pin 81	PA0	S48/PG0
Pin 82	PA1	S49/PG1
Pin 83	PA2	S51/PG2
Pin 84	PA3	S52/PG3

LC87F6AC8A

■ Difference between the LC876B00 Series and LC876800 Series

Function	LC876B00 Series	LC876800 Series
ADC	8 bits ×15 channels Conversion time: 32/64/128/256 tCYC	8 bits ×14 channels Conversion time: 32/64 tCYC
Port3 (4 bits)	No middle withstand voltage port	Medium withstand voltage input support
No. of VFD pins	48	52
Middle withstand voltage input voltage	12V max. (P0)	14V max. (P0, P3)
Timer 0 capture resisters	2 (T0CAH/T0CAL, T0CAH1/T0CAL1)	1 (T0CAH/T0CAL)
Timer 8	8-bit timer with 8-bit prescaler × 2 channels 16-bit timer with 8-bit prescaler × 2 channels	Not supported
External interrupt INT6/INT7	INT6 is assigned to P0 and INT7 to P34.	
Multifrequency RC oscillator	Built-in	
No. of Port A bits	PA0 to PA3: 4 bits	
IFLG	List of interrupt source flag function	

Pin Assignment	LC876B00 Series	LC876800 Series
Pin 1	P16/T1PWML/AN14	P16/T1PWML
Pin 3	SI2P0/SO2/INT4/T1IN/INT6/T0LCP1	SI2P0/SO2/INT4/T1IN
Pin 7	P34/INT5/T1IN/INT7/T0HCP1	P34/INT5/T1IN
Pin 81	PA0	S48/PG0
Pin 82	PA1	S49/PG1
Pin 83	PA2	S51/PG2
Pin 84	PA3	S52/PG3

■ Operating Voltage Differences between the LC876A00/LC876B00 Series and LC876800/ LC876900 Series

Operating Supply Voltage	LC876A00/LC876B900 Series	LC876800/LC876900 Series
Operating supply voltage/instruction cycle time	2.8 to 5.5[V] (0.252μs ≤ Tcyc ≤ 200μs) 2.5 to 5.5[V] (0.735μs ≤ Tcyc ≤ 200μs) Except for onboard programming (V_{DD} < 4.5V)	3.0 to 5.5[V] (0.294μs ≤ Tcyc ≤ 200μs) 2.5 to 5.5[V] (0.735μs ≤ Tcyc ≤ 200μs) Except for onboard programming (V_{DD} < 4.5V)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F6AC8ALU-EJ-H	QIP100E(14X20) (Pb-Free / Halogen Free)	250 / Tray Foam