Freescale Semiconductor
Technical Data

Document Number: MRFE6VP61K25H
Rev. 4, 3/2013

RoHS

RF Power LDMOS Transistors

High Ruggedness N-Channel Enhancement-Mode Lateral MOSFETs

MRFE6VP61K25HR6
MRFE6VP61K25HSR5
MRFE6VP61K25GSR5

These high ruggedness devices are designed for use in high VSWR industrial (including laser and plasma exciters), broadcast (analog and digital), aerospace and radio/land mobile applications. They are unmatched input and output designs allowing wide frequency range utilization, between 1.8 and 600 MHz.

- Typical Performance: V_{DD} = 50 Volts, I_{DQ} = 100 mA

Signal Type	P_{out} (W)	f (MHz)	G_{ps} (dB)	η_D (%)
Pulse (100 μsec, 20% Duty Cycle)	1250 Peak	230	24.0	74.0
CW	1250 CW	230	22.9	74.6

Application Circuits (1) — Typical Performance

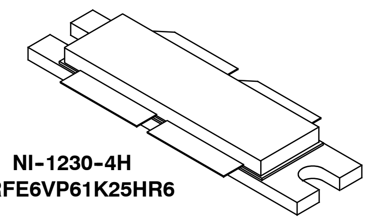
Frequency (MHz)	Signal Type	P_{out} (W)	G_{ps} (dB)	η_D (%)
27	CW	1300	27	81
40	CW	1300	26	85
81.36	CW	1250	27	84
87.5-108	CW	1100	24	80
144-148	CW	1250	26	78
170-230	DVB-T	225	25	30
352	Pulse (200 μsec, 20% Duty Cycle)	1250	21.5	66
352	CW	1150	20.5	68
500	CW	1000	18	58

1. Contact your local Freescale sales office for additional information on specific circuit designs.

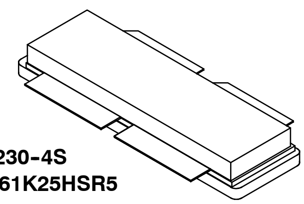
Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	P_{out} (W)	Test Voltage	Result
230	Pulse (100 μsec, 20% Duty Cycle)	>65:1 at all Phase Angles	1500 Peak (3 dB Overdrive)	50	No Device Degradation

1.8-600 MHz, 1250 W CW, 50 V WIDEBAND RF POWER LDMOS TRANSISTORS



NI-1230-4H
MRFE6VP61K25HR6



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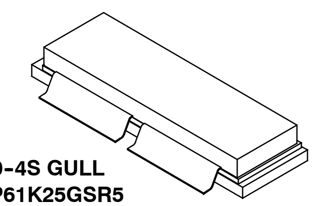
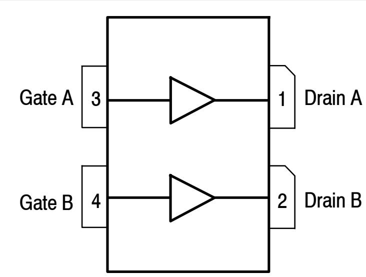


NI-1230-4S GULL
MRFE6VP61K25GSR5



(Top View)

Note: The backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Features

- Unmatched Input and Output Allowing Wide Frequency Range Utilization
- Device can be used Single-Ended or in a Push-Pull Configuration
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Characterized from 30 V to 50 V for Extended Power Range
- Suitable for Linear Application with Appropriate Biasing
- Integrated ESD Protection with Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel. R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel.

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +133	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1333 6.67	W W/°C
Operating Junction Temperature [1,2]	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case CW: Case Temperature 63°C, 1250 W CW, I_{DQ} = 100 mA, 230 MHz	$R_{\theta JC}$	0.15	°C/W
Thermal Impedance, Junction to Case Pulse: Case Temperature 66°C, 1250 W Pulse, 100 μsec Pulse Width, 20% Duty Cycle, I_{DQ} = 100 mA, 230 MHz	$Z_{\theta JC}$	0.03	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 3500 V
Machine Model (per EIA/JESD22-A115)	B, passes 250 V
Charge Device Model (per JESD22-C101)	IV, passes 4000 V

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [4]					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 mA)	$V_{(BR)DSS}$	133	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	20	μAdc
On Characteristics					
Gate Threshold Voltage [4] (V_{DS} = 10 Vdc, I_D = 1776 μAdc)	$V_{GS(th)}$	1.7	2.2	2.7	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.9	2.2	2.9	Vdc
Drain-Source On-Voltage [4] (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.15	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 30 Adc)	g_{fs}	—	28.0	—	S
Dynamic Characteristics [4]					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	2.8	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	185	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	562	—	pF

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [(1)] (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 1250 W Peak (250 W Avg.), f = 230 MHz, 100 μsec Pulse Width, 20% Duty Cycle					
Power Gain	G_{ps}	23.0	24.0	26.0	dB
Drain Efficiency	η_D	72.5	74.0	—	%
Input Return Loss	IRL	—	-14	-10	dB

Table 5. Load Mismatch/Ruggedness (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 100 mA

Frequency (MHz)	Signal Type	VSWR	P_{out} (W)	Test Voltage, V_{DD}	Result
230	Pulse (100 μsec, 20% Duty Cycle)	>65:1 at all Phase Angles	1500 Peak (3 dB Overdrive)	50	No Device Degradation

1. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.

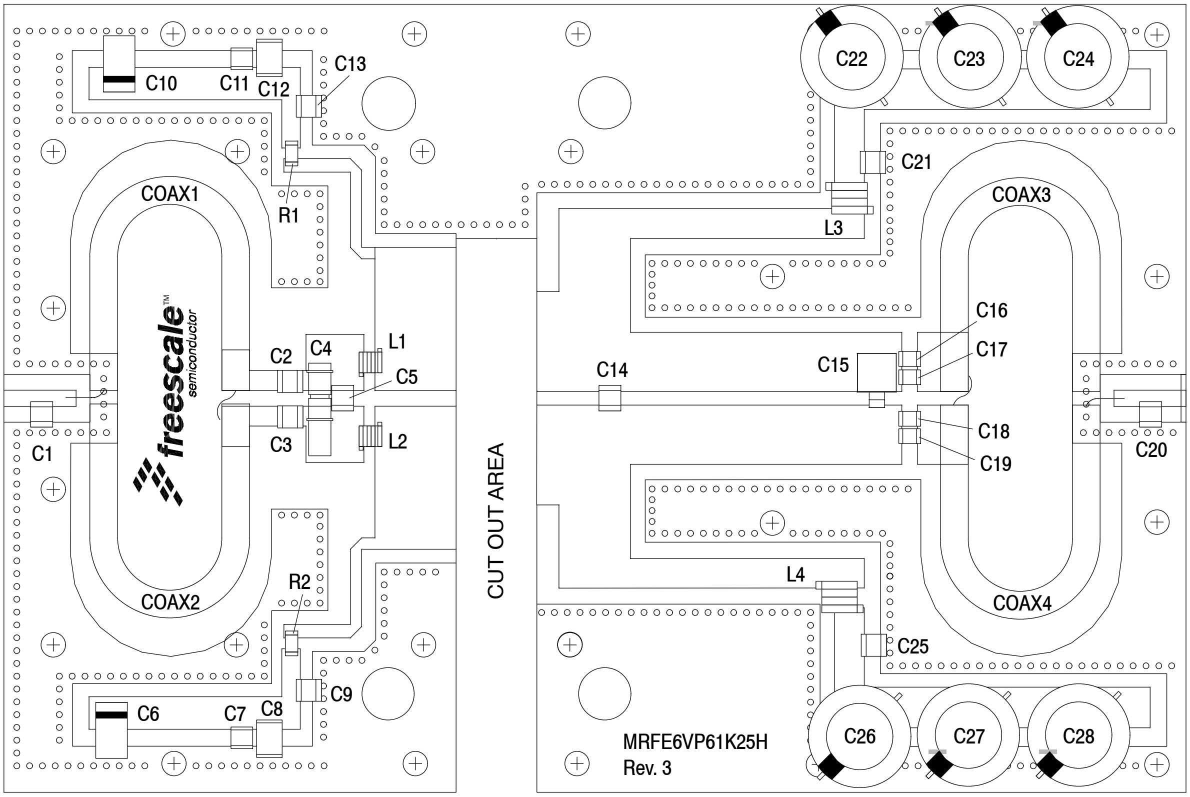


Figure 2. MRFE6VP61K25HR6(HSR6) 230 MHz Production Test Circuit Component Layout — Pulse

Table 6. MRFE6VP61K25HR6(HSR6) 230 MHz Production Test Circuit Component Designations and Values — Pulse

Part	Description	Part Number	Manufacturer
C1	20 pF Chip Capacitor	ATC100B200JT500XT	ATC
C2, C3, C5	27 pF Chip Capacitors	ATC100B270JT500XT	ATC
C4	0.8-8.0 pF Variable Capacitor, Gigatrim	27291SL	Johanson
C6, C10	22 μF, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C7, C11	0.1 μF Chip Capacitors	CDR33BX104AKYS	AVX
C8, C12	220 nF Chip Capacitors	C1812C224K5RACTU	Kemet
C9, C13, C21, C25	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C14	43 pF Chip Capacitor	ATC100B430JT500XT	ATC
C15	75 pF Metal Mica	MIN02-002EC750J-F	CDE
C16, C17, C18, C19	240 pF Chip Capacitors	ATC100B241JT200XT	ATC
C20	6.2 pF Chip Capacitor	ATC100B6R2BT500XT	ATC
C22, C23, C24, C26, C27, C28	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
Coax1, 2, 3, 4	25 Ω Semi Rigid Coax, 2.2″ Shield Length	UT-141C-25	Micro-Coax
L1, L2	5 nH Inductors	A02TKLC	Coilcraft
L3, L4	6.6 nH Inductors	GA3093-ALC	Coilcraft
R1, R2	10 Ω Chip Resistors	CRCW120610R0JNEA	Vishay
PCB	0.030″, ε_r = 2.55	AD255A	Arlon

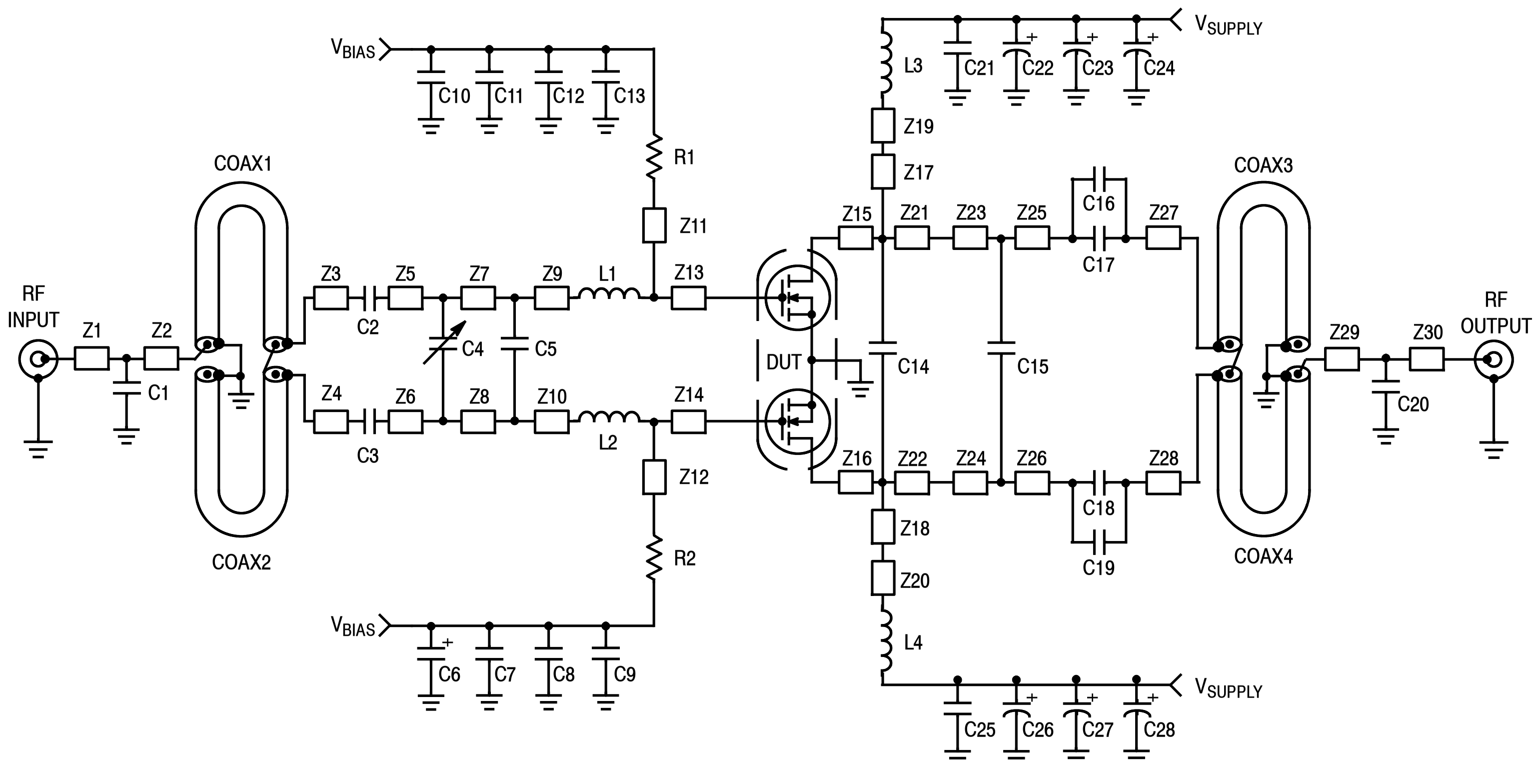
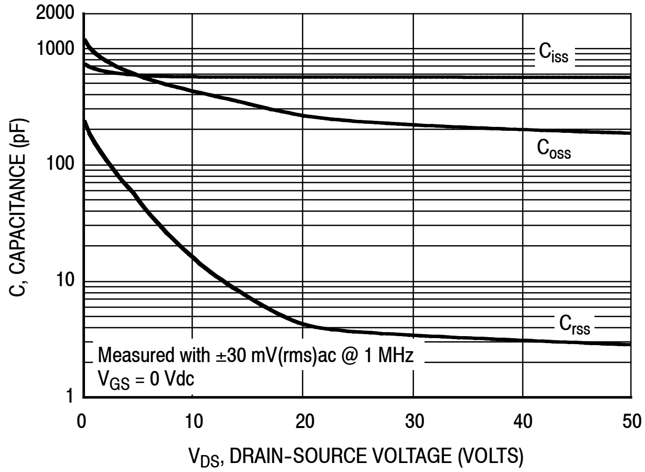


Figure 3. MRFE6VP61K25HR6(HSR6) 230 MHz Production Test Circuit Schematic — Pulse

Table 7. MRFE6VP61K25HR6(HSR6) 230 MHz Production Test Circuit Microstrips — Pulse

Microstrip	Description	Microstrip	Description	Microstrip	Description
Z1	0.192″ × 0.082″ Microstrip	Z11*, Z12*	0.872″ × 0.058″ Microstrip	Z23, Z24	1.251″ × 0.300″ Microstrip
Z2	0.175″ × 0.082″ Microstrip	Z13, Z14	0.412″ × 0.726″ Microstrip	Z25, Z26	0.127″ × 0.300″ Microstrip
Z3, Z4	0.170″ × 0.100″ Microstrip	Z15, Z16	0.371″ × 0.507″ Microstrip	Z27, Z28	0.116″ × 0.300″ Microstrip
Z5, Z6	0.116″ × 0.285″ Microstrip	Z17*, Z18*	0.466″ × 0.363″ Microstrip	Z29	0.186″ × 0.082″ Microstrip
Z7, Z8	0.116″ × 0.285″ Microstrip	Z19*, Z20*	0.187″ × 0.154″ Microstrip	Z30	0.179″ × 0.082″ Microstrip
Z9, Z10	0.108″ × 0.285″ Microstrip	Z21, Z22	0.104″ × 0.507″ Microstrip		

* Line length includes microstrip bends



Note: Each side of device measured separately.

Figure 4. Capacitance versus Drain-Source Voltage

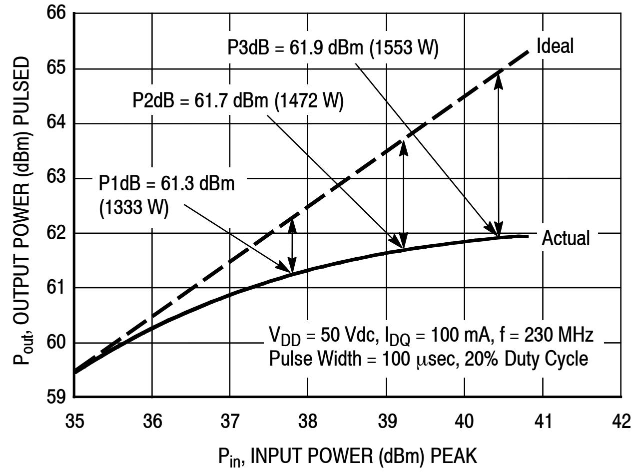


Figure 5. Output Power versus Input Power

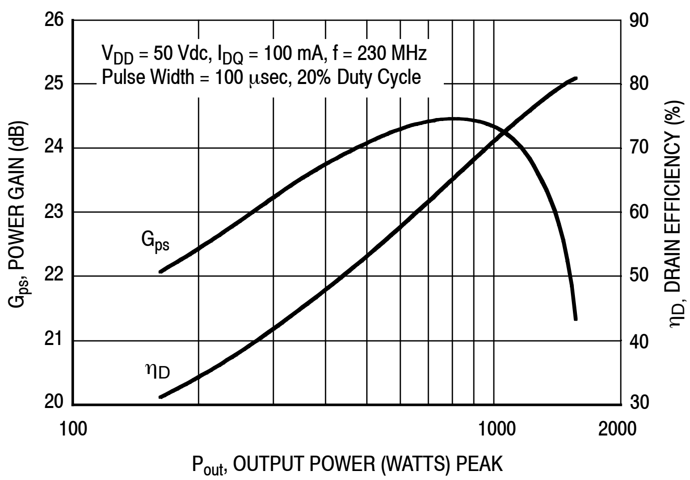


Figure 6. Power Gain and Drain Efficiency versus Output Power

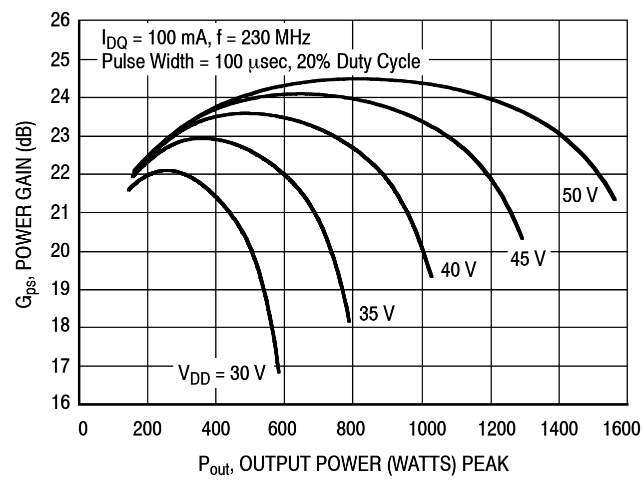


Figure 7. Power Gain versus Output Power

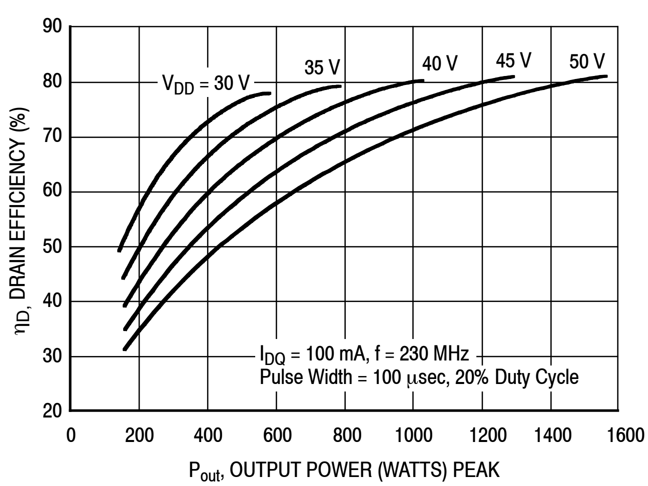


Figure 8. Drain Efficiency versus Output Power

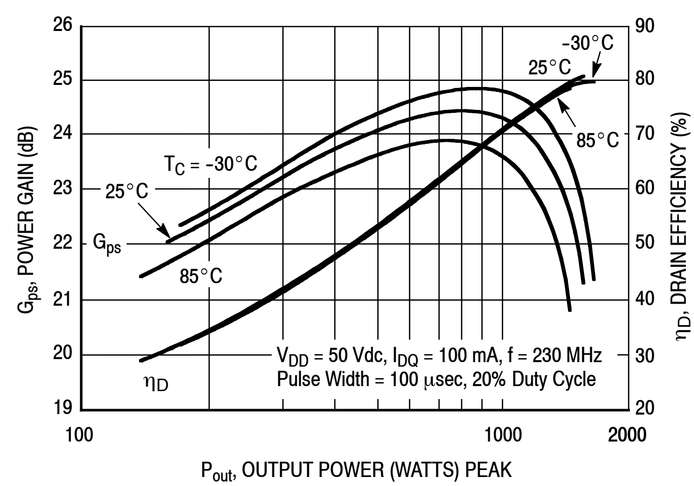
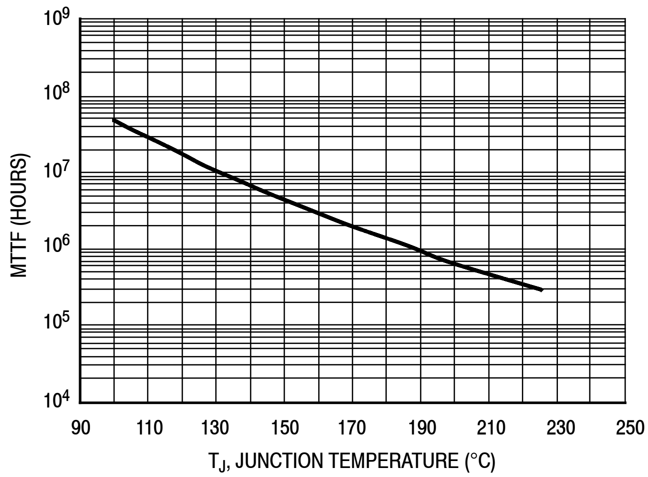


Figure 9. Power Gain and Drain Efficiency versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 50 Vdc, P_{out} = 1250 W CW, and η_D = 74.6%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 10. MTTF versus Junction Temperature — CW

V_{DD} = 50 Vdc, I_{DQ} = 100 mA, P_{out} = 1250 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
230	1.29 + j3.54	2.12 + j2.68

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

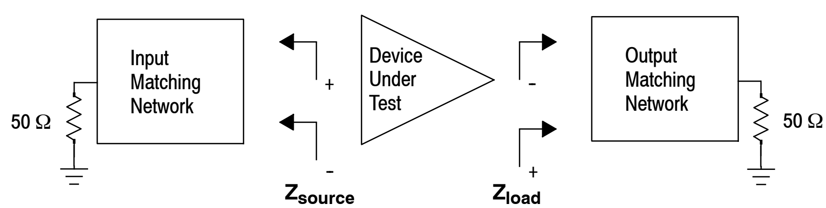


Figure 11. Series Equivalent Test Circuit Source and Load Impedance — 230 MHz Pulse

V_{DD} = 50 Vdc, I_{DQ} = 100 mA

f (MHz)	Z_{source} (Ω)	Z_{load} (Ω)
1.8 [(1)]	34.4 + j192.0 [(1)]	5.00 - j4.00 [(1)]
27	12.5 + j7.00	7.00 + j0.70
40	5.75 + j5.06	5.39 + j2.62
81.36	4.04 + j5.93	4.89 + j2.95
88	2.20 + j6.70	4.90 + j2.90
98	2.30 + j6.90	4.10 + j2.50
108	2.30 + j7.00	4.40 + j3.60
144	1.60 + j5.00	3.90 + j1.50
175	1.33 + j3.90	3.50 + j2.50
230	1.29 + j3.54	2.12 + j2.68
352	0.98 + j1.45	1.82 + j2.05
500	0.29 + j1.47	1.79 + j1.80

1. Simulated data.

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

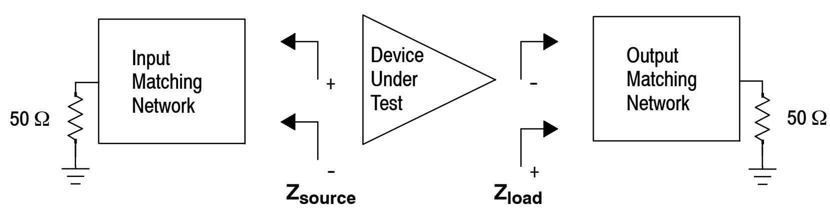
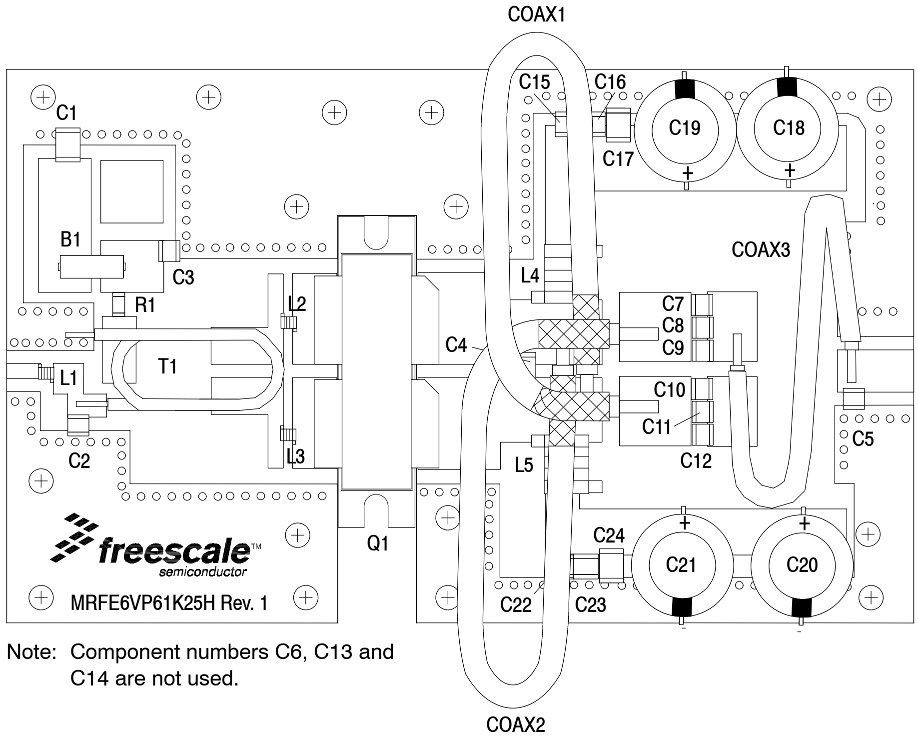


Figure 12. Source and Load Impedances Optimized for IRL, Power and Efficiency — Push-Pull



Note: Component numbers C6, C13 and C14 are not used.

Figure 13. MRFE6VP61K25HR6(HSR6) 87.5-108 MHz FM Broadcast Reference Circuit Component Layout

Table 8. MRFE6VP61K25HR6(HSR6) 87.5-108 MHz FM Broadcast Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Long Ferrite Bead	2743021447	Fair-Rite
C1	6.8 μF, 50 V Chip Capacitor	C4532X7R1H685K	TDK
C2	27 pF Chip Capacitor	ATC100B270JT500XT	ATC
C3, C7, C8, C9, C10, C11, C12	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C4	39 pF Mica Capacitor	MIN02-002DC390J-F	Cornell Dubilier
C5	3 pF Chip Capacitor	ATC100B3R0CT500XT	ATC
C15, C22	10K pF Chip Capacitors	ATC200B103KT50XT	ATC
C16, C23	1 μF, 100 V Chip Capacitors	C3225JB2A105KT	TDK
C17, C24	10 μF, 100 V Chip Capacitors	C5750X7S2A106MT	TDK
C18, C19, C20, C21	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
L1	39 nH Inductor	1812SMS-39NJLC	Coilcraft
L2, L3	2.5 nH Inductors	A01TKLC	Coilcraft
L4, L5	7 Turn, #16 AWG, ID = 0.3″ Inductors	Copper Wire	
Q1	RF Power LDMOS Transistor	MRFE6VP61K25HR6	Freescale
R1	11 Ω, 1/4 W Chip Resistor	CRCW120611R0FKEA	Vishay
T1	Balun	TUI-9	Comm Concepts
Coax1, Coax2	Flex Cables (12 Ω) 5.9″	TC-12	Comm Concepts
Coax3	Coax Cable, Quickform 50 Ω, 8.7″	SUCOFORM 250-01	Huber+Suhner
PCB	0.030″, ε_r = 3.5	TC-350	Arlon
Heatsink	NI-1230 Copper Heatsink	C193X280T970	Machine Shop

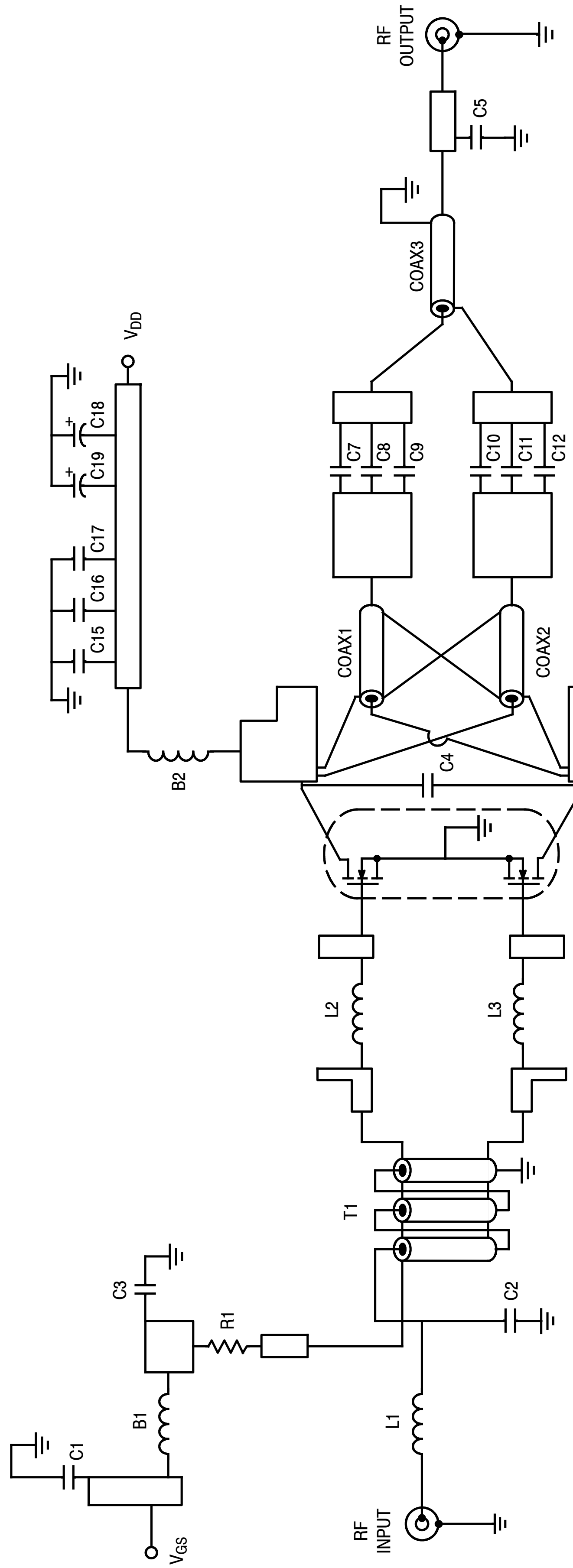


Figure 14. MRFE6VP61K25HR6(HSR6) 87.5–108 MHz FM Broadcast Reference Circuit Schematic

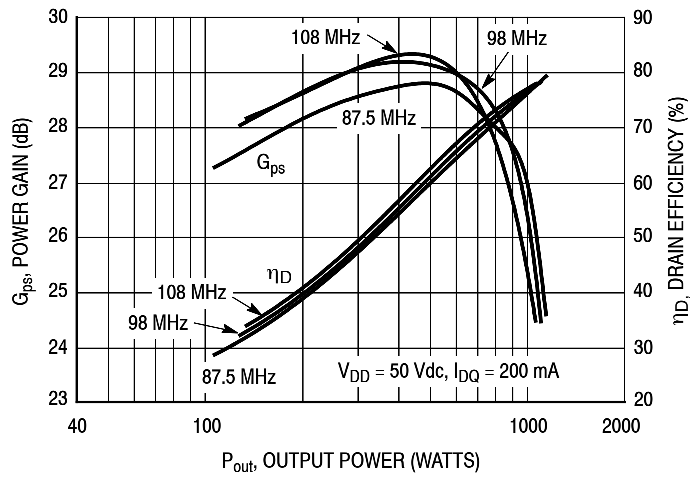


Figure 15. Power Gain and Drain Efficiency versus Output Power

V_{DD} = 50 Vdc, I_{DQ} = 200 mA, P_{out} = 1100 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
87.5	2.20 + j6.70	4.90 + j2.90
98	2.30 + j6.90	4.10 + j2.50
108	2.30 + j7.00	4.40 + j3.60

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

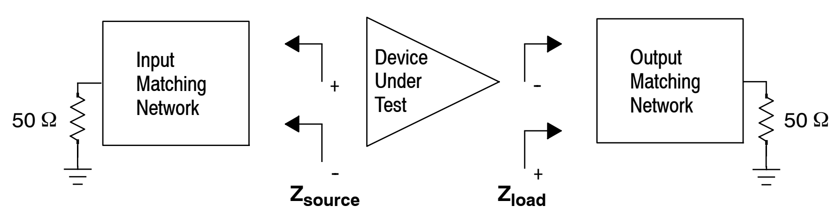
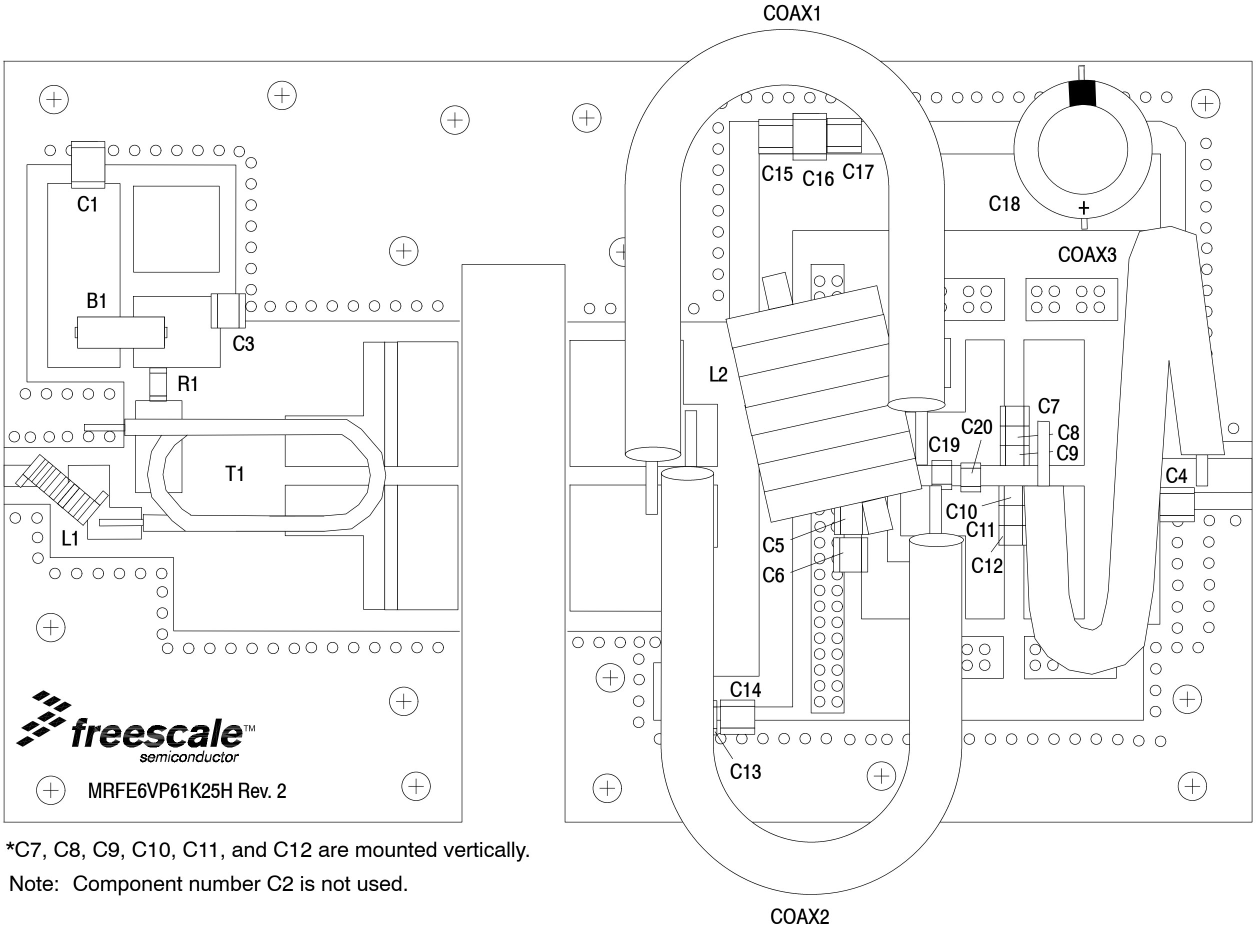


Figure 16. Series Equivalent 87.5-108 MHz FM Broadcast Reference Circuit Source and Load Impedance

144-148 MHz REFERENCE CIRCUIT



*C7, C8, C9, C10, C11, and C12 are mounted vertically.

Note: Component number C2 is not used.

Figure 17. MRFE6VP61K25HR6(HSR6) 144-148 MHz Reference Circuit Component Layout

Table 9. MRFE6VP61K25HR6(HSR6) 144-148 MHz Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	95 Ω, 100 MHz Long Ferrite Bead	2743021447	Fair-Rite
C1	6.8 μF, 50 V Chip Capacitor	C4532X7R1H685K	TDK
C3, C5, C7, C8, C9, C10, C11, C12, C13, C15	1000 pF Chip Capacitors	ATC100B102KT50XT	ATC
C4	5.6 pF Chip Capacitor	ATC100B5R6CT500XT	ATC
C6	470 pF Chip Capacitor	ATC100B471JT200XT	ATC
C14, C16	1 μF, 100 V Chip Capacitors	C3225JB2A105KT	TDK
C17	2.2 μF, 100 V Chip Capacitor	HMK432B7225KM-T	Taiyo Yuden
C18	470 μF, 100 V Electrolytic Capacitor	MCGPR100V477M16X32-RH	Multicomp
C19, C20	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
L1	43 nH Inductor	B10TJLC	Coilcraft
L2	7 Turn, #14 AWG, ID = 0.4″ Inductor	Handwound	Freescale
R1	11 Ω, 1/4 W Chip Resistor	CRCW120611R0FKEA	Vishay
T1	Balun	TUI-9	Comm Concepts
Coax1, Coax2	Flex Cables, 10.2 Ω, 4.7″	TC-12	Comm Concepts
Coax3	Coax Cable, 50 Ω, 6.7″	SUCOFORM250-01	Huber+Suhner
PCB	0.030”, ε_r = 3.50	TC-350	Arlon

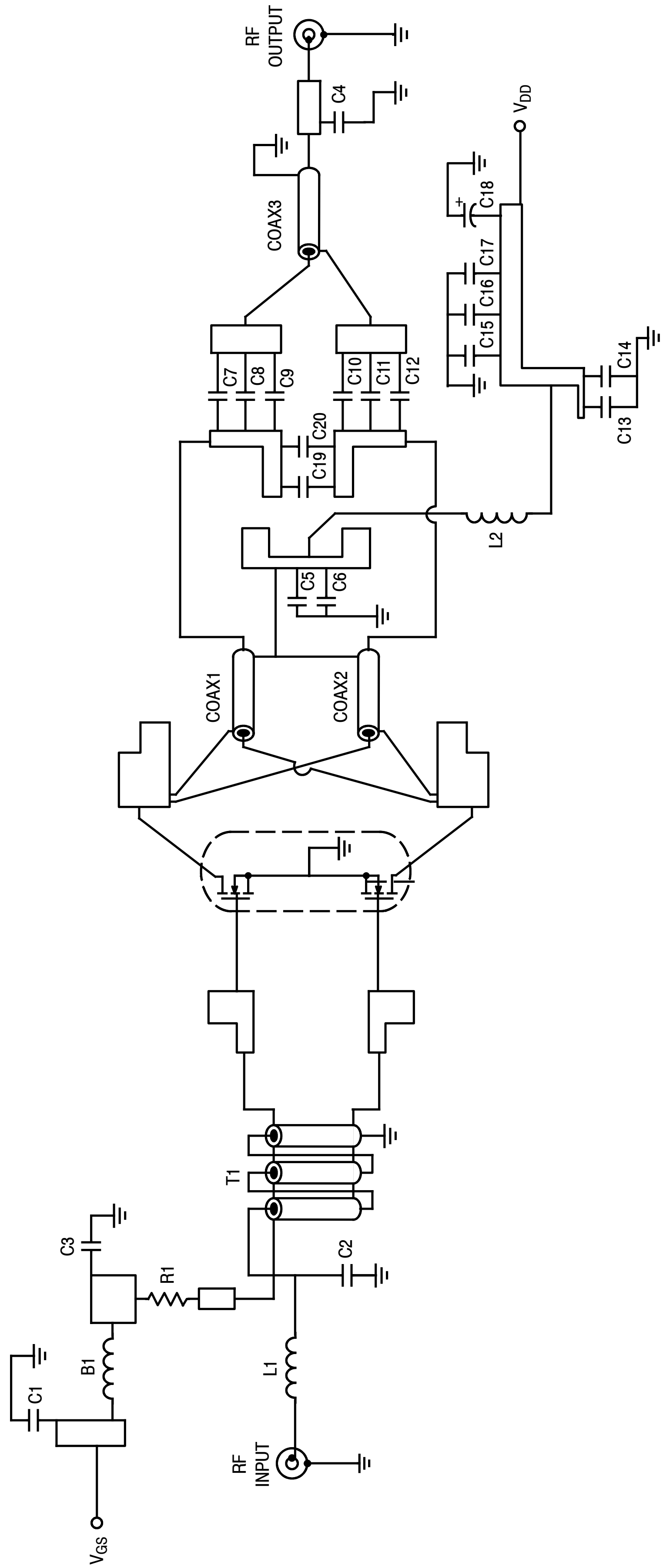


Figure 18. MRFE6VP61K25HR6(HSR6) 144-148 MHz Reference Circuit Schematic

V_{DD} = 50 Vdc, I_{DQ} = 200 mA, P_{out} = 1100 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
144	1.6 + j5.0	3.9 + j1.5

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

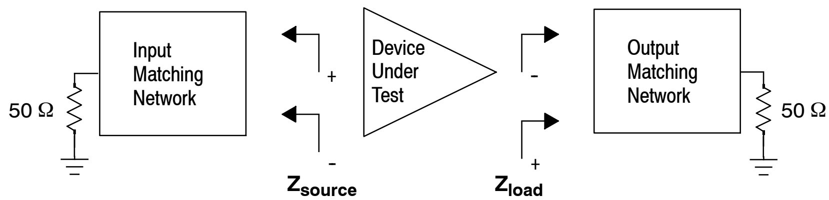


Figure 19. Series Equivalent 144-148 MHz Reference Circuit Source and Load Impedance

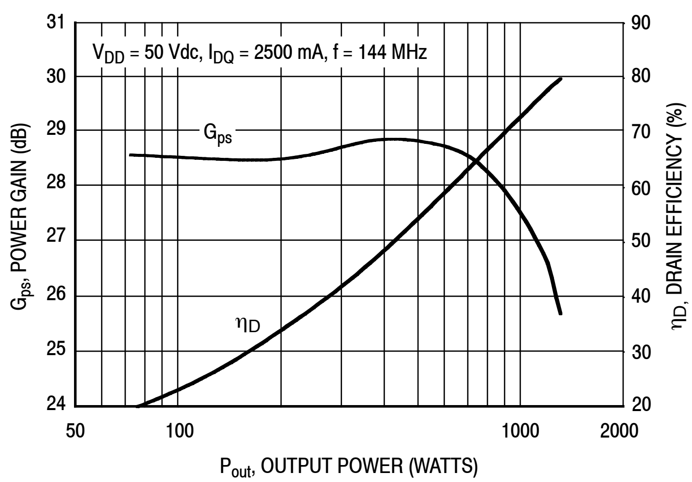


Figure 20. Power Gain and Drain Efficiency versus Output Power

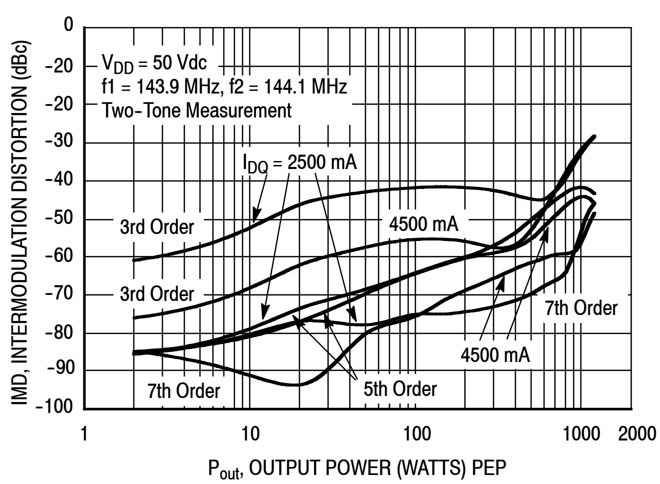
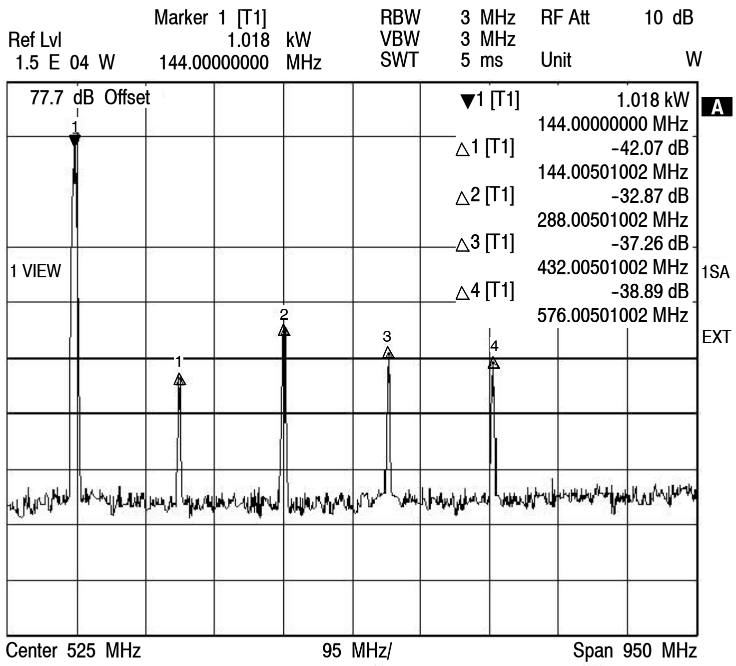


Figure 21. Intermodulation Distortion Products versus Output Power

HARMONIC MEASUREMENTS

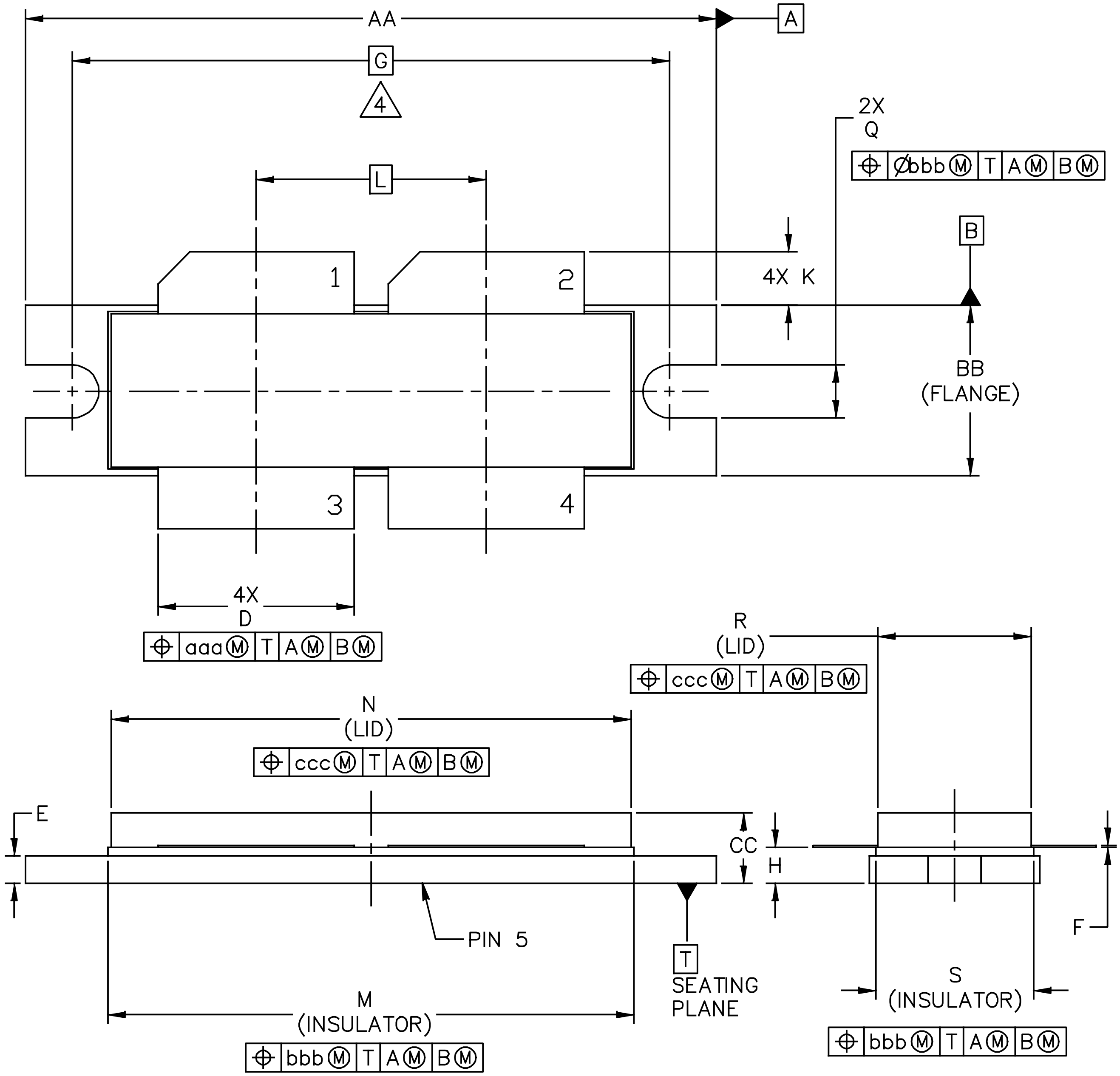


144 MHz, 1 kW

H2	H3	H4	H5
-42 dB	-33 dB	-37 dB	-39 dB

Figure 22. 144 MHz Harmonics @ 1 kW

PACKAGE DIMENSIONS



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	STANDARD: NON–JEDEC	
	28 FEB 2013	

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 INCH (38.61 MM) BASED ON M3 SCREW.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	1.615	1.625	41.02	41.28	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	Q	.120	.130	3.05	3.30
CC	.170	.190	4.32	4.83	R	.355	.365	9.02	9.27
D	.455	.465	11.56	11.81	S	.365	.375	9.27	9.53
E	.062	.066	1.57	1.68					
F	.004	.007	0.10	0.18					
G	1.400 BSC		35.56 BSC		aaa	.013		0.33	
H	.082	.090	2.08	2.29	bbb	.010		0.25	
K	.117	.137	2.97	3.48	ccc	.020		0.51	
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					

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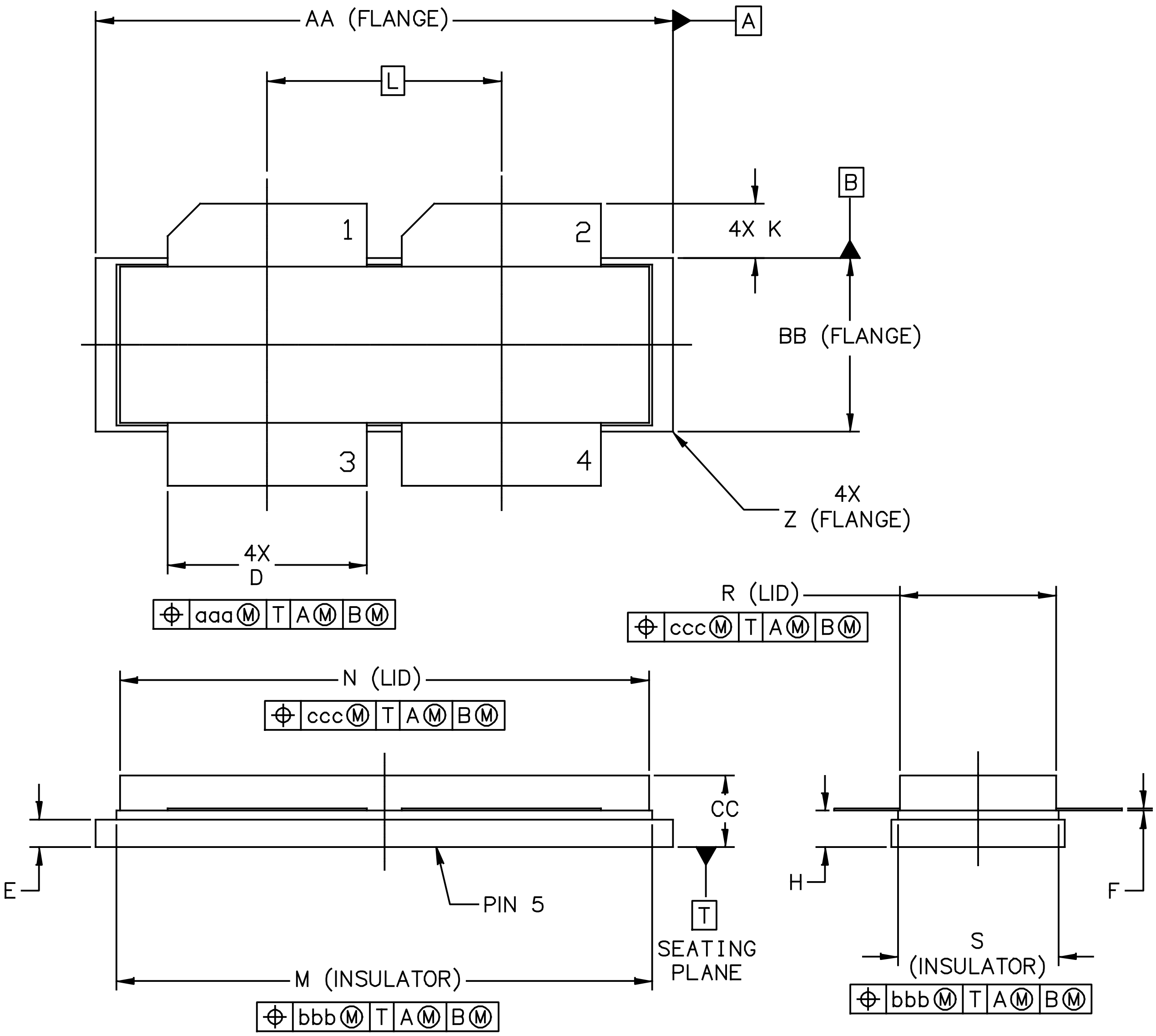

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	STANDARD: NON–JEDEC	
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NOTES:

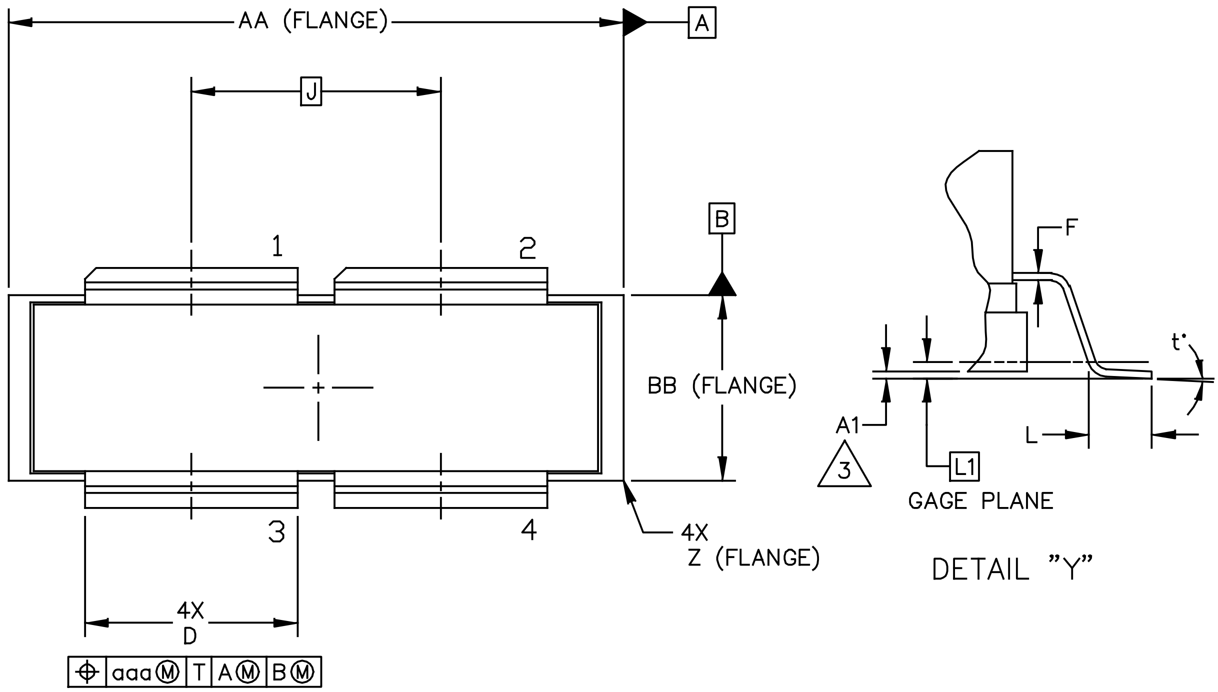
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

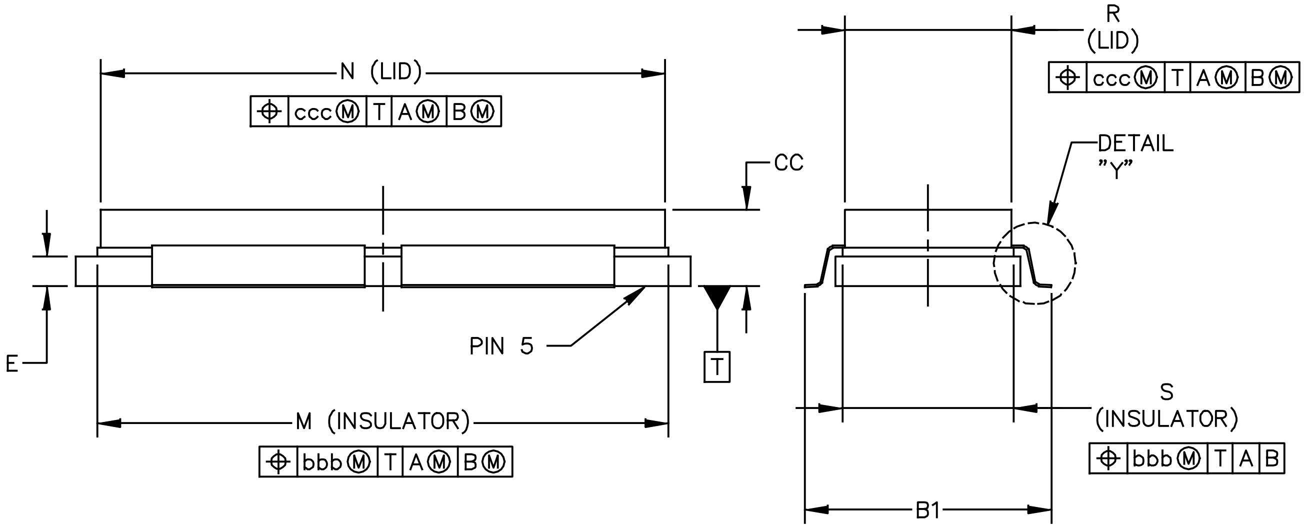
2. CONTROLLING DIMENSION: INCH

3. DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM PACKAGE BODY

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	R	.355	.365	9.02	9.27
BB	.395	.405	10.03	10.29	S	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	Z	R.000	R.040	R0.00	R1.02
D	.455	.465	11.56	11.81					
E	.062	.066	1.57	1.68	aaa	.013		0.33	
F	.004	.007	0.10	0.18	bbb	.010		0.25	
H	.082	.090	2.08	2.29	ccc	.020		0.51	
K	.117	.137	2.97	3.48					
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI–1230–4S	DOCUMENT NO: 98ARB18247C	REV: G
	STANDARD: NON–JEDEC	
		01 MAR 2013





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	STANDARD: NON-JEDEC	
	07 MAR 2013	

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	R	.355	.365	9.02	9.27
A1	−.001	.011	−0.03	0.28	S	.365	.375	9.27	9.53
BB	.395	.405	10.03	10.29	Z	R.000	R.040	R0.00	R1.02
B1	.564	.574	14.32	14.58	t°	0°	8°	0°	8°
CC	.170	.190	4.32	4.83					
D	.455	.465	11.56	11.81	aaa	.013		0.33	
E	.062	.066	1.57	1.68	bbb	.010		0.25	
F	.004	.007	0.10	0.18	ccc	.020		0.51	
J	.540 BSC		13.72 BSC						
L	.038	.046	0.97	1.17					
L1	.01 BSC		0.25 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI−1230−4S GULL	DOCUMENT NO: 98ASA00459D	REV: A
	STANDARD: NON−JEDEC	
		07 MAR 2013

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2010	• Initial Release of Data Sheet
1	Jan. 2011	• Fig. 1, Pin Connections, corrected pin 4 label from RF_{out}/V_{GS} to RF_{in}/V_{GS}, p. 1
2	May 2012	• Added Application Circuits Typical Performance table, p. 1 • Capable of Handling VSWR bullet: corrected 1250 Peak Output Power value to 1500 and converted to table, p. 1, 3 • Table 1, Max Ratings: final DC test specification for Drain-Source Voltage changed from +125 to +133 Vdc, p. 2 • Table 3, ESD Protection Characteristics: added the device's ESD passing level as applicable to each ESD class, p. 2 • Table 4, Off Characteristics: final DC test specification for Drain-Source Breakdown Voltage minimum value changed from 125 to 133 Vdc, p. 2 • Table 4, On Characteristics: added Forward Transconductance, p. 2 • Fig. 10, MTTF versus Junction Temperature - CW: MTTF end temperature on graph changed to match maximum operating junction temperature, p. 7 • Added Fig. 12, Source and Load Impedances Optimized for IRL, Power and Efficiency — Push-pull, p. 8 • Added Fig. 13, 87.5-108 MHz FM Broadcast Reference Circuit Component Layout, p. 9 • Added Table 9, 87.5-108 MHz FM Broadcast Reference Circuit Component Designations and Values, p. 9 • Added Fig. 14, 87.5-108 MHz FM Broadband Reference Circuit Schematic, p. 10 • Added Fig. 15, Power Gain and Drain Efficiency versus Output Power (87.5-108 MHz), p. 11 • Added Fig. 16, Series Equivalent 87.5-108 MHz FM Broadcast Reference Circuit Source and Load Impedance, p. 11 • Added Fig. 17, 144-148 MHz Reference Circuit Component Layout, p. 12 • Added Table 9, 144-148 MHz Reference Circuit Component Designations and Values, p. 12 • Added Fig. 18, 144-148 MHz Reference Circuit Schematic, p. 13 • Added Fig. 19, Series Equivalent 144-148 MHz Reference Circuit Source and Load Impedance, p. 14 • Added Fig. 20, Power Gain and Drain Efficiency versus Output Power (144-148 MHz), p. 14 • Added Fig. 21, Intermodulation Distortion Products versus Output Power (144-148 MHz), p. 14 • Added Fig. 22, 144 MHz Harmonics @ 1 kW, p. 15
3	Oct. 2012	• Added part number MRFE6VP61K25GSR5, p. 1 • Added 2282-02 (NI-1230S-4 Gull) package isometric, p. 1, and Mechanical Outline, p. 20, 21
4	Mar. 2013	• MRFE6VP61K25HR6 tape and reel option replaced with MRF6VP61K25HR5 per PCN15551. • Replaced Case Outline 98ASB16977C, Issue E with Issue F, p. 16, 17. Changed dimension C from 0.150″-0.200″ to CC 0.170″-0.190″. • Replaced Case Outline 98ARB18247C, Issue F with Issue G, p. 18, 19. Changed dimension C from 0.150″-0.200″ to CC 0.170″-0.190″. Added minimum Z dimension R0.00″. • Replaced Case Outline 98ASA00459D, Issue O with Issue A, p. 20, 21. Changed dimension C from 0.150″-0.200″ to CC 0.170″-0.190″. Corrected positional tolerance for dimension S.

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