Integrated Circuit Systems, Inc.

M2041

VCSO Based Clock PLL with AutoSwitch

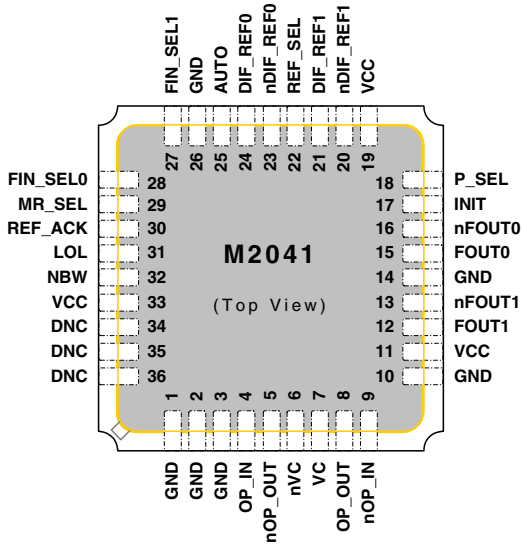
General Description

The M2041 is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL. It is designed for clock protection, frequency translation and jitter attenuation in optical networking systems supporting 2.5-10Gb data rates. It features dual differential inputs with two modes of input selection: manual and automatic upon clock failure. The clock multiplication ratios and output divider ratio are pin selectable. External loop components allow the tailoring of PLL loop response.

Features

- Integrated SAW (surface acoustic wave) delay line; output frequencies of 125 to 700 MHz; * outputs VCSO frequency or 1/4; pin-configurable dividers
- Loss of Lock (LOL) indicator output
- Narrow Bandwidth control input (NBW pin); Initialization (INIT) input overrides NBW at power-up
- Dual reference clock inputs support LVDS, LVPECL, LVCMOS, LVTTL
- AutoSwitch (AUTO pin) - automatic (non-revertive) reference clock reselection upon clock failure; Hitless Switching (HS) options with or without Phase Build-out (PBO) enable SONET (GR-253) /SDH (G.813) MTIE and TDEV compliance
- Acknowledge pin (REF_ACK pin) indicates the actively selected reference input
- Dual differential LVPECL outputs
- Low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)
- Single 3.3V power supply
- Small 9 x 9 mm SMT (surface mount) package

Pin Assignment (9 x 9 mm SMT)



Example I/O Clock Frequency Combinations Using M2041-11-622.0800

Input Reference Clock (MHz)	PLL Ratio (Pin Selectable)	Output Clock (MHz) (Pin Selectable)
19.44	32	622.08 or 155.52
77.76	8	
155.52	4	
622.08	1	

* Specify VCSO center frequency at time of order.

Simplified Block Diagram