APPLICATION NOTE

ATA6661/ATA6662/ATA6662C Development Board

ATA6661/ATA6662

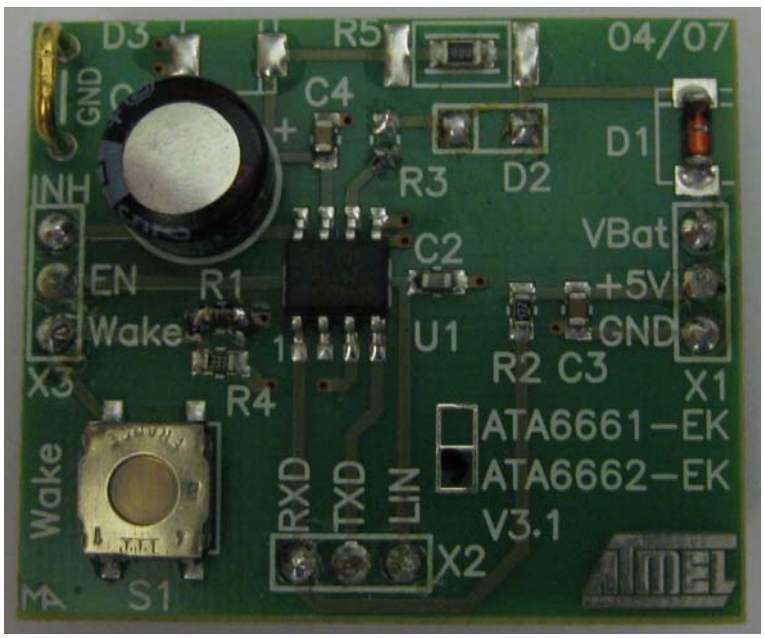
Introduction

The development board for the Atmel® ATA6661/ATA6662 (ATA6661-EK, ATA6662-EK) is designed to give designers a quick start with these ICs and for the prototyping and testing of new designs. The Atmel ATA6661/ATA6662 is a fully integrated LIN transceiver complying with the LIN 2.x specification. The Atmel ATA6661 and Atmel ATA6662 are pin and function compatible, but the Atmel ATA6662 has improved EMC behavior.

The IC interfaces between the LIN protocol handler and the physical layer, and is designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control on the LIN bus ensures secure data communication up to 20Kbaud with a RC oscillator for the protocol handling. The bus output is capable of withstanding high voltage and complies with the 42V powernet requirements. Sleep mode guarantees minimal current consumption.

This document has been developed to give the user an quick start with the development board of the Atmel ATA6661/ATA6662. For more detailed information about the use of the Atmel ATA6661/ATA6662 itself, please refer to the corresponding datasheet.

Figure 1. Atmel ATA6661/ATA6662 Development Board



Development Board Features

The development board for the Atmel® ATA6661/ATA6662 supports the following features:

- Includes all components necessary for ATA6661/ATA6662 operation
- All pins are easily accessible
- Can be used for master or slave operation
- Wake-up pulse via an on-board switch
- 24V application can be built up on the board

Quick Start

The development board for the Atmel ATA6661/ATA6662 is shipped with all components necessary to start with the development of a LIN slave node immediately.

Connecting an external 12V DC power supply between the terminals VBAT and GND puts the IC in the pre-normal mode. In this mode, the inhibit pin INH will be switched to the VS level in order to enable an external voltage regulator (not included on the board). The LIN pin is in the recessive state.

Please note that the communication is still inactive during pre-normal mode.

In order to communicate via the LIN bus interface, you have to switch to normal mode by applying 5V at pin EN.

As RXD is an open-drain output, the necessary pull-up resistor can be activated by applying a +5V DC voltage, for example at pin +5V on the board.

1. Hardware Description

In the following sections only the normal operating conditions will be described. For detailed information concerning the mentioned features, refer to the corresponding datasheet.

1.1 Power Supply (VBAT, +5V and GND)

The development board requires an external 5.7V to 18V DC power supply between the terminals VBAT and GND. The input circuit is protected against inverse-polarity with the protection diode D1, so that there is normally a difference between the VBAT and VS level of approximately 0.7V.

The DC voltage at pin +5V is only needed when the pull-up resistor for the pin RXD is to be activated.

1.2 LIN Interface (LIN, TXD and RXD)

1.2.1 Bus Pin (LIN)

A low-side driver with internal current limitation, thermal shutdown, and an internal pull-up resistor in compliance with LIN spec 2.0 is implemented. LIN receiver thresholds are compatible to the LIN protocol specification.

On the board at the LIN pin there is a 220-pF capacitor to ground. Additionally, the two extra components (diode D2 (LL4148) in series with resistor R3 (1 kΩ)) necessary to use the development board for a LIN master application have designated placeholders for convenient mounting.

1.2.2 Input Pin (TXD)

This pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to have the LIN bus low. If TXD is high, the LIN output transistor is turned off and the bus is in the recessive state, pulled up by the internal resistor. If TXD is low, the LIN output transistor is turned on and the bus is in the dominant state. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 20 ms, the LIN bus driver is switched to the recessive state.

1.2.3 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD, LIN low (dominant state) is reported by a low level at RXD. The output is short-circuit protected.

Please note that the Atmel® ATA6661/ATA6662 has to be in normal mode in order to have the communication via LIN enabled.

1.3 System Control (EN, INH and WAKE)

1.3.1 Enable Pin (EN)

This pin controls the operation mode of the interface. If EN = 1 the interface is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. If EN = 0 the device is switched to sleep mode and no transmission is possible.

1.3.2 Inhibit Pin (INH)

This pin is used to control an external switchable voltage regulator having an inhibit input. The inhibit pin is a high-side switch structure connected to VS. If the device is in normal mode, the inhibit high-side switch is turned on and the external voltage regulator is activated. When the device is in sleep mode, the inhibit switch is turned off and the external voltage regulator will be disabled.

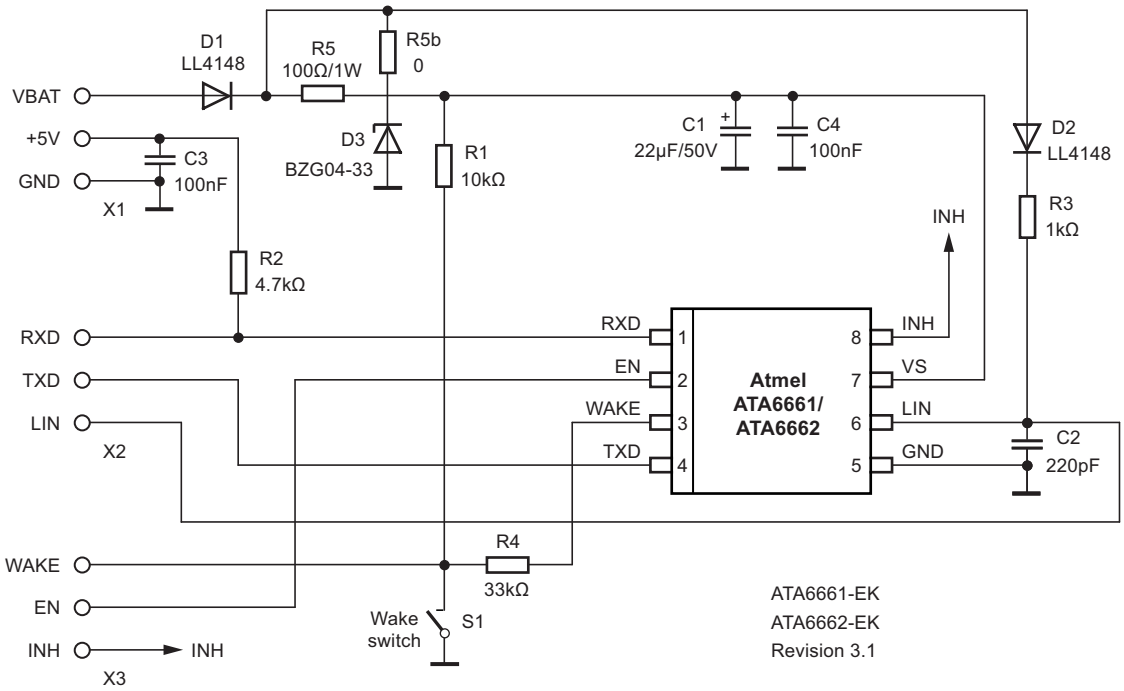
1.3.3 Wake Pin (WAKE)

This pin is a high voltage input used to wake the device up from sleep mode. It is usually connected to an external switch in order to generate a local wake-up.

If no local wake-up is needed in the application, the WAKE pin should be connected directly to the VS pin.

2. Schematic and Layout of the ATA6661/ATA6662 Development Board

Figure 2-1. Schematic of the Development Board for the Atmel ATA6661/ATA6662



Notes: 1. D2 and R3 are only necessary for a master node.

2. R5 and D3 are only used in 24V applications. They guarantee that the supply voltage VS never exceeds the maximum rating of VS_{max} = 40V. Refer to the corresponding application note of the Atmel® ATA6661 for further information.

Figure 2-2. Board Component Placement; Top Side, Top View

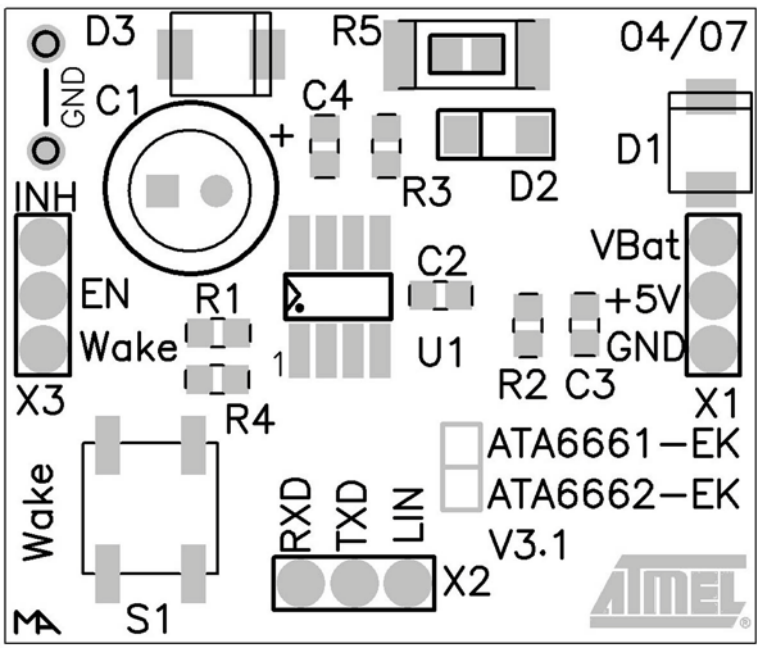


Figure 2-3. Atmel ATA6661/ATA6662 Development Board; Top Side, Top View

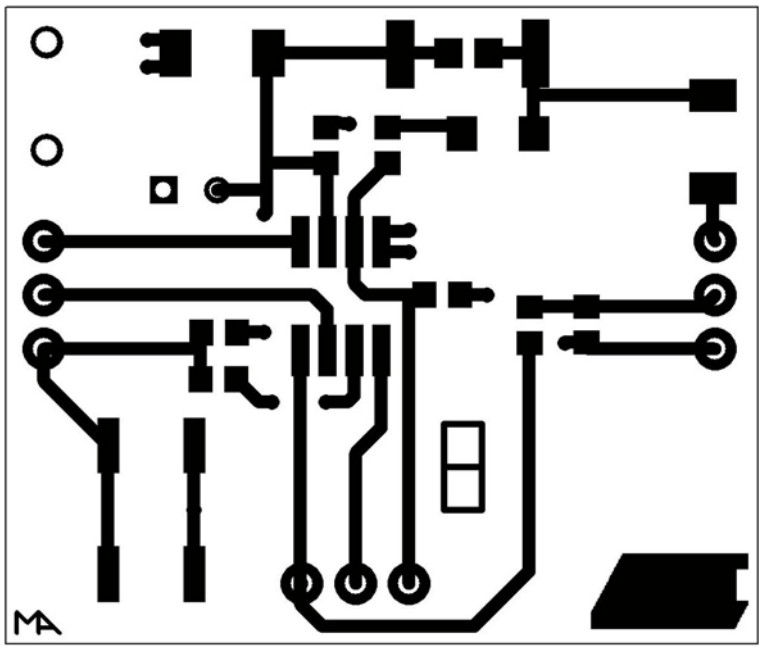
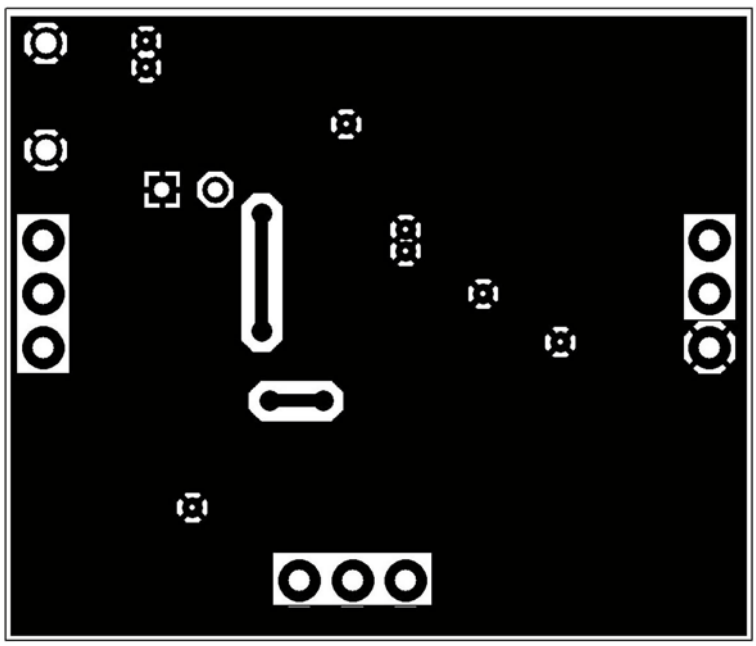


Figure 2-4. Atmel ATA6661/ATA6662 Development Board; Bottom Side, Top View (as if PCB Were Transparent)



3. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4968D-AUTO-06/15	• Put document in the latest template
4968C-AUTO-05/11	• Section 1 “Introduction” on page 1 updated • Section 3 “Schematic and Layout of the ATA6661/ATA6662 Development Board on pages 5 to 7 updated
4968B-AUTO-03/11	• C version on page 1 added

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