DS2251T
128k Soft Microcontroller Module

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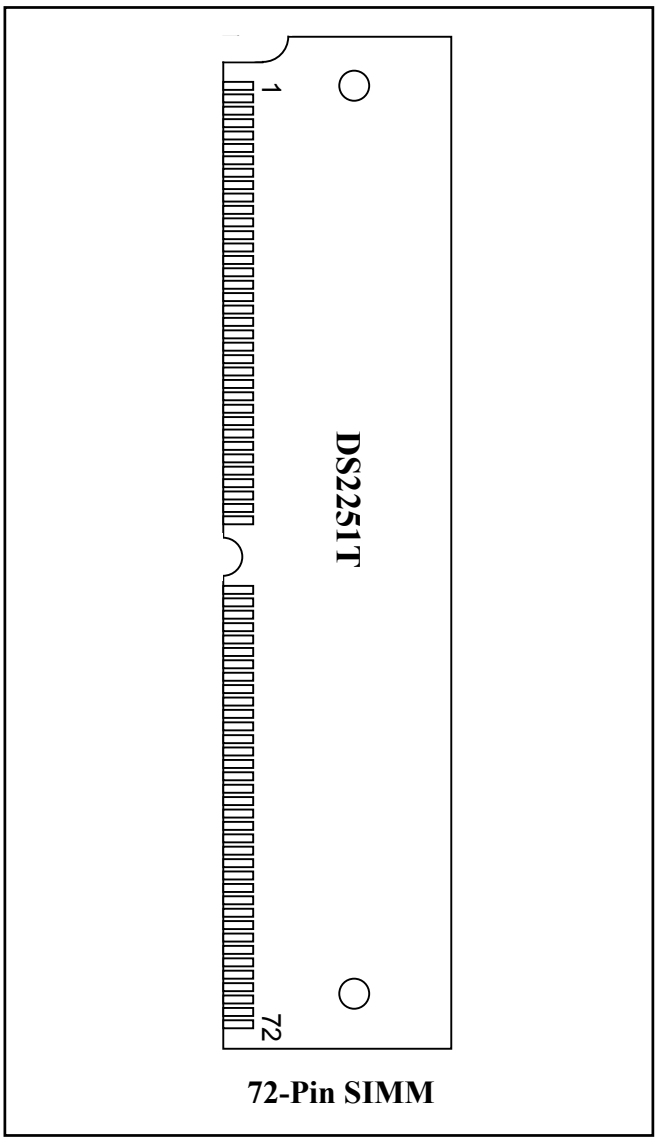
FEATURES

- **8051-Compatible Microcontroller Adapts to Its Task**
  - 32, 64, or 128kbytes of Nonvolatile SRAM for Program and/or Data Storage
  - In-System Programming via On-Chip Serial Port
  - Capable of Modifying its Own Program or Data Memory in the End System
  - Provides Separate Byte-Wide Bus for Peripherals
  - Performs CRC-16 Check of NV RAM Memory
- **High-Reliability Operation**
  - Maintains All Nonvolatile Resources Up to 10 Years in the Absence of V_{CC} at Room Temperature
  - Power-Fail Reset
  - Early Warning Power-fail Interrupt
  - Watchdog Timer
  - Lithium Backed Memory Remembers System State
  - Precision Reference for Power Monitor
- **Fully 8051-Compatible**
  - 128 Bytes Scratchpad RAM
  - Two Timer/Counters
  - On-Chip Serial Port
  - 32 Parallel I/O Port Pins
- **Permanently Powered Real-Time Clock**

PIN CONFIGURATION



72-Pin SIMM

DESCRIPTION

The DS2251T 128k soft microcontroller module is an 8051-compatible microcontroller module based on nonvolatile RAM technology. It is designed for systems that need large quantities of nonvolatile memory. Like other members of the secure microcontroller family, it provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program, then reprogram the microcontroller while in-system. The application software can even change its own operation. This allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NV RAM, the DS2251T is ideal for data logging applications. The powerful real-time clock includes interrupts for time stamp and date. It keeps time to one-hundredth of seconds using its on-board 32kHz crystal.

The DS2251T provides the benefits of NV RAM without using I/O resources. Between 32 kbytes and 128 kbytes of onboard NV RAM are available. A non-multiplexed Byte-wide address and data bus is used for memory access. This bus, which is available at the connector, can perform all memory access and also provide decoded chip enables for off-board memory mapped peripherals. This leaves the 32 I/O port pins free for application use.

The DS2251T provides high-reliability operation in portable systems or systems with unreliable power. These features include the ability to save the operating state, Power-fail Reset, Power-fail Interrupt, and Watchdog Timer. All nonvolatile memory and resources are maintained for over 10 years at room temperature in the absence of power.

A user loads programs into the DS2251T via its on-chip serial Bootstrap loader. This function supervises the loading of software into NV RAM, validates it, then becomes transparent to the user. Software is stored in onboard CMOS SRAM. Using its internal Partitioning, the DS2251T can divide a common RAM into user-selectable program and data segments. This Partition can be selected at program loading time, but can be modified anytime later. The microprocessor will decode memory access to the SRAM, access memory via its Byte-wide bus and write-protect the memory portion designated as program (ROM).

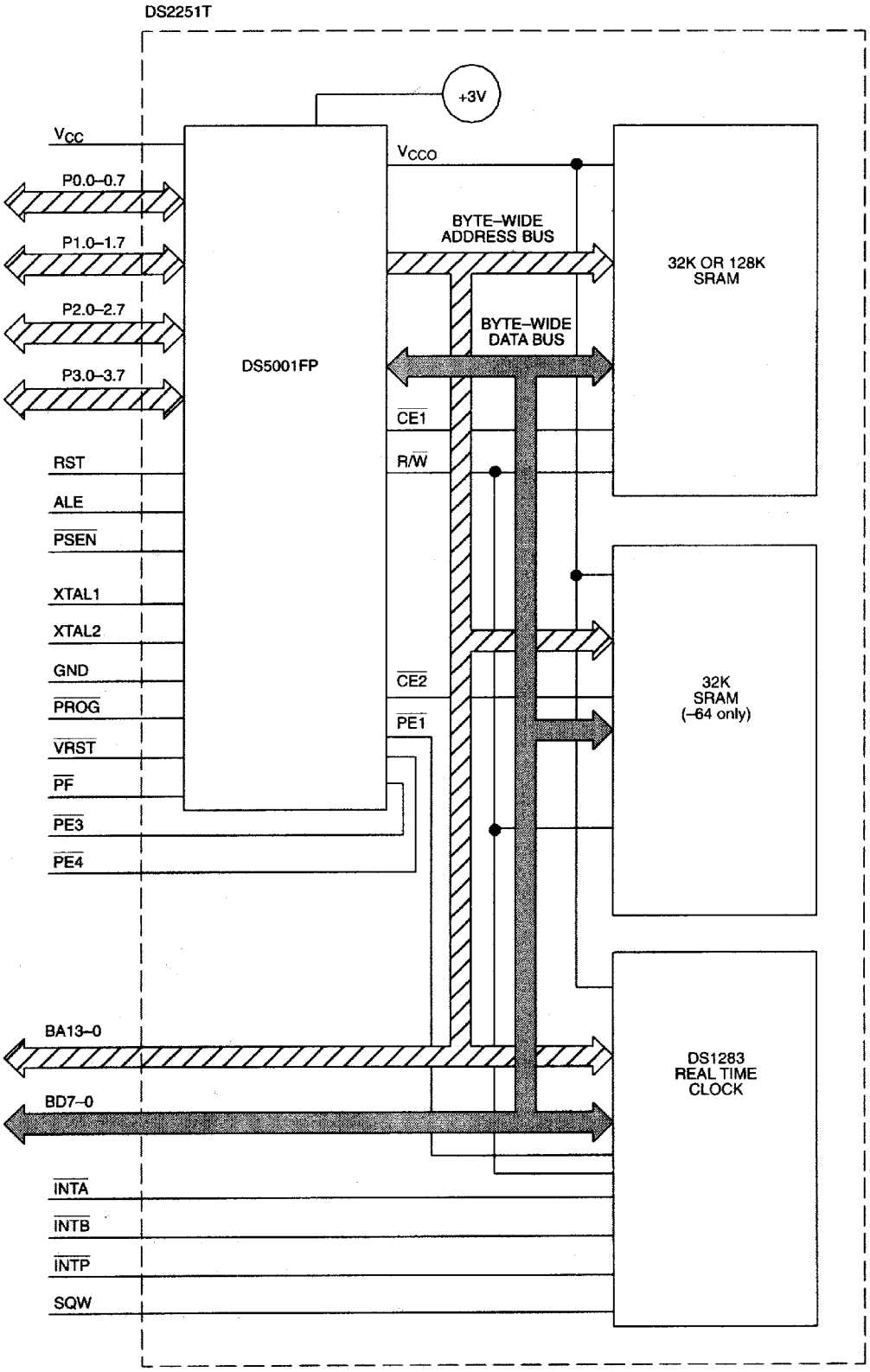
Operating information is contained in the Secure Microcontroller User's Guide. This data sheet provides ordering information, pinout, and electrical specifications.

ORDERING INFORMATION

PART	RAM SIZE (kB)	MAX CRYSTAL SPEED (MHz)	TIMEKEEPING?
DS2251T-32-16	32	16	Yes
DS2251T-32-16#	32	16	Yes
DS2251T-64-16	64	16	Yes
DS2251T-64-16#	64	16	Yes
DS2251T-128-16	128	16	Yes
DS2251T-128-16#	128	16	Yes

Denotes a RoHS-compliant package that may contain lead exempt under the RoHS requirements.

DS2251T BLOCK DIAGRAM Figure 1



PIN ASSIGNMENT

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	P1.0	19	XTAL2	37	P0.2	55	$\overline{\text{INTB}}$
2	P1.1	20	GND	38	P0.1	56	BD0
3	P1.2	21	P2.0	39	P0.0	57	BD1
4	P1.3	22	P2.1	40	V_{CC}	58	BD2
5	P1.4	23	P2.2	41	BA0	59	BD3
6	P1.5	24	P2.3	42	BA1	60	BD4
7	P1.6	25	P2.4	43	BA2	61	BD5
8	P1.7	26	P2.5	44	BA3	62	BD6
9	RST	27	P2.6	45	BA4	63	BD7
10	P3.0/RXD	28	P2.7	46	BA5	64	R/$\overline{\text{W}}$
11	P3.1/TXD	29	$\overline{\text{PSEN}}$	47	BA6	65	$\overline{\text{PF}}$
12	P3.2/$\overline{\text{INT0}}$	30	ALE	48	BA7	66	$\overline{\text{PE3}}$
13	P3.3/$\overline{\text{INT1}}$	31	$\overline{\text{PROG}}$	49	BA8	67	$\overline{\text{PE4}}$
14	P3.4/T0	32	P0.7	50	BA9	68	$\overline{\text{INTP}}$
15	P3.5/T1	33	P0.6	51	BA10	69	$\overline{\text{INTA}}$
16	P3.6/$\overline{\text{WR}}$	34	P0.5	52	BA11	70	SQW
17	P3.7/$\overline{\text{RD}}$	35	P0.4	53	BA12	71	$\overline{\text{VRST}}$
18	XTAL1	36	P0.3	54	BA13	72	BA15

PIN DESCRIPTION

PIN	DESCRIPTION
39–32	**P0.0–P0.7.** General-purpose I/O Port 0. This port is open-drain and cannot drive a logic 1. It requires external pullups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pullups.
1–8	**P1.0–P1.7.** General-purpose I/O Port 1.
21–28	**P2.0–P2.7.** General-purpose I/O Port 2. Also serves as the MSB of the Expanded Address bus.
10	**P3.0/RXD.** General-purpose I/O port pin 3.0. Also serves as the receive signal for the on-board UART. This pin should **NOT** be connected directly to a PC COM port.
11	**P3.1/TXD.** General-purpose I/O port pin 3.1. Also serves as the transmit signal for the on-board UART. This pin should **NOT** be connected directly to a PC COM port.
12	**P3.2/$\overline{\text{INT0}}$.** General-purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
13	**P3.3/$\overline{\text{INT1}}$.** General-purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
14	**P3.4/T0.** General-purpose I/O port pin 3.4. Also serves as the Timer 0 input.

PIN	DESCRIPTION
15	**P3.5/T1.** General-purpose I/O port pin 3.5. Also serves as the Timer 1 input.
16	**P3.6/$\overline{\text{WR}}$.** General-purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
17	**P3.7/$\overline{\text{RD}}$.** General-purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
9	**RST.** Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally, can be left unconnected if not used. An RC power-on reset circuit is not needed and is **NOT** recommended.
29	$\overline{\text{PSEN}}$ **.** Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used.
30	**ALE.** Address Latch Enable. Used to de-multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a ‘373 type transparent latch.
19, 18	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
20	**GND.** Logic ground.
40	**V_{CC}. +5V**
72	**BA15.** Monitor test point to reflect the logical value of A15. Not needed for memory access.
54–41	**BA13–BA 0.** Byte-wide Address bus bits 13–0. This bus is combined with the non-multiplexed data bus (BD7–BD0) to access onboard NV SRAM and off-board peripherals. Peripheral decoding is performed using $\overline{\text{PE3}}$ and $\overline{\text{PE4}}$. These are on 16k boundaries, so BA14 or BA15 are not needed. Read/write access is controlled by R/$\overline{\text{W}}$. BA13–BA0 connect directly to memory-mapped peripherals.
63–56	**BD7–BD0.** Byte-wide Data Bus Bits 7–0. This 8-bit bi-directional bus is combined with the non-multiplexed address bus (BA14–BA0) to access on-board NV SRAM and off-board peripherals.
64	**R/$\overline{\text{W}}$.** Read/Write. This signal provides the write enable to the SRAMs on the Byte-wide bus. It is controlled by the memory map and Partition. The blocks selected as Program (ROM) will be write-protected. This signal is also used for the write enable to off-board peripherals.
66	$\overline{\text{PE3}}$ **.** Peripheral Enable 3. Accesses data memory between addresses 8000h and BFFFh when the PES bit is set to a logic 1. $\overline{\text{PE3}}$ is not lithium backed and can be connected to any type of peripheral function.
67	$\overline{\text{PE4}}$ **.** Peripheral Enable 4. Accesses data memory between addresses C000h and FFFFh when the PES bit is set to a logic 1. $\overline{\text{PE4}}$ is not lithium backed and can be connected to any type of peripheral function.
31	$\overline{\text{PROG}}$ **.** Invokes the Bootstrap loader on a falling edge. This signal should be debounced so that only one edge is detected. If connected to ground, the micro will enter Bootstrap loading on power-up. This signal is pulled up internally.

PIN	DESCRIPTION
71	**$\overline{\text{VRST}}$.** This I/O pin (open-drain with internal pullup) indicates that the power supply (V_{CC}) has fallen below the V_{CCMIN} level and the micro is in a reset state. When this occurs, the DS2251T will drive this pin to a logic 0. Because the micro is lithium backed, this signal is guaranteed even when V_{CC} = 0V. Because it is an I/O pin, it will also force a reset if pulled low externally. This allows multiple parts to synchronize their power-down resets.
65	**$\overline{\text{PF}}$.** This output goes to a logic 0 to indicate that the micro has switched to lithium backup. It corresponds to $V_{CC} < V_{LI}$. Because the micro is lithium backed, this signal is guaranteed even when V_{CC} = 0V.
55	**$\overline{\text{INTB}}$.** $\overline{\text{INTB}}$ from the real-time clock. This output may be connected to a micro interrupt input.
68	**$\overline{\text{INTP}}$.** $\overline{\text{INTP}}$ from the real-time clock. This open-drain output requires a pullup and may be connected to a micro interrupt input.
69	**$\overline{\text{INTA}}$.** $\overline{\text{INTA}}$ from the real-time clock. This output may be connected to a micro interrupt input.
70	**SQW.** Square-wave output from the DS1283 real-time clock. Can be programmed to output a 1024Hz square wave.

INSTRUCTION SET

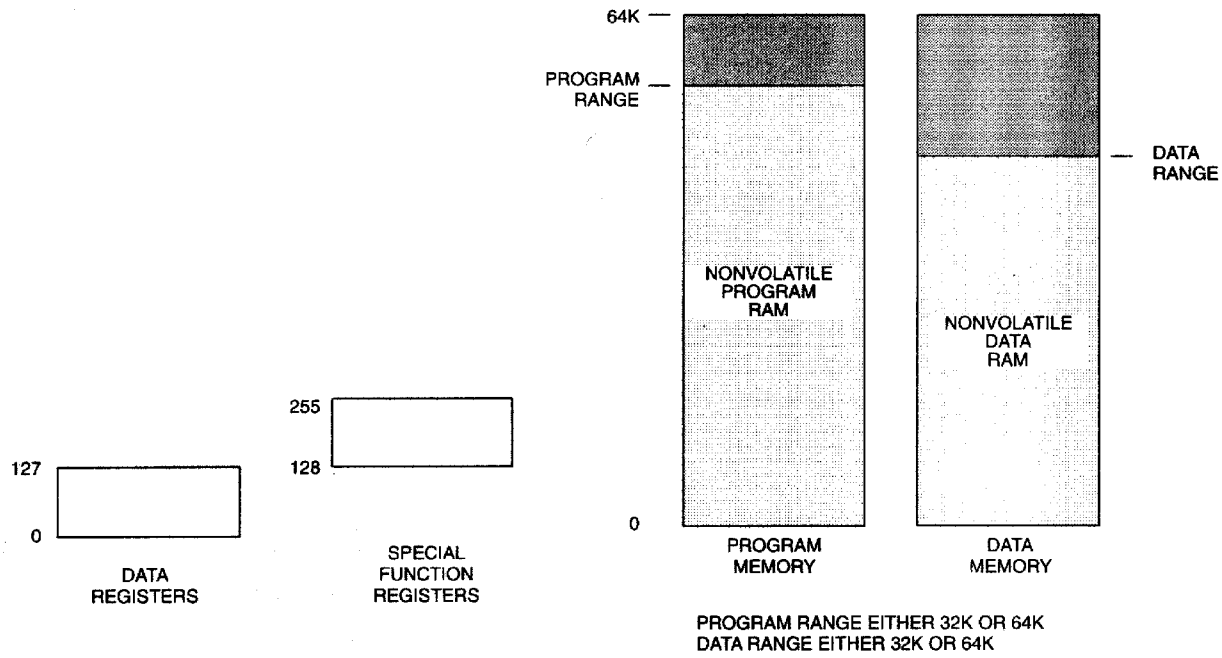
The DS2251T executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS2251T.

A complete description of the instruction set and operation are provided in the Secure Microcontroller User's Guide.

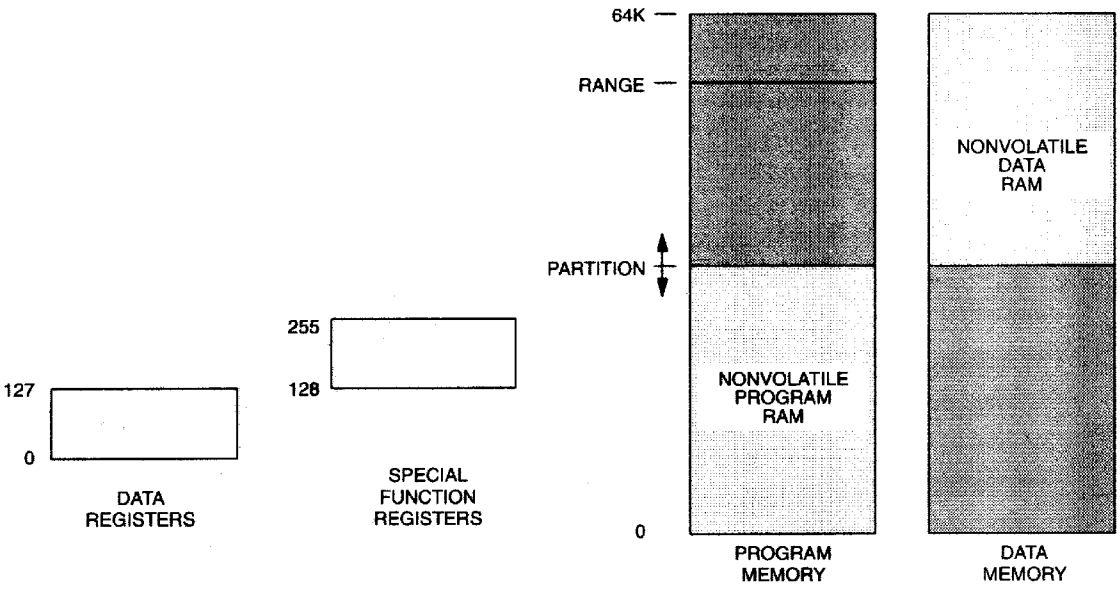
MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS2251T. The entire 64k of program and 64k of data are available to the byte-wide bus. This preserves the I/O ports for application use. The user controls the portion of memory that is actually mapped to the byte-wide bus by selecting the Program Range and Data Range. Any area not mapped into the NV RAM is reached via the Expanded bus on Ports 0 and 2. An alternate configuration allows dynamic Partitioning of a 64k space as shown in Figure 3. Selecting PES = 1 provides access to the real-time clock on the DS2251T and enables $\overline{\text{PE3}}$ and $\overline{\text{PE4}}$ for peripheral access as shown in Figure 4. These selections are made using Special Function Registers. The memory map and its controls are covered in detail in the Secure Microcontroller User's Guide.

DS2251T MEMORY MAP IN NON-PARTITIONABLE MODE (PM = 1) Figure 2



DS2251T MEMORY MAP IN PARTITIONABLE MODE (PM = 0) Figure 3



NOTE: PARTITIONABLE MODE IS NOT SUPPORTED IN 128KB MODE.

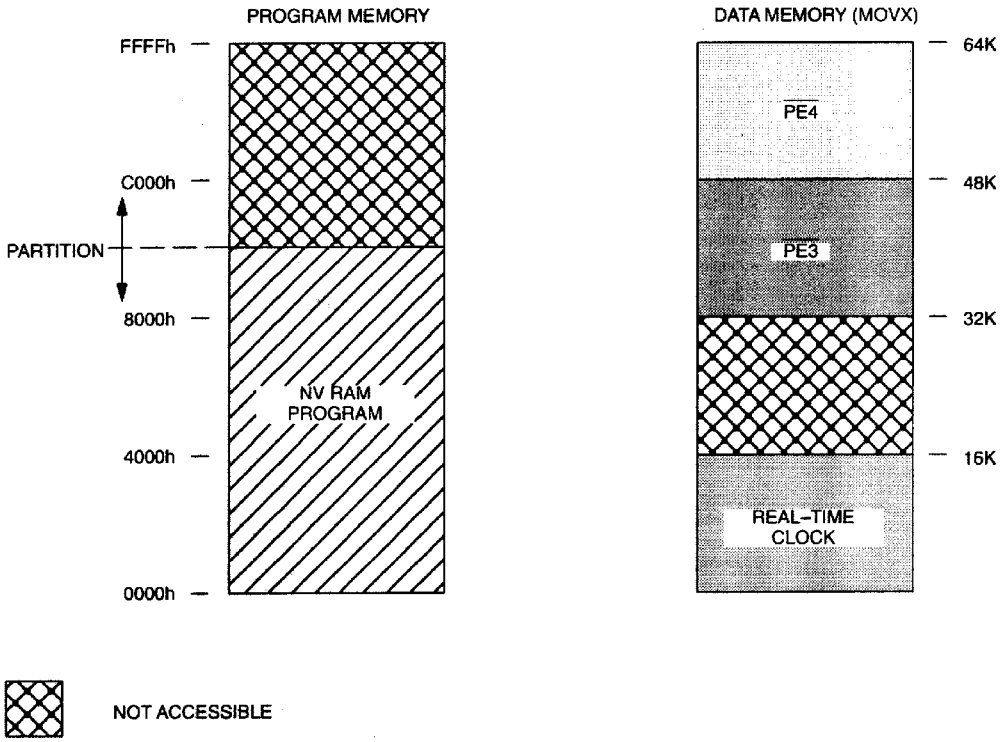
LEGEND:

= ON–CHIP REGISTERS

= ACCESSED VIA BYTEWIDE BUS

= ACCESSED VIA EXPANDED BUS (PORTS 0 AND 2)

DS2251T MEMORY MAP WITH (PES = 1) Figure 4



POWER MANAGEMENT

The DS2251T monitors V_{CC} to provide power-fail reset, early warning power-fail interrupt, and switchover to lithium backup. It uses an internal band-gap reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI}, respectively. When V_{CC} drops below V_{PFW}, the DS2251T will perform an interrupt vector to location 2Bh if the power-fail warning is enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS2251T invokes a reset state. No further code execution will be performed unless power rises back above V_{CCMIN}. All decoded chip enables and the R/$\overline{W}$ signal go to an inactive (logic 1) state. The $\overline{VRST}$ signal will be driven to a logic 0. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry will switch to the built-in lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. $\overline{PF}$ will be driven to a logic 0. The Secure Microcontroller User's Guide has more information on this topic. The trip points V_{CCMIN} and V_{PFW} are listed in the electrical specifications.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……...-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground…….-0.3V to +6.0V
Operating Temperature Range……-40°C to +85°C
Storage Temperature (**Note 1**)……..-55°C to +125°C
Soldering Temperature……+260°C for 10 seconds

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Note 1: Storage temperature is defined as the temperature of the device when V_{CC} = 0V and V_{LI} = 0V. In this state the contents of SRAM are not battery backed and are undefined.

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	-0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC}+0.3	V	1
Input High Voltage RST, XTAL1 $\overline{PROG}$	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage at I_{OL} = 1.6mA (Ports 1, 2, 3, $\overline{PF}$)	V_{OL1}		0.15	0.45	V	1, 7
Output Low Voltage at I_{OL} = 3.2mA (Ports 0, ALE, $\overline{PSEN}$, BA13:BA0, BD7:BD0, R/$\overline{W}$, $\overline{PE3}$:$\overline{PE4}$)	V_{OL2}		0.15	0.45	V	1
Output High Voltage at I_{OH} = -80µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage at I_{OH} = -400µA (Ports 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA13:BA0, BD7:BD0, R/$\overline{W}$, $\overline{PE3}$:$\overline{PE4}$)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN} = 0.45V (Ports 1, 2, 3)	I_{IL}			-50	µA	
Transition Current; 1 to 0 V_{IN} = 2.0V (Ports 1, 2, 3)	I_{TL}			-500	µA	
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0)	I_{IL}			±10	µA	
RST Pulldown Resistor	R_{RE}	40		150	kΩ	
$\overline{VRST}$ Pullup Resistor	R_{VR}		4.7		kΩ	
$\overline{PROG}$ Pullup Resistor	R_{PR}		40		kΩ	
Power-Fail Warning Voltage	V_{PFW}	4.25	4.37	4.50	V	1
Minimum Operating Voltage	$V_{CC(MIN)}$	4.00	4.12	4.25	V	1
Operating Current at 16MHz	I_{CC}			45	mA	2

DC CHARACTERISTICS (continued)

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Idle Mode Current at 12MHz		I_{IDLE}			7.0	mA	3
Stop Mode Current		I_{STOP}			80	µA	4
Pin Capacitance		C_{IN}			10	pF	5
Reset Trip Point in Stop Mode	With BAT = 3.0V		4.0		4.25	V	1
	With BAT = 3.3V		4.4		4.65		

AC CHARACTERISTICS—EXPANDED BUS MODE TIMING SPECIFICATIONS

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

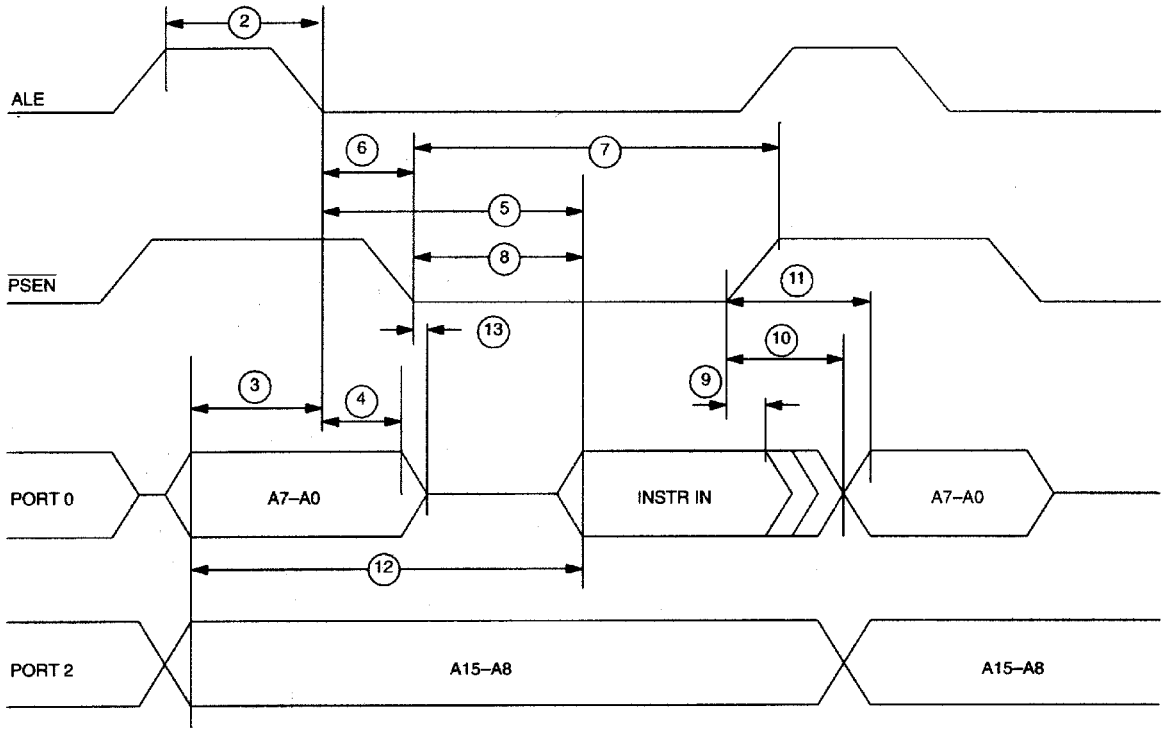
#	PARAMETER		SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency		$1/t_{CLK}$	1.0	16 (-16)	MHz
2	ALE Pulse Width		t_{ALPW}	$2t_{CLK}$ - 40		ns
3	Address Valid to ALE Low		t_{AVALL}	t_{CLK} - 40		ns
4	Address Hold After ALE Low		t_{AVAAV}	t_{CLK} - 35		ns
5	ALE Low to Valid Instruction In	At 12MHz	t_{ALLVI}		$4t_{CLK}$ - 150	ns
		At 16MHz			$4t_{CLK}$ - 90	
6	ALE Low to $\overline{PSEN}$ Low		t_{ALLPSL}	t_{CLK} - 25		ns
7	$\overline{PSEN}$ Pulse Width		t_{PSPW}	$3t_{CLK}$ - 35		ns
8	$\overline{PSEN}$ Low to Valid Instruction In	At 12MHz	t_{PSLVI}		$3t_{CLK}$ - 150	ns
		At 16MHz			$3t_{CLK}$ - 90	
9	Input Instr. Hold after $\overline{PSEN}$ Going High		t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{PSEN}$ Going High		t_{PSIX}		t_{CLK} - 20	ns
11	Address Hold after $\overline{PSEN}$ Going High		t_{PSAV}	t_{CLK} - 8		ns
12	Address Valid to Valid Instruction In	At 12MHz	t_{AVVI}		$5t_{CLK}$ - 150	ns
		At 16MHz			$5t_{CLK}$ - 90	
13	$\overline{PSEN}$ Low to Address Float		t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width		t_{RDPW}	$6t_{CLK}$ - 100		ns
15	$\overline{WR}$ Pulse Width		t_{WRPW}	$6t_{CLK}$ - 100		ns
16	$\overline{RD}$ Low to Valid Data In	At 12MHz	t_{RDLDV}		$5t_{CLK}$ - 165	ns
		At 16MHz			$5t_{CLK}$ - 105	
17	Data Hold after $\overline{RD}$ High		t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High		t_{RDHDZ}		$2t_{CLK}$ - 70	ns
19	ALE Low to Valid Data In	At 12MHz	t_{ALLVD}		8_{CLK} - 150	ns

AC CHARACTERISTICS—EXPANDED BUS MODE TIMING SPECIFICATIONS (continued)

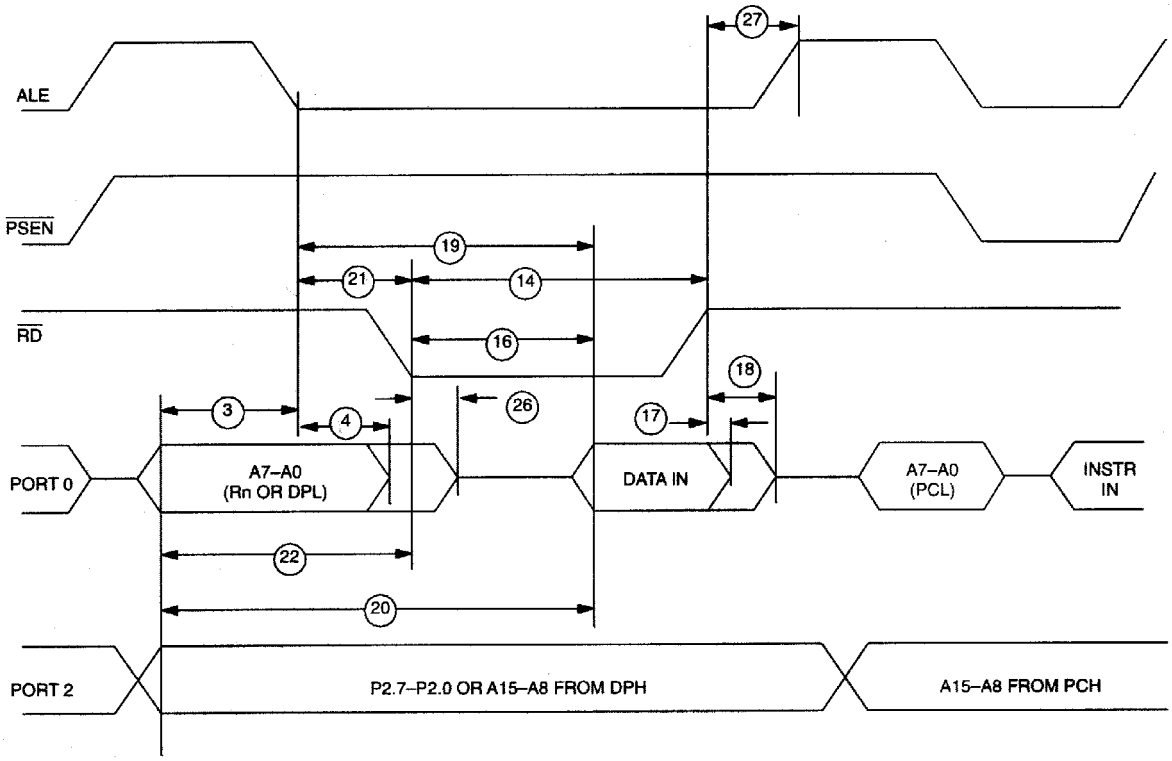
(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS	
19	ALE Low to Valid Data In	At 12MHz	t_{ALLVD}		$8t_{CLK}$ - 150	ns
		At 16MHz			$8t_{CLK}$ - 90	
20	Valid Address to Valid Data In	At 12MHz	t_{AVDV}		$9t_{CLK}$ - 165	ns
		At 16MHz			$9t_{CLK}$ - 105	
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low		t_{ALLRDL}	$3t_{CLK}$ -50	$3t_{CLK}$ + 50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low		t_{AVRDL}	$4t_{CLK}$ -130		ns
23	Data Valid to $\overline{WR}$ Going Low		t_{DVWRL}	t_{CLK} - 60		ns
24	Data Valid to $\overline{WR}$ High	At 12MHz	t_{DVWRH}	$7t_{CLK}$ - 150		ns
		At 16MHz		$7t_{CLK}$ - 90		
25	Data Valid after $\overline{WR}$ High		t_{WRHDV}	t_{CLK} - 50		ns
26	$\overline{RD}$ Low to Address Float		t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High		t_{RDHALH}	t_{CLK} - 40	t_{CLK} + 50	ns

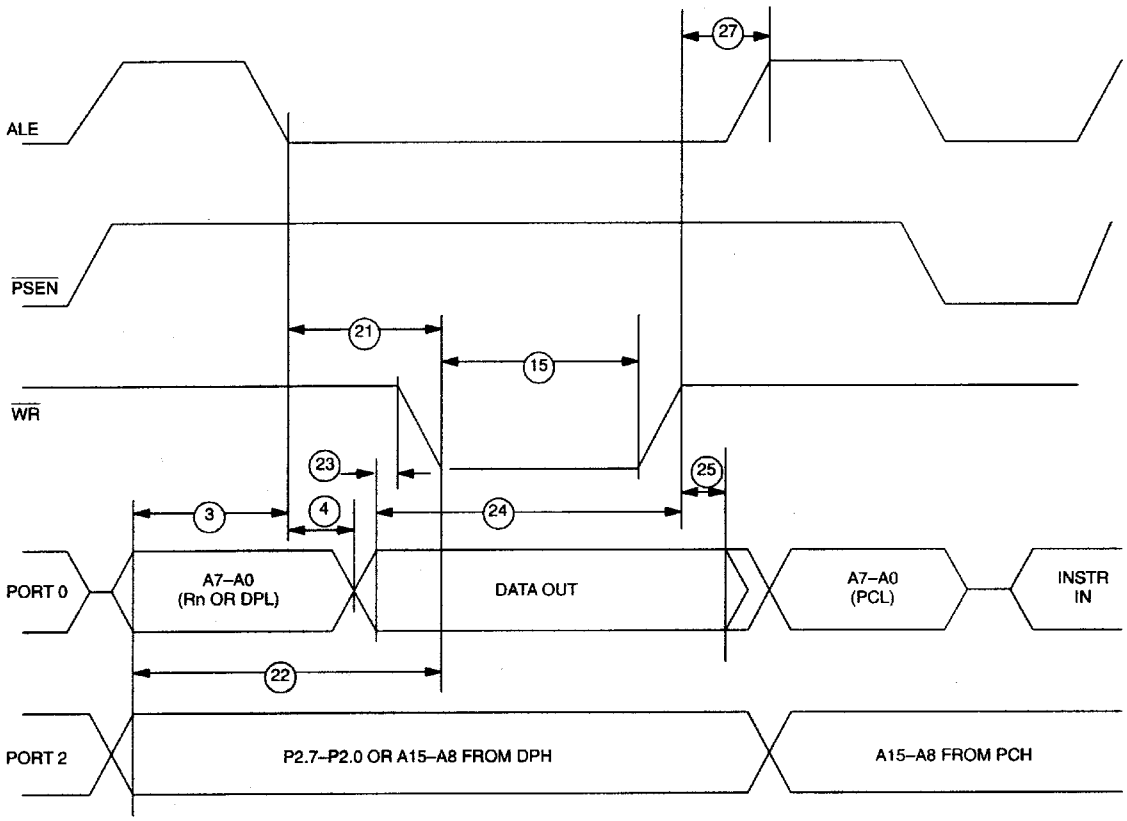
EXPANDED PROGRAM MEMORY READ CYCLE



EXPANDED DATA MEMORY READ CYCLE



EXPANDED DATA MEMORY WRITE CYCLE

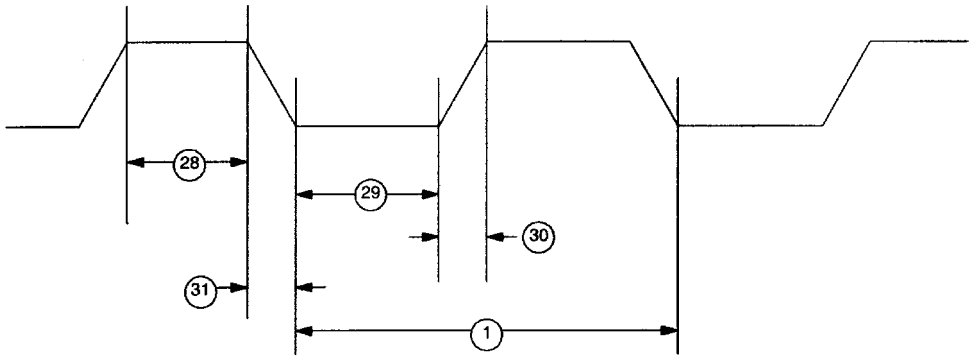


AC CHARACTERISTICS—EXTERNAL CLOCK DRIVE

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	At 12MHz	t_{CLKHPW}	20		ns
		At 16MHz		15		
29	External Clock Low Time	At 12MHz	t_{CLKLPW}	20		ns
		At 16MHz		15		
30	External Clock Rise Time	At 12MHz	t_{CLKR}		20	ns
		At 16MHz			15	
31	External Clock Fall Time	At 12MHz	t_{CLKF}		20	ns
		At 16MHz			15	

EXTERNAL CLOCK TIMING

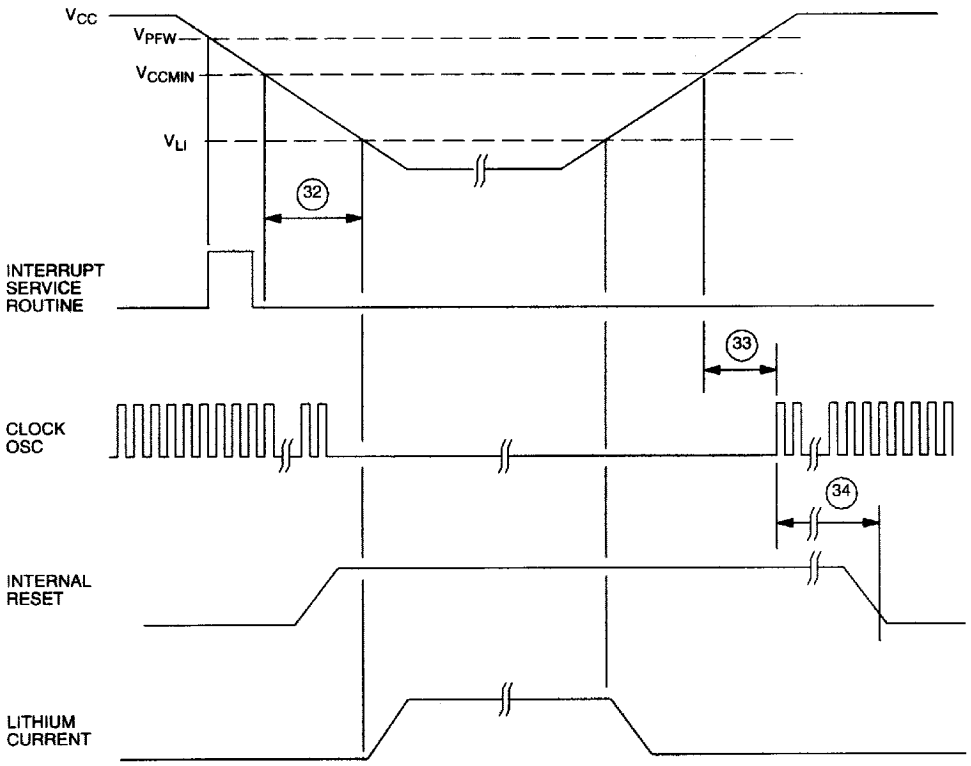


AC CHARACTERISTICS—POWER CYCLE TIMING

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCMIN} to 3.3V	t_F	130		µs
33	Crystal Startup Time	t_{CSU}		(Note 6)	
34	Power-On Reset Delay	t_{POR}		21,504	t_{CLK}

POWER CYCLE TIMING

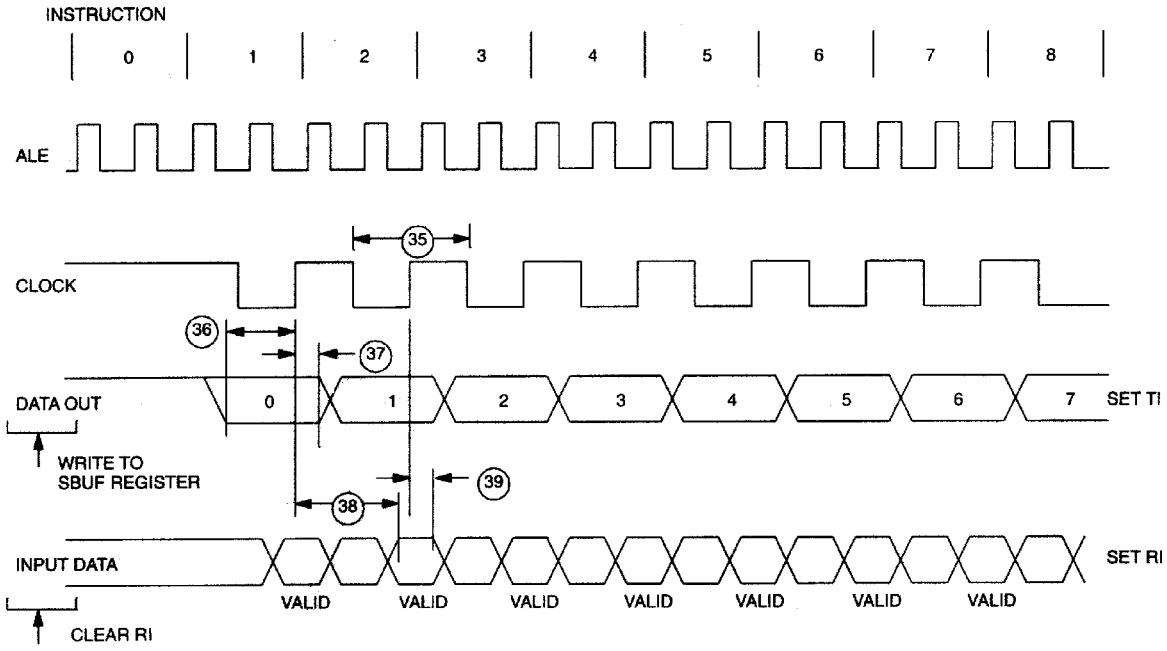


AC CHARACTERISTICS—SERIAL PORT TIMING: MODE 0

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$ - 133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$ - 117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$ - 133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING: MODE 0

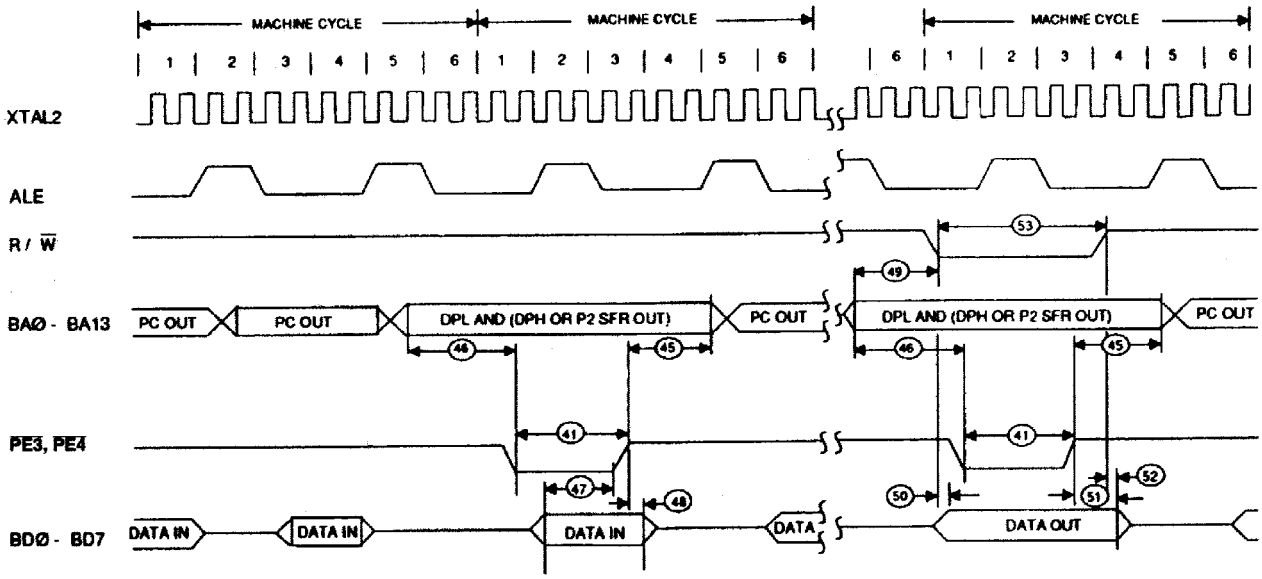


AC CHARACTERISTICS—PARALLEL PROGRAM LOAD TIMING

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
41	Pulse Width of $\overline{PE}$ 3-4	t_{CEPW}	$4t_{CLK}$ - 35		ns
45	Byte-wide Address Hold after $\overline{PE}$ 3-4 High During MOVX	t_{CEHDA}	$4t_{CLK}$ - 30		ns
46	Delay from Byte-wide Address Valid $\overline{PE}$ 3-4 Low During MOVX	t_{CELDA}	$4t_{CLK}$ - 35		ns
47	Byte-wide Data Setup to $\overline{PE}$ 3-4 High During MOVX (read)	t_{DACEH}	$1t_{CLK}$ + 40		ns
48	Byte-wide Data Hold after $\overline{PE}$ 3-4 High During MOVX (read)	t_{CEHDV}	10		ns
49	Byte-wide Address Valid to R/$\overline{W}$ Active During MOVX (write)	t_{AVRWL}	$3t_{CLK}$ - 35		ns
50	Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write)	t_{RWLDV}	20		ns
51	Valid Data Out Hold Time from $\overline{PE}$ 3-4 High	t_{CEHDV}	$1t_{CLK}$ - 15		ns
52	Valid Data Out Hold Time from R/$\overline{W}$ High	t_{RWHDV}	0		ns
53	Write Pulse Width (R/$\overline{W}$ Low Time)	t_{RWLPW}	$6t_{CLK}$ - 20		ns

BYTE-WIDE BUS TIMING



RPC AC CHARACTERISTICS—DBB READ

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
54	$\overline{CS}$, A_0 Setup to $\overline{RD}$	t_{AR}	0		ns
55	$\overline{CS}$, A_0 Hold After $\overline{RD}$	t_{RA}	0		ns
56	$\overline{RD}$ Pulse Width	t_{RR}	160		ns
57	$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		130	ns
58	$\overline{RD}$ to Data Out Delay	t_{RD}	0	130	ns
59	$\overline{RD}$ to Data Float Delay	t_{RDZ}		85	ns

RPC AC CHARACTERISTICS—DBB WRITE

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
60	$\overline{CS}$, A_0 Setup to $\overline{WR}$	t_{AW}	0		ns
61A	$\overline{CS}$, Hold After $\overline{WR}$	t_{WA}	0		ns
61B	A_0, Hold After $\overline{WR}$	t_{WA}	20		ns
62	$\overline{WR}$ Pulse Width	t_{WW}	20		ns
63	Data Setup to $\overline{WR}$	t_{DW}	130		ns
64	Data Hold After $\overline{WR}$	t_{WD}	20		ns

AC CHARACTERISTICS—DMA

(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

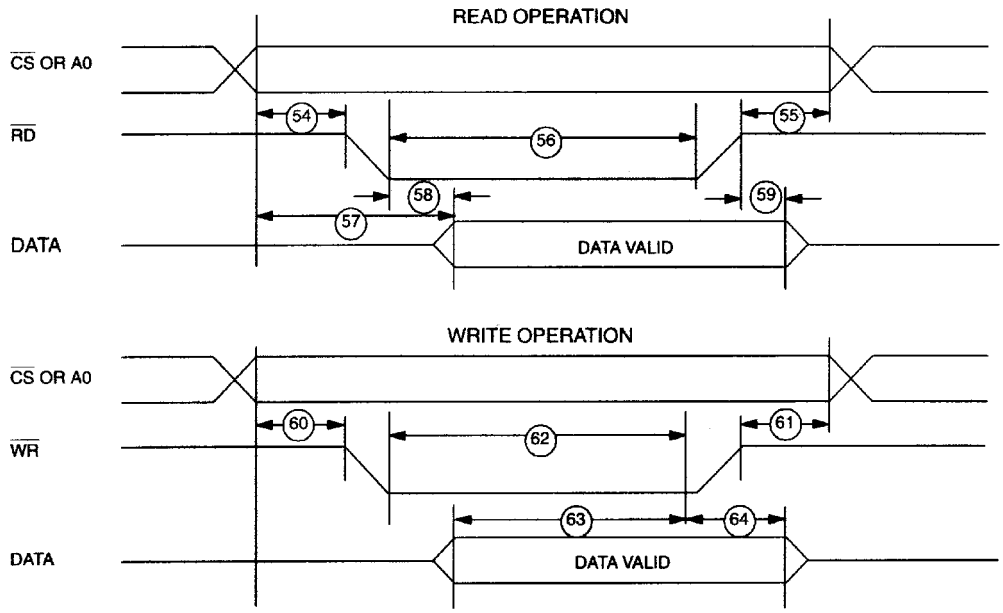
#	PARAMETER	SYMBOL	MIN	MAX	UNITS
65	$\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$	t_{ACC}	0		ns
66	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	t_{CAC}	0		ns
67	$\overline{DACK}$ to Data Valid	t_{ACD}	0	130	ns
68	$\overline{RD}$ or $\overline{WR}$ to DRQ Cleared	t_{CRQ}		110	ns

AC CHARACTERISTICS—$\overline{PROG}$

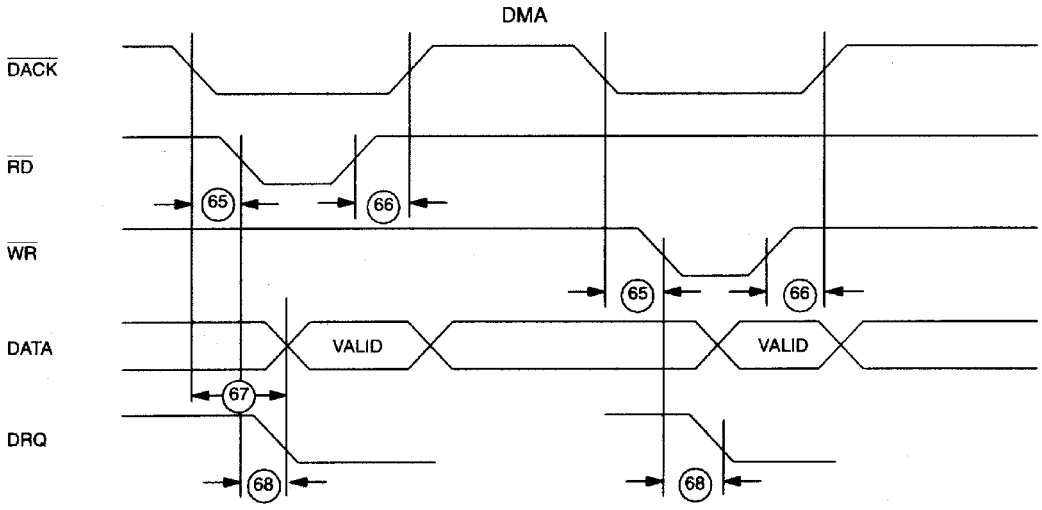
(V_{CC} = 5V ±10%, T_A = 0˚C to +70˚C.)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
69	$\overline{PROG}$ Low to Active	t_{PRA}	48		CLKS
70	$\overline{PROG}$ High to Inactive	t_{PRI}	48		CLKS

RPC TIMING MODE 16



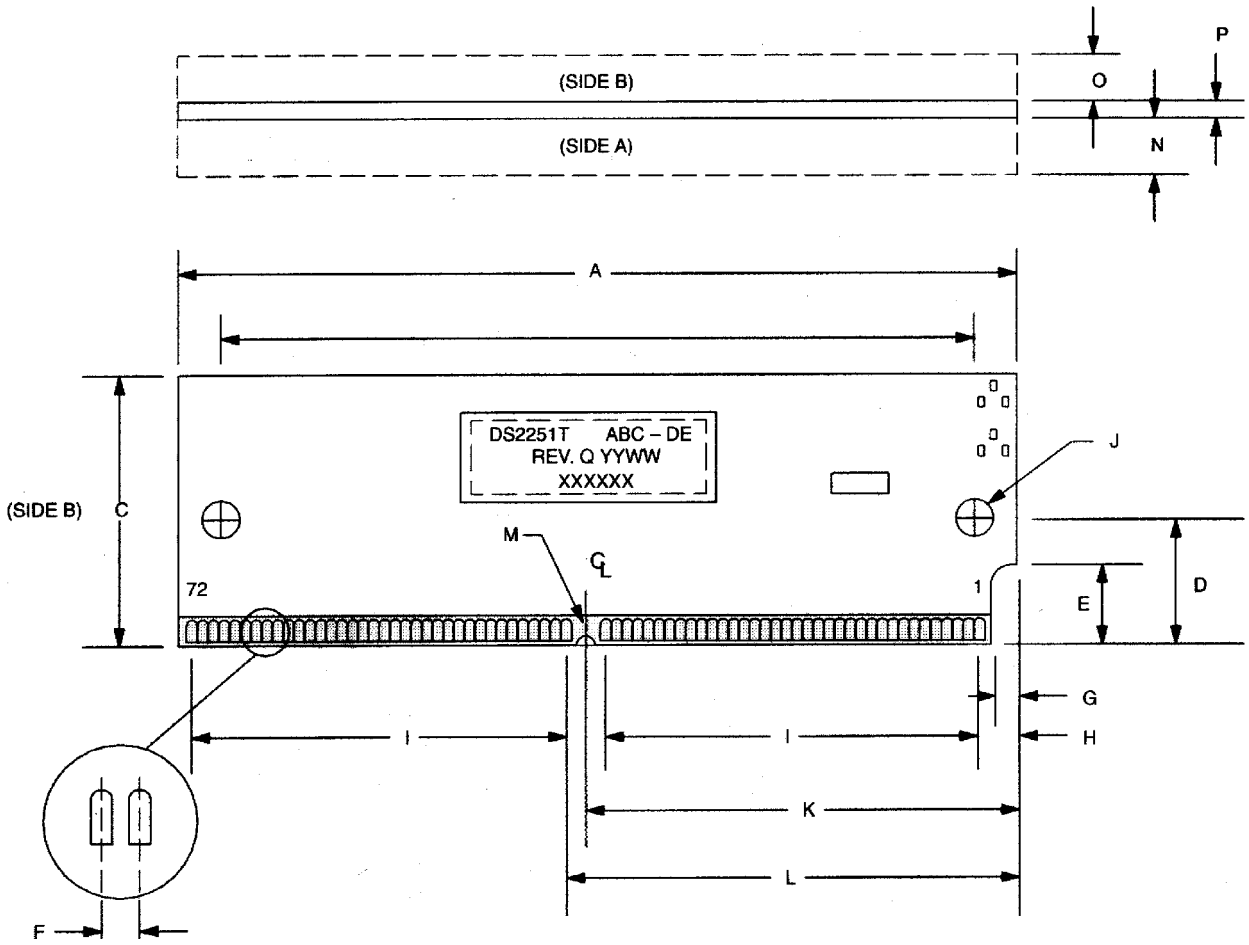
RPC TIMING MODE 16 (continued)



NOTES:

1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10ns, V_{IL} = 0.5V; XTAL2 disconnected; RST = PORT0 = V_{CC}.
3. Idle mode I_{IDLE} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10ns, V_{IL} = 0.5V; XTAL2 disconnected; PORT0 = V_{CC}, RST = V_{SS}.
4. Stop mode I_{STOP} is measured with all output pins disconnected; PORT0 = V_{CC}; XTAL2 not connected; RST = XTAL1 = V_{SS}.
5. Pin capacitance is measured with a test frequency—1MHz, T_A = +25°C.
6. Crystal startup time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on-chip oscillator. The user should check with the crystal vendor for a worst-case specification on this time.
7. $\overline{PF}$ pin operation is specified with $V_{BAT} \geq 3.0V$.

PACKAGE DRAWING



PKG	INCHES	
DIM	MIN	MAX
A	4.245	4.255
B	3.979	3.989
C	0.995	1.005
D	0.395	0.405
E	0.245	0.255
F	0.050 BSC	
G	0.075	0.085
H	0.245	0.255
I	1.750 BSC	
J	0.120	0.130
K	2.120	2.130
L	2.245	2.255
M	0.057	0.067
N	-	0.275
O	-	0.145
P	0.047	0.054

DATA SHEET REVISION SUMMARY

The following represent the key differences between 12/13/95 and 08/13/96 version of the DS2251T data sheet. Please review this summary carefully.

1. Change V_{CC} slew rate definition to reference 3.3V instead of V_{LI}.
2. Add minimum value to PCB thickness.

The following represent the key differences between 08/15/96 and 05/29/97 version of the DS2251T data sheet. Please review this summary carefully.

1. $\overline{PF}$ signal moved from V_{OL2} test specification to V_{OL1}. (PCND73001)

The following represent the key differences between 05/28/97 and 11/08/99 version of the DS2251T data sheet. Please review this summary carefully. (PCN I80903)

1. Correct Absolute Maximum Ratings to reflect changes to DS5001FP microprocessor.
2. Add note clarifying that SRAM contents are not defined under storage temperature conditions.

The following represent the key differences between 11/08/99 and 01/18/00 version of the DS2251T data sheet. Please review this summary carefully.

1. Document converted from interleaf to Microsoft Word.

The following represent the key differences between 01/18/00 and 06/13/06 version of the DS2251T data sheet. Please review this summary carefully.

1. Updated reference in Features (High-Reliability Operation) to 10-year NV RAM data life to include room temperature caveat.
2. Added RoHS-compliant packages to Ordering Information table.
3. Replaced references to “Secure Microcontroller Data Book” with “Secure Microcontroller User’s Guide.”

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