

VSC8115

155 Mbps, 622 Mbps (OC-3/12/STM-1/4) Clock and Data Recovery

The VSC8115 functions as a Clock and Data Recovery (CDR) unit for SONET/SDH-based equipment to derive high-speed timing signals. The VSC8115 recovers the clock from the scrambled NRZ data operating at 622.08 Mbps (STS-12/OC-12/STM-4) or 155.52 Mbps (STS-3/OC-3/STM-1). After the clock is recovered, the data is retimed using an output flip-flop. In the absence of a valid signal, the PLL will lock to the reference clock, providing the downstream device a constant clock signal, and reducing the relocking time.

Both recovered clock and retimed data outputs can be configured as LVDS or LVPECL signals to facilitate a low-jitter and low-power interface.

Applications

- SONET/SDH systems
- DWDM systems
- ATM switch and routers
- Optical test equipment

Specifications

- Data rates: OC-3/12
- Low power: 180 mW typical power
- +3.3 V power supply
- 20-pin TSSOP package

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Features

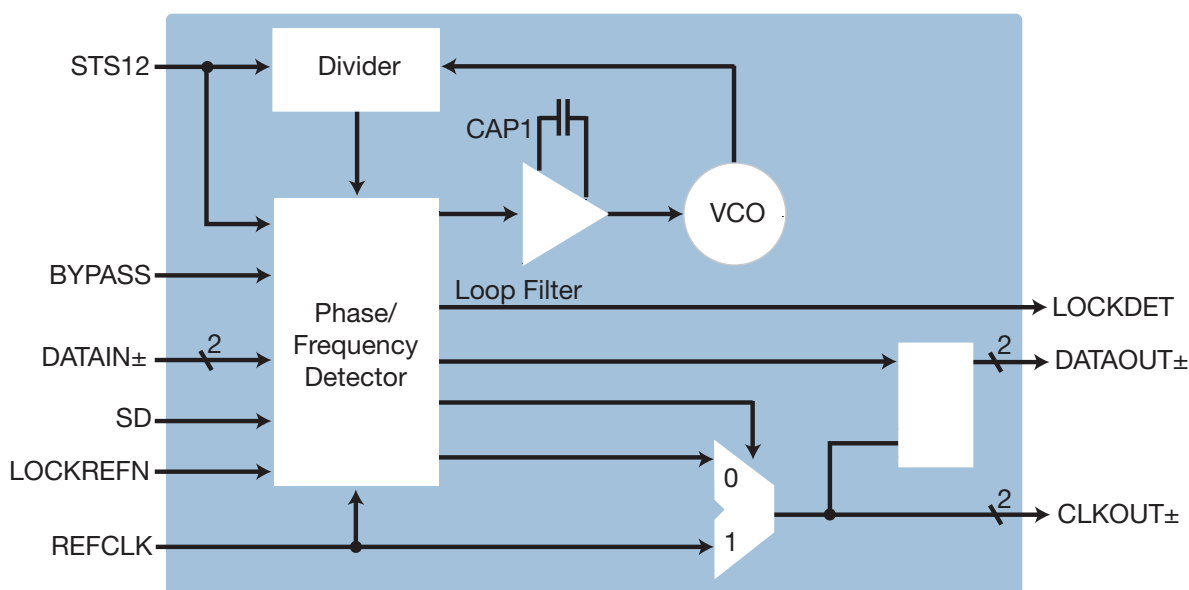
- Performs clock and data recovery for OC-12 (STM-4) and OC-3 (STM-1) NRZ data
- Low power: 188 mW typical power dissipation
- High-speed outputs can be configured for LVPECL or LVDS levels
- Signal and lock detect status outputs
- PLL bypass operation facilitates board debug process
- Automatic lock to reference

Benefits

- Allows customers to use a single CDR for 155 Mbps and 622 Mbps applications
- Enables flexible implementation, simplifies layout
- Enables the system management process to monitor the incoming signal
- Facilitates in board debugging process
- Provides downstream ASIC constant clock signal when a valid signal is not present

Related Products

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