CDB4340A/41A

Evaluation Board for CS4340A and CS4341A

Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

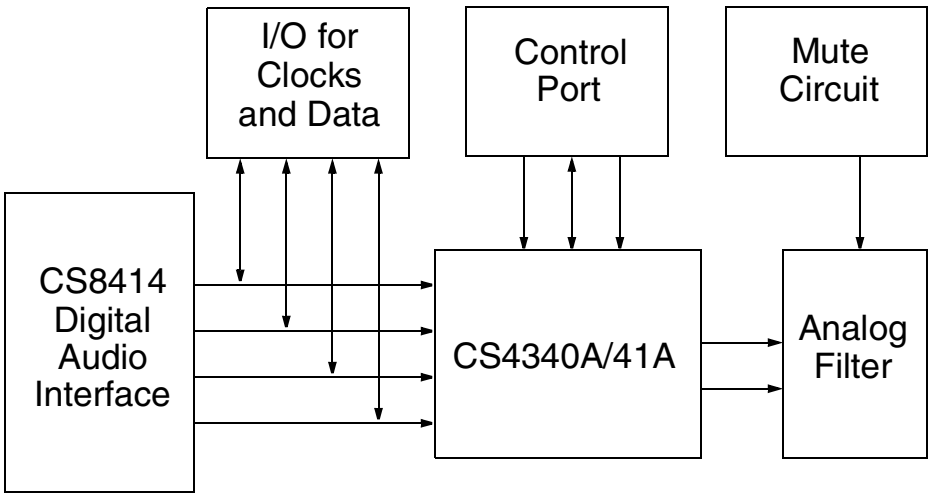
Description

The CDB4340A/41A evaluation board is an excellent means for quickly evaluating the CS4340A/41A family of 24-bit, stereo D/A converters. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4341A and a power supply. Analog outputs are provided via RCA phono jacks for both channels.

The CS8414 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converters and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4340A, CDB4341A	Evaluation Board



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1. CDB4340A/41A SYSTEM OVERVIEW

The CDB4340A/41A evaluation board is an excellent means of quickly evaluating the CS4340A/41A. The CS8414 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB4340A/41A schematic has been partitioned into 10 schematics shown in Figures 2 through 11. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CDB4340A/41A ERRATA

The CS4340A is mounted on the same PCB used to evaluate the CS4340. Please see tables 3 to 5 for jumper settings that are not applicable to the CDB4340A/41A. These jumpers should retain the default setting from the factory. Also, all SDATA net names for the CS4340A shall be interpreted as SDIN, as seen in the pin description of the CS4340A datasheet.

3. CS4340A/41A DIGITAL TO ANALOG CONVERTER

A description of the CS4340A is included in the CS4340A data sheet. A description of the CS4341A is included in the CS4341A data sheet.

4. CS8414 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8414 Digital Audio Receiver, Figure 5. The outputs of the CS8414 include a serial bit clock, serial data, left-right clock (FSYNC), and a 256 Fs master clock. The operation of the CS8414 and a discussion of the digital audio interface are included in the CS8414 Datasheet.

During normal operation, the CS8414 operates in the Channel Status mode where the LED's display channel status information for the channel selected by the CSLR/FCK jumper.

When the Error & Frequency button is enabled, the CS8414 operates in the Error and Frequency information mode. The information displayed by the LED's can be decoded by consulting the CS8414 data sheet.

Encoded sample frequency information can be displayed provided a proper clock is being applied to the FCK pin of the CS8414. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8414. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option of CSLR/FCK should be selected if the FCK pin is being driven by a clock signal.

5. CS8414 DATA FORMAT

The CS8414 data format can be set with jumpers M0, M1, M2, and M3, as described the CS8414 datasheet. The format selected must be compatible with the data format of the CS4340A or CS4341A, shown in the CS4340A and CS4341A datasheets. Please note that the CS8414 does not support all the possible modes of the CS4340A or CS4341A, see Table 1 for details. The default settings for M0-M3 on the evaluation board are given in Tables 3-5.

CS4341A Format	CS4340A Format	CS8414 Format	External SCLK	Internal SCLK
0	-	2	Yes	Yes
1	0	2	Yes	No
2	1	0	No	Yes
3	2	Unsupported	-	-
4	-	Unsupported	-	-
5	3	5	Yes	No
6	-	6	Yes	Yes
7	0	2	Yes	No

Table 1. CS8414 Supported Formats

6. ANALOG OUTPUT FILTER

The evaluation board includes a pair of single pole passive filters. The passive filters, Fig. 3, have a corner frequency of approximately 95 kHz with JP3 and JP6 installed and 190 kHz without JP3 and JP6.

7. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow the interface to external systems via the 10-pin header, J9. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 11. The 74HC243 transceiver functions as an I/O buffer where jumpers HDR1-HDR6 determine if the transceiver operates as a transmitter or receiver. A transmit function is implemented with the HDR1-HDR6 jumpers in the 8414 position. LRCK, SDATA, and SCLK from the CS8414 will be outputs on J9. The transceiver operates as a receiver with jumpers HDR1-HDR6 in the EXTERNAL position. MCLK, LRCK, SDATA and SCLK on J9 become inputs.

8. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by three binding posts (GND, +5V, +3V/+5V) (see Figure 10). The +5V input supplies power to the +5 Volt digital circuitry (VA+5, VD+5, VDPC+5), while the +3V/+5V input supplies power to the Voltage Level Converter and the CS4340A/41A for evaluation in either +3 or +5 Volt mode.

9. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4340A/41A requires careful attention to power supply and grounding arrangements to optimize performance. Figure 10 details the power distribution used on this board. The CDB4340A/41A ground plane is split to control the digital return currents in order to minimize digital interference. The decoupling capacitors are located as close to the CS4340A/41A as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yields large reductions in radiated noise.

10. CDB4341A CONTROL PORT SOFTWARE

The CDB4341A is shipped with Windows based software for interfacing with the CS4341A control port via the DB25 connector, P1. The software can be used to communicate with the CS4341A in either SPI or I^2C mode; however, in SPI mode the CS4341A registers are write-only.

Run SETUP.EXE from the distribution diskette to install the software. Further documentation for the software is available on the distribution diskette. The documentation is available in the plain text format file, README.TXT.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 V	input	+ 5 Volt power
+3V/+5V	input	+ 3 Volt or + 5 Volt power for the CS4340A/41A and the Voltage Level Converter
GND	input	ground connection from power supply
Digital input	input	digital audio interface input via coax
Optical input	input	digital audio interface input via optical
J9	input/output	I/O for master, serial, left/right clocks and serial data
Parallel Port	input/output	parallel connection to PC for SPI/I^2C control port signals
Control I/O	input/output	I/O for SPI/I^2C control port signals
AOUTA	output	channel A analog output with single-pole passive filter
AOUTB	output	channel B analog output with single-pole passive filter

Table 2. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI *LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*Low *High *Low *Low	See CS8414 Datasheet for details
SCLK	**N/A**	INT *EXT	**N/A**
DEM_8414	**N/A**	*8414 DEM	**N/A**
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
HDR 7	Enables the external mute for AOUTA	*ON OFF	Mute Enabled Mute Disabled
HDR 8	Enables the external mute for AOUTB	*ON OFF	Mute Enabled Mute Disabled
MCLK	Selects Single-Speed or Double-Speed Modes	*x1 ÷2	Selects Single-Speed Mode Selects Double-Speed Mode
HDR15	DIF1	HI *LOW	See CS4340A Datasheet for details
HDR16	DIF0	HI *LOW	See CS4340A Datasheet for details
HDR17	DEM0	HI *LOW	See CS4340A Datasheet for details
ENCTRL	Enables/Disables parallel port	Enable *Disable	Invalid for CS4340A Disables parallel port

Table 3. CDB4340A Jumper Selectable Options

*Default setting from factory

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI *LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*Low *High *Low *Low	See CS8414 Datasheet for details
SCLK	**N/A**	INT *EXT	**N/A**
DEM_8414	**N/A**	*8414 DEM	“Don’t Care” for CS4341A
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
HDR 7	Enables the external mute for AOUTA	*ON OFF	Mute Enabled Mute Disabled
HDR 8	Enables the external mute for AOUTB	*ON OFF	Mute Enabled Mute Disabled
MCLK	Selects Single-Speed or Double-Speed Modes	*x1 ÷2	Selects Single-Speed Mode Selects Double-Speed Mode
HDR15	SCL Pull-Up	*HI LOW	SCL pulled high Invalid for I^2C mode
HDR16	SDA Pull-Up	*HI LOW	SDA pulled high Invalid for I^2C mode
HDR17	AD0	HI *LOW	“Don’t Care” for Control Port Mode
ENCTRL	Enables/Disables parallel port	*Enable Disable	Enables parallel port Disables parallel port (must use HDR14)

Table 4. CDB4341A (I^2C Mode) Jumper Selectable Options

*Default setting from factory

Notes: The CDB4341A evaluation board is shipped from the factory configured for I^2C mode.

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI *LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*Low *High *Low *Low	See CS8414 Datasheet for details
SCLK	**N/A**	INT *EXT	**N/A**
DEM_8414	**N/A**	*8414 DEM	“Don’t Care” for CS4341A
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
HDR 7	Enables the external mute for AOUTA	*ON OFF	Mute Enabled Mute Disabled
HDR 8	Enables the external mute for AOUTB	*ON OFF	Mute Enabled Mute Disabled
MCLK	Selects Single-Speed or Double-Speed Modes	*x1 ÷2	Selects Single-Speed Mode Selects Double-Speed Mode
HDR15	CCLK Pull-up or Pull-down	*HI LOW	“Don’t Care” for SPI mode
HDR16	CDIN Pull-up or Pull-down	*HI LOW	“Don’t Care” for SPI mode
HDR17	$\overline{CS}$ Pull-up	HI *LOW	“Don’t Care” for Control Port Mode
ENCTRL	Enables/Disables parallel port	*Enable Disable	Enables parallel port Disables parallel port (must use HDR14)

Table 5. CDB4341A (SPI Mode) Jumper Selectable Options

*Default setting from factory

Notes: When in SPI mode, it is not possible to read the control registers of the CS4341A. The CDB4341A evaluation board is shipped from the factory configured for I^2C mode.

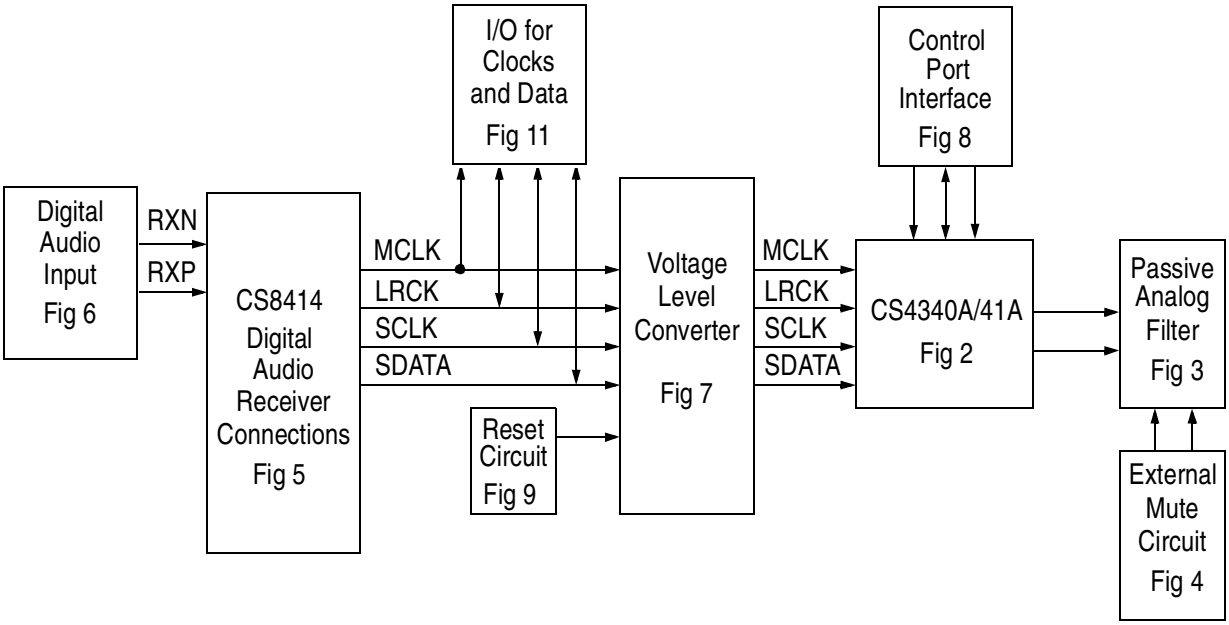

Figure 1. System Block Diagram and Signal Flow

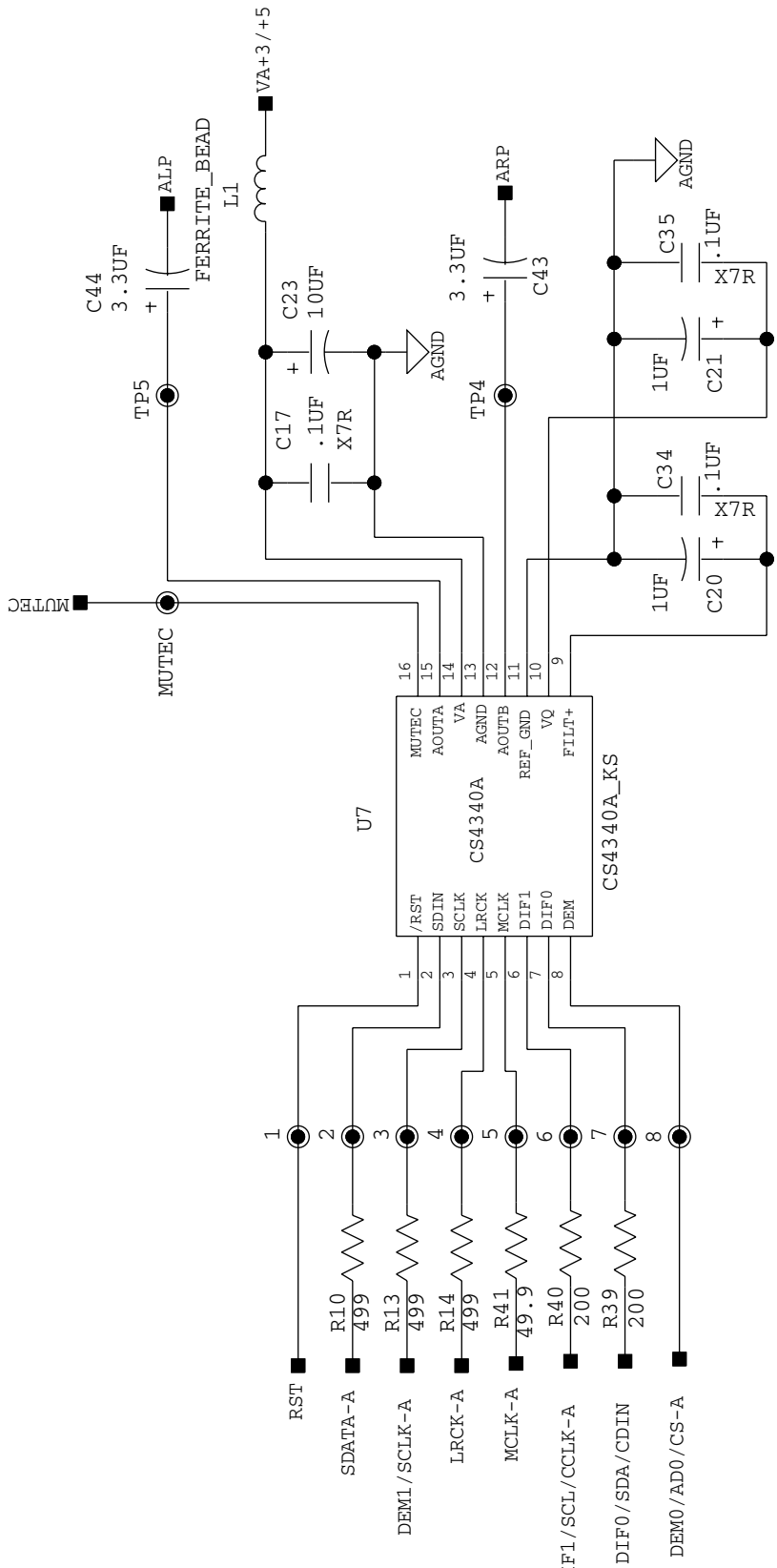

Figure 2. CS4340A/41A

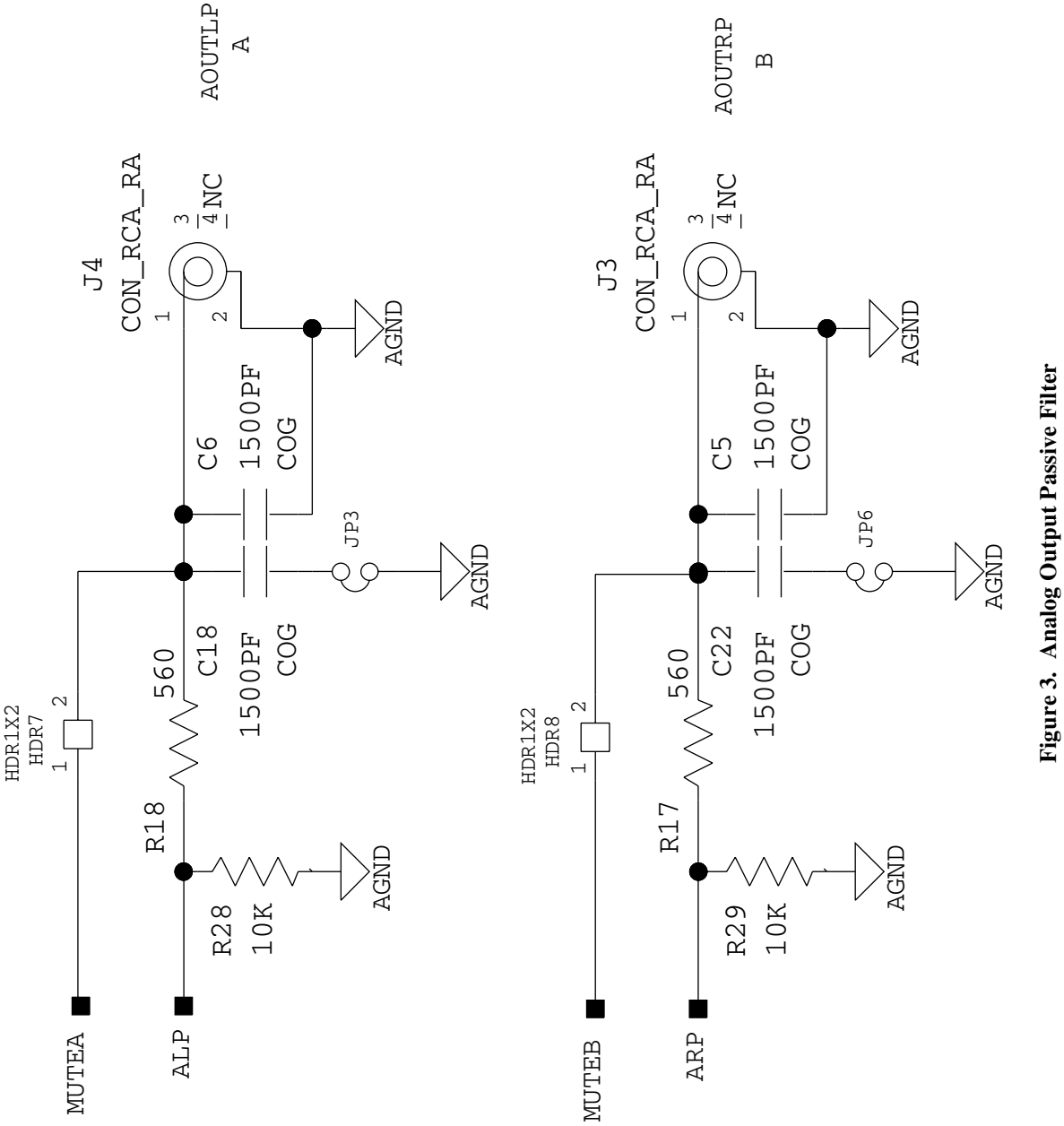

Figure 3. Analog Output Passive Filter

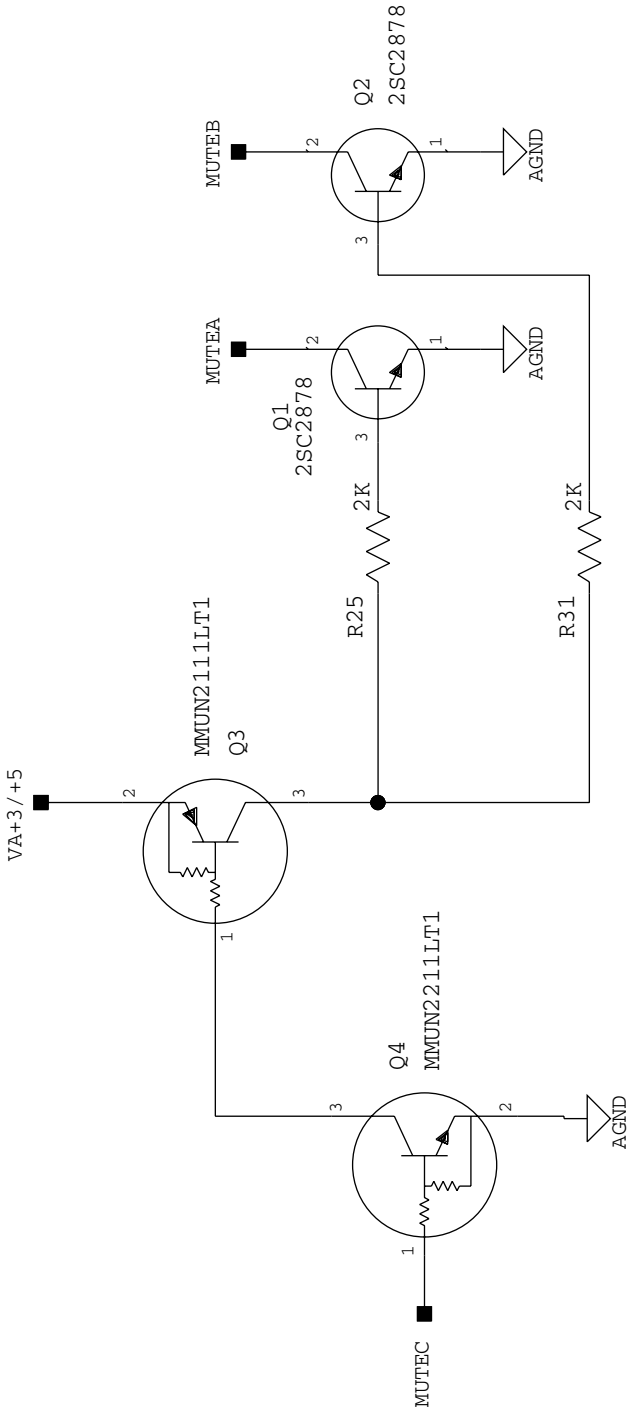

Figure 4. External Mute Circuit

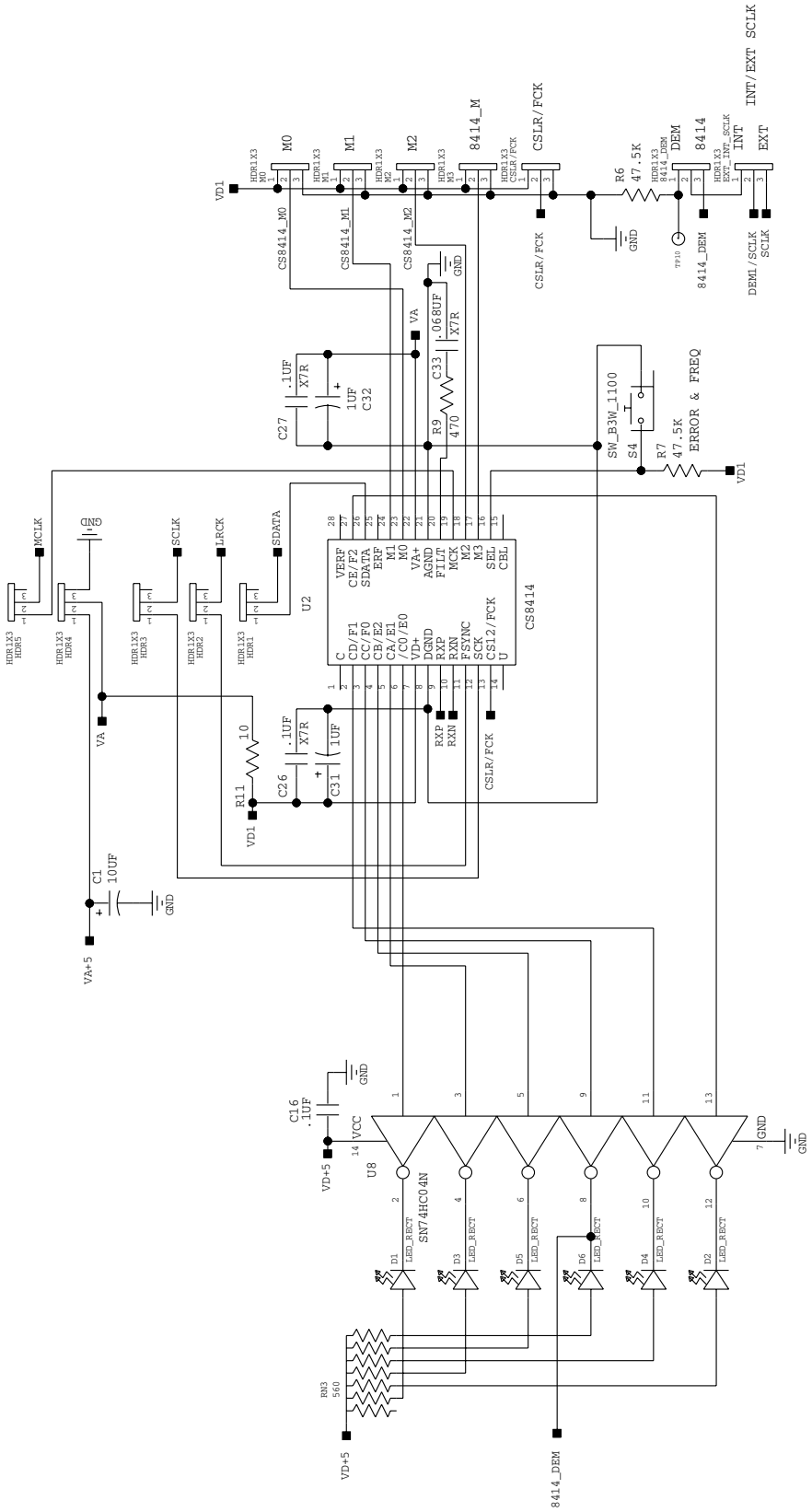

Figure 5. CS8414 Digital Audio Receiver Connections

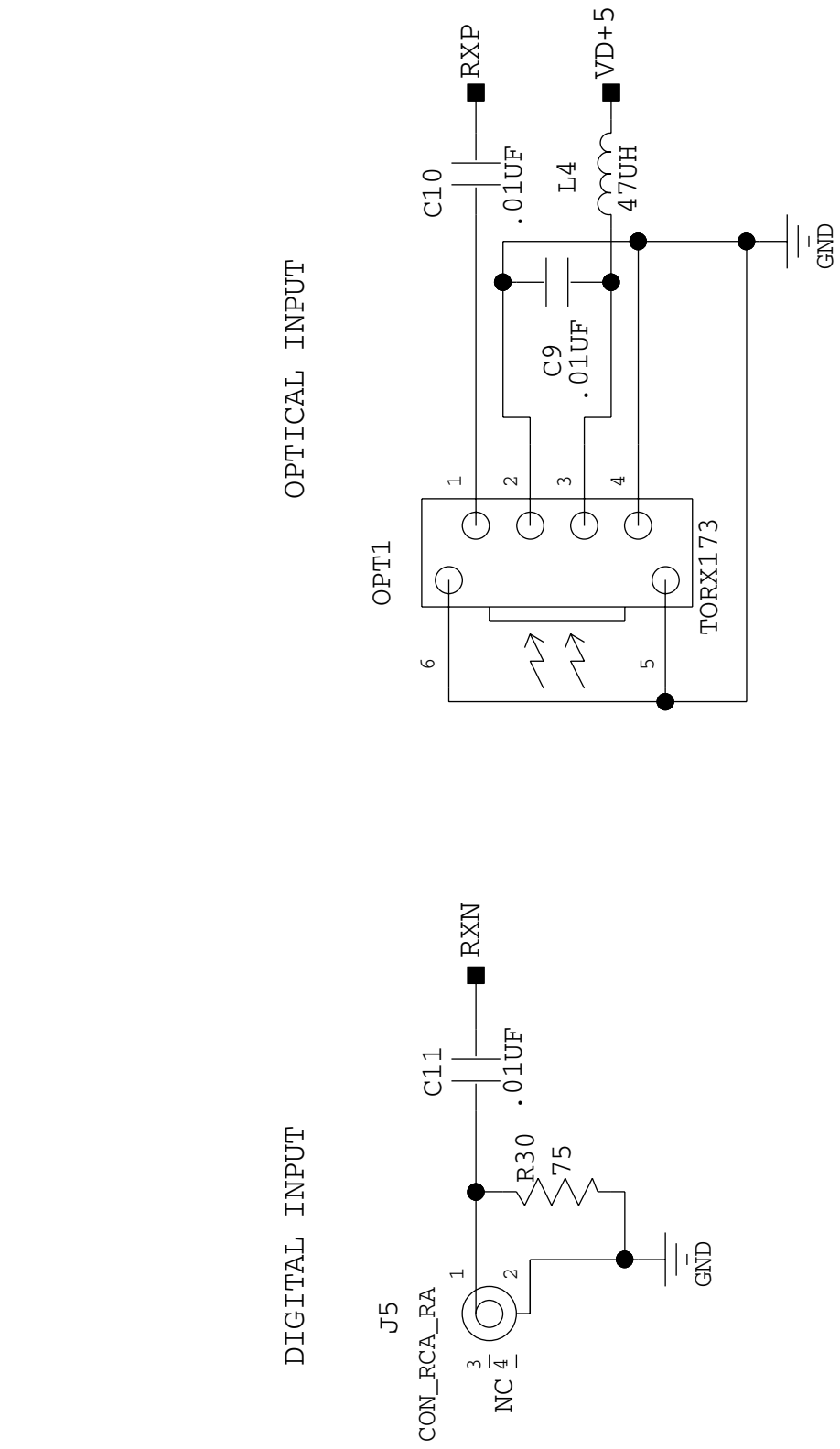

Figure 6. Digital Audio Inputs

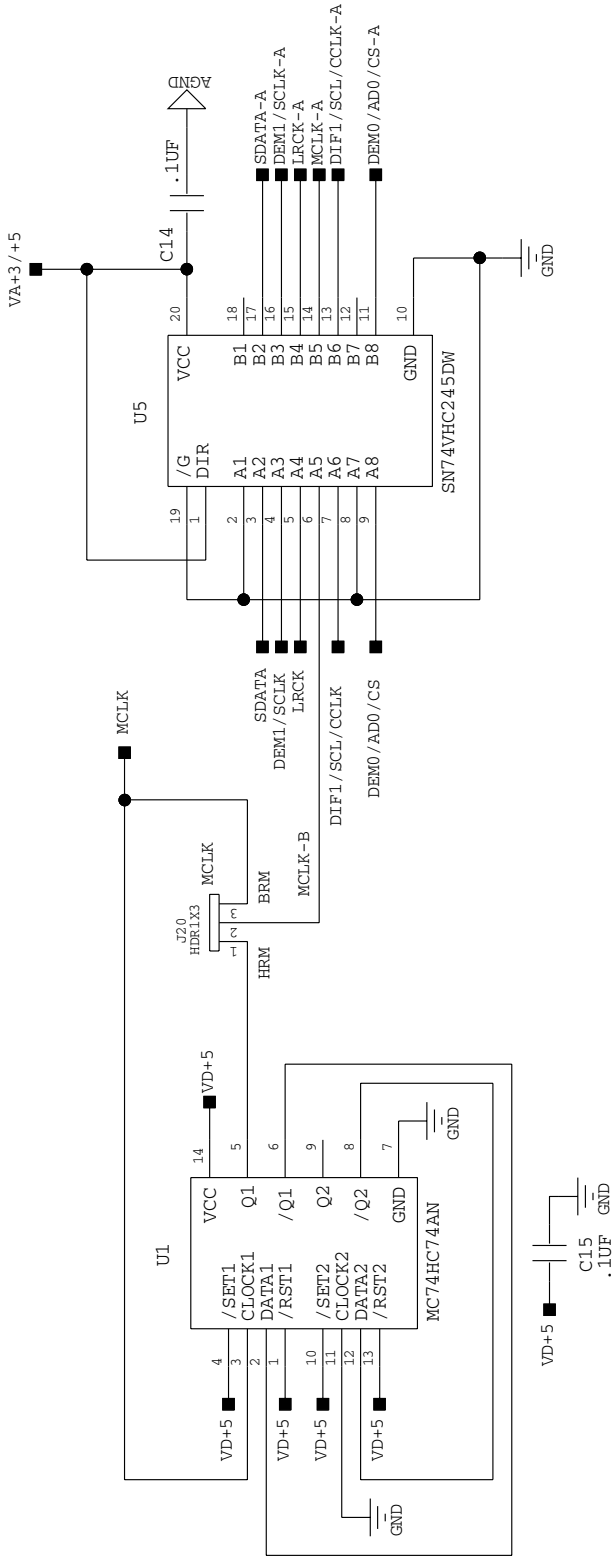

Figure 7. MCLK Divider and Voltage Level Converter

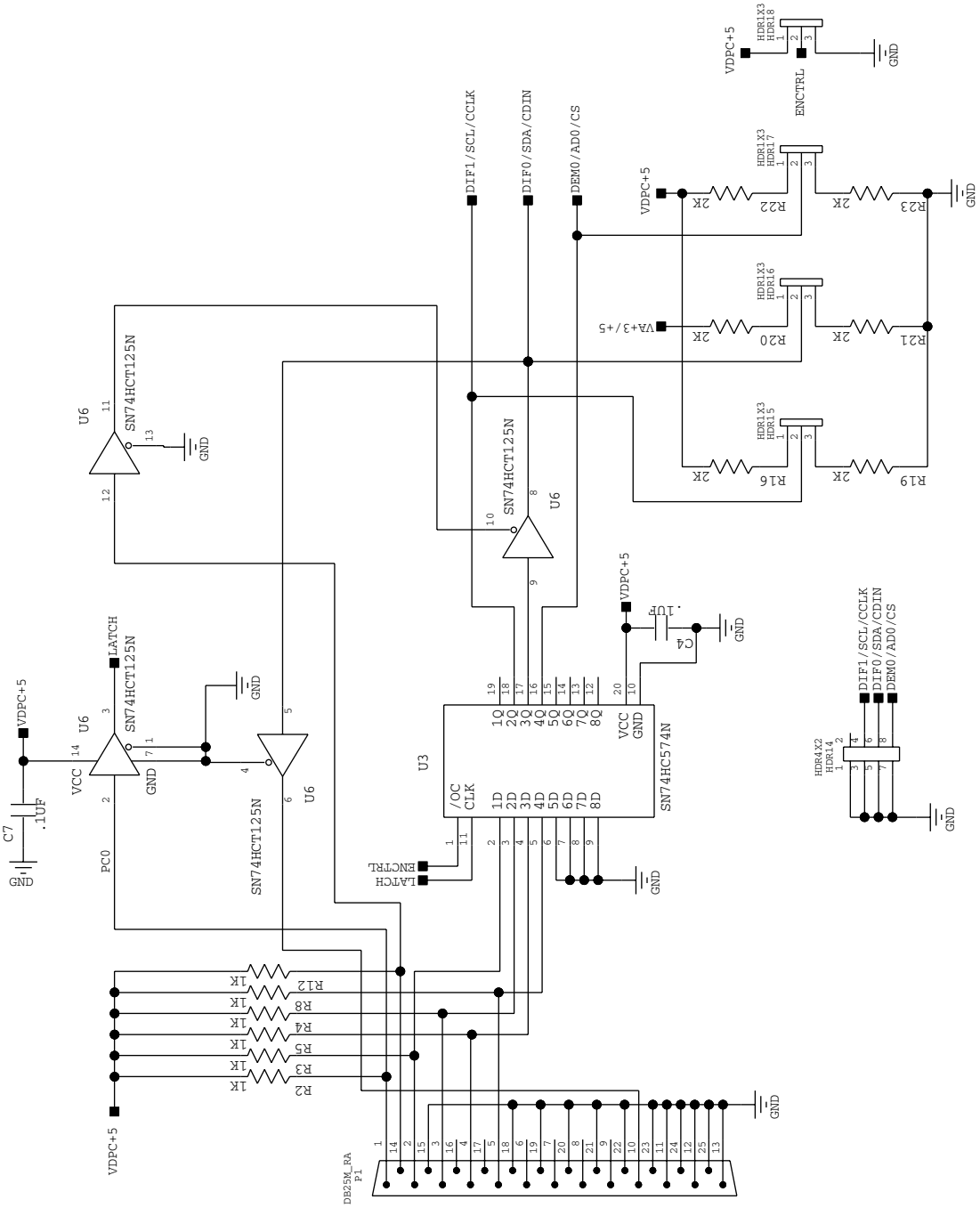

Figure 8. Control Port Interface

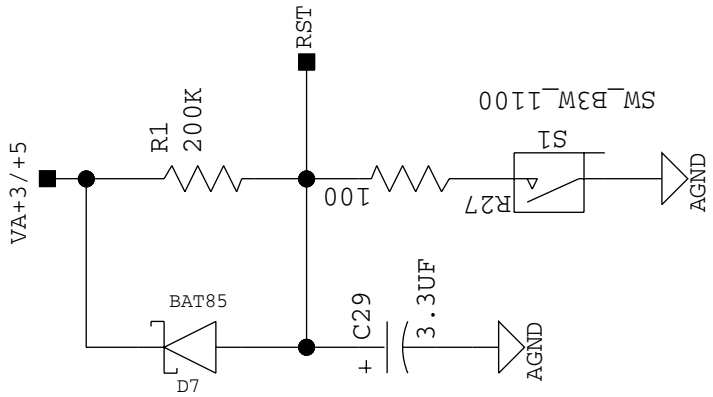

Figure 9. Reset Circuitry

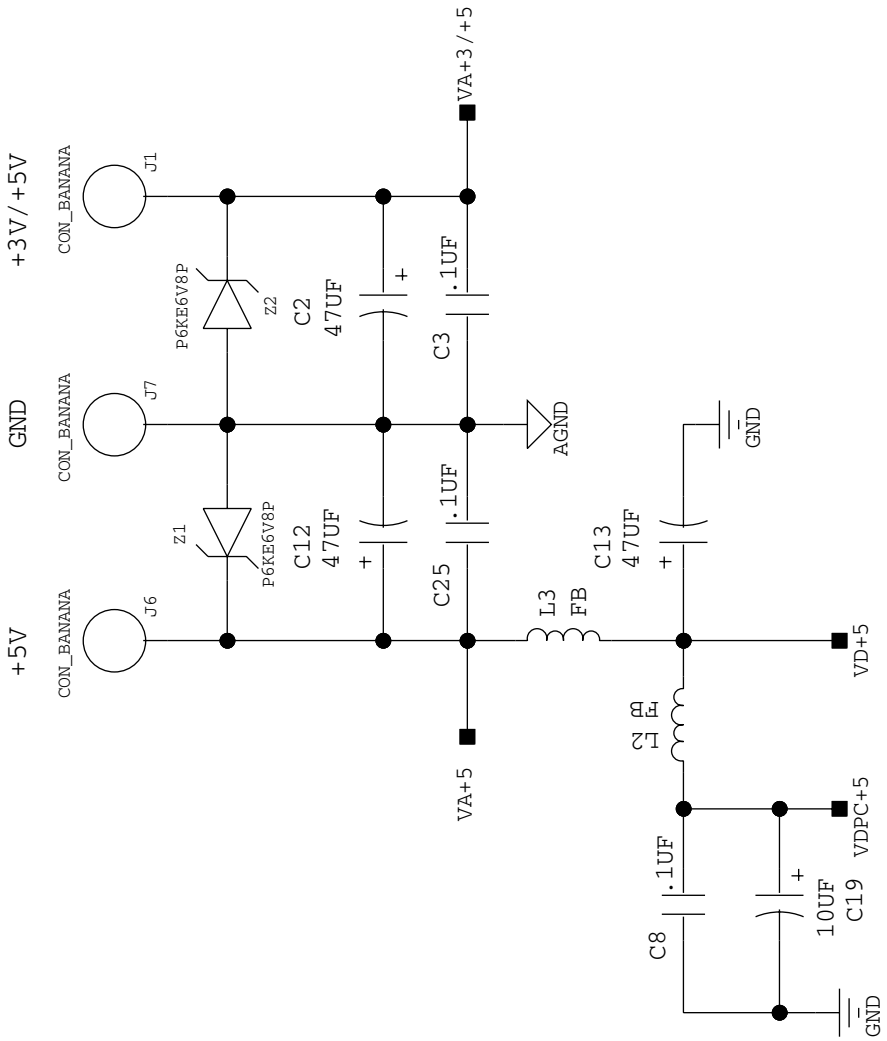

Figure 10. Power Supply

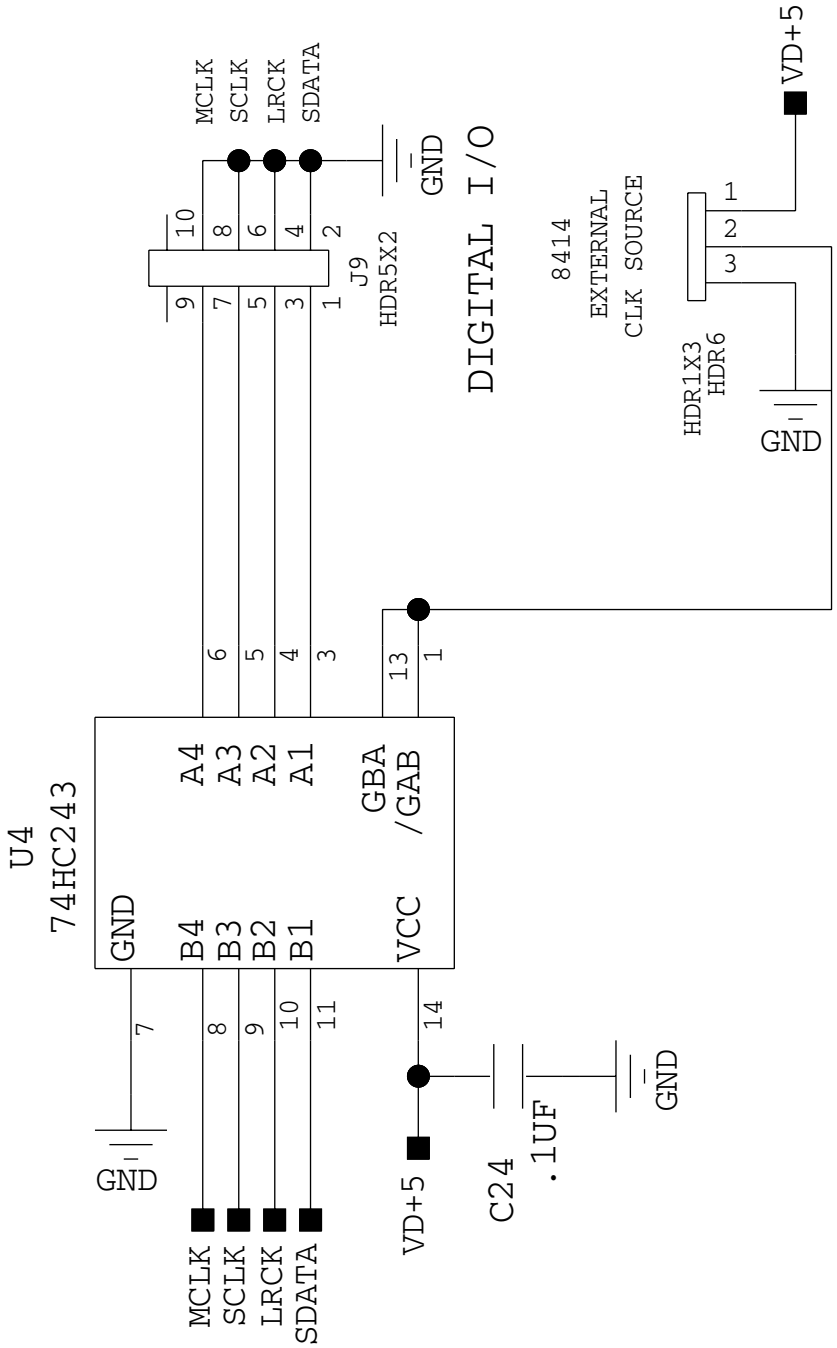

Figure 11. I/O for Clocks and Data

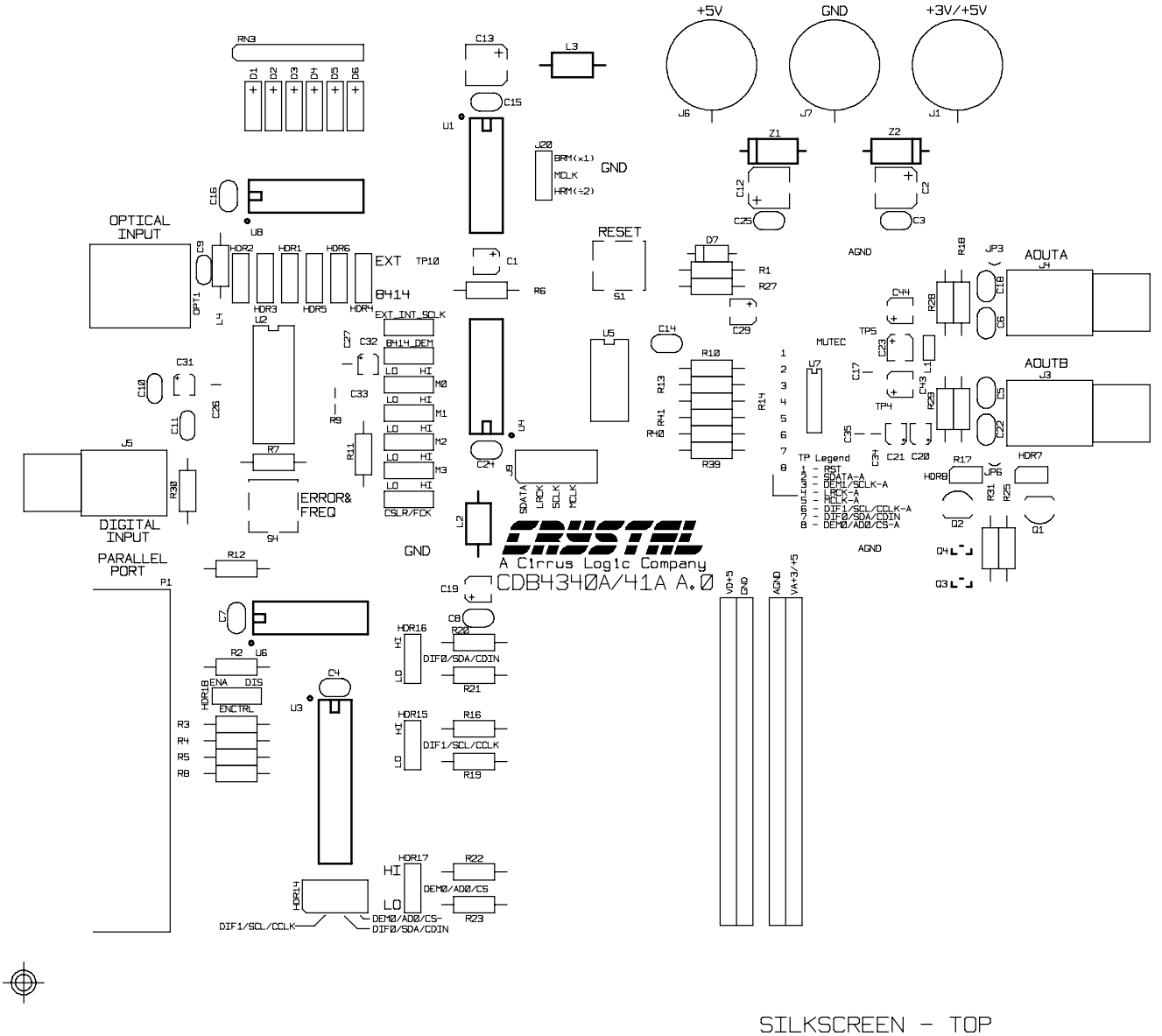

Figure 12. Silkscreen Top

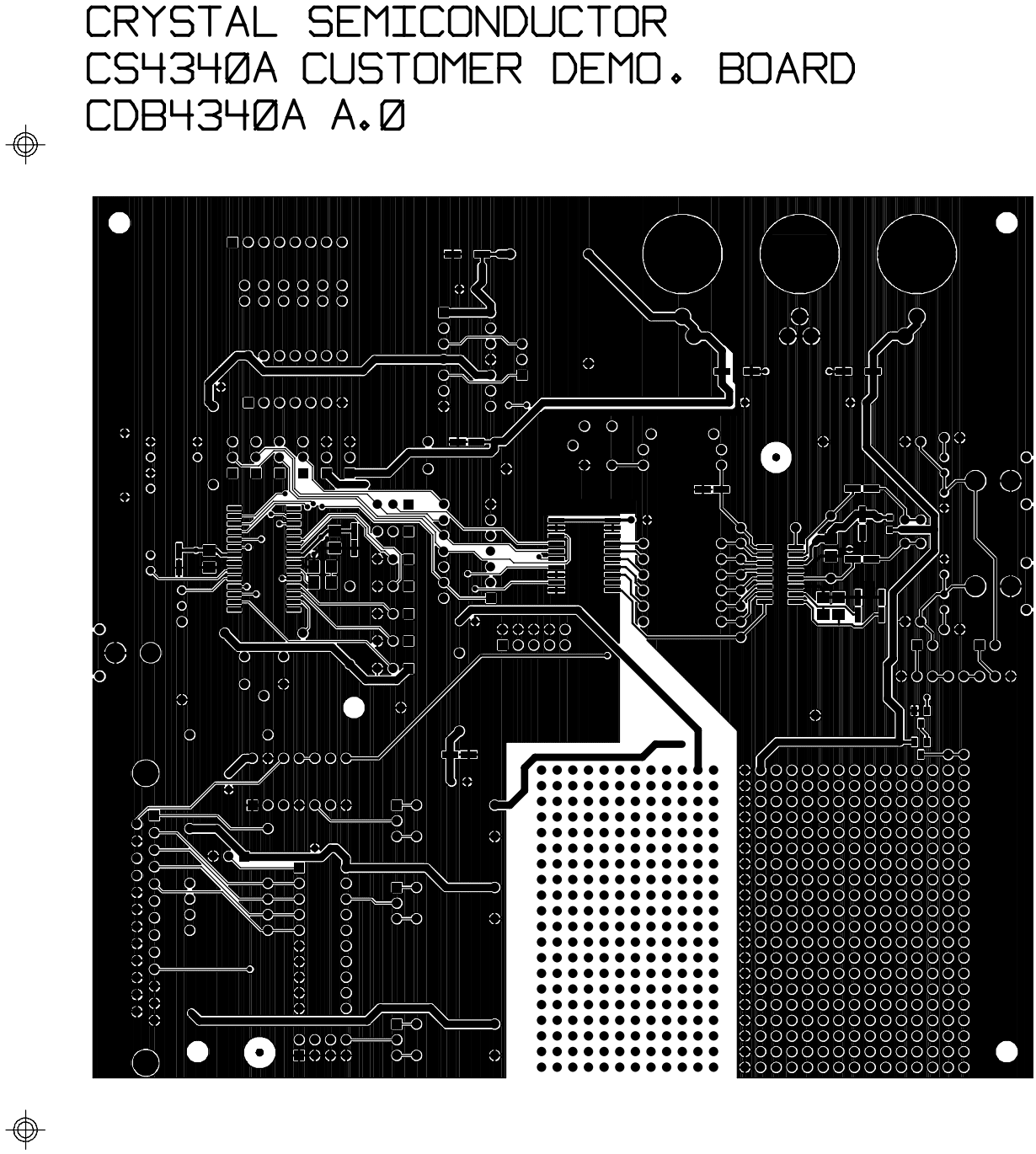

Figure 13. Top Side

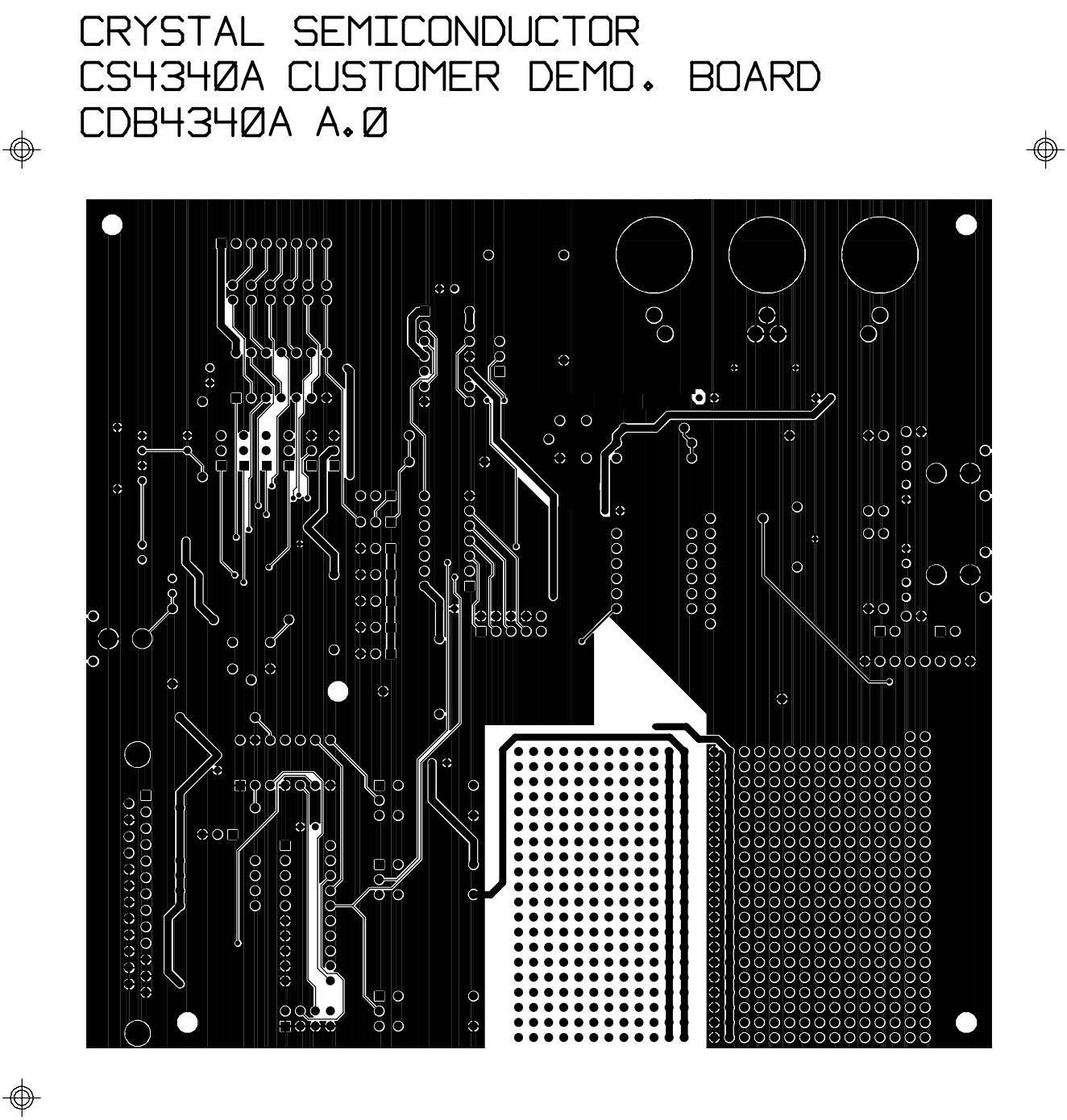

Figure 14. Bottom Side

• Notes •

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