SR3.3
RailClamp®
Low Capacitance TVS Diode Array

Description

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The SR series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by electrostatic discharge **(ESD)**, electrical fast transients **(EFT)**, and tertiary **lightning.**

The unique design of the SR series devices incorporates four surge rated, low capacitance steering diodes and a TVS diode in a single package. The TVS diode is constructed using Semtech's proprietary low voltage EPD technology for superior electrical characteristics at 3.3 volts.

During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

The low capacitance array configuration allows the user to protect two high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges.

Features

- ESD protection to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Array of surge rated diodes with internal EPD TVS™ diode
- Protects two I/O lines
- Low capacitance (<10pF) for high-speed interfaces
- Low leakage current (< 1µA)
- Low operating voltage: 3.3V
- Solid-state technology

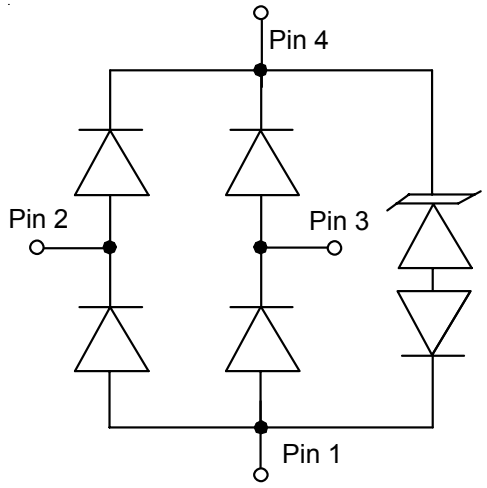
Mechanical Characteristics

- JEDEC SOT-143 package
- Molding compound flammability rating: UL 94V-0
- Marking : R3.3
- Packaging : Tape and Reel

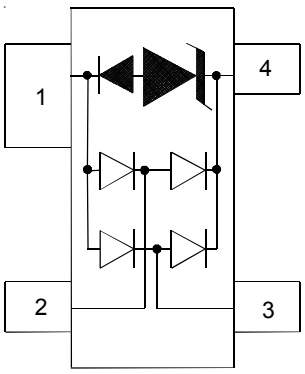
Applications

- Data and I/O lines
- Sensitive Analog Inputs
- Video Line Protection
- Portable Electronics
- Microcontroller Input Protection
- WAN/LAN Equipment

Circuit Diagram



Schematic & PIN Configuration



SOT-143 (Top View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	150	Watts
Peak Pulse Current (tp = 8/20µs)	I_{PP}	10	A
Peak Forward Voltage (I_F = 1A, tp=8/20µs)	V_{FP}	1.5	V
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

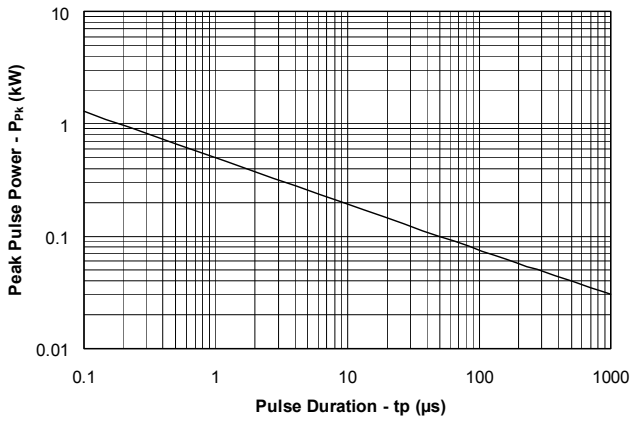
Electrical Characteristics

SR3.3

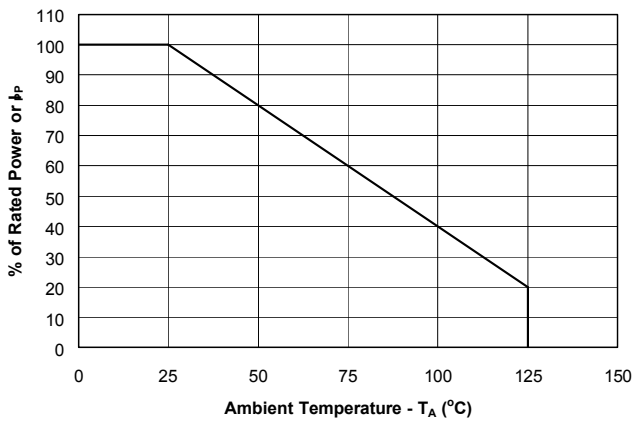
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				3.3	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2µA	3.5			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20µs			7	V
Clamping Voltage	V_C	I_{PP} = 10A, tp = 8/20µs			15	V
Junction Capacitance	C_j	Between I/O pins and Ground V_R = 0V, f = 1MHz		6	10	pF
		Between I/O pins V_R = 0V, f = 1MHz		3		pF

Typical Characteristics

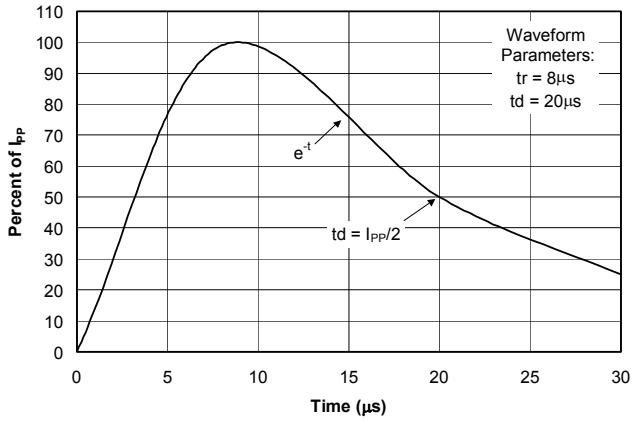
Non-Repetitive Peak Pulse Power vs. Pulse Time



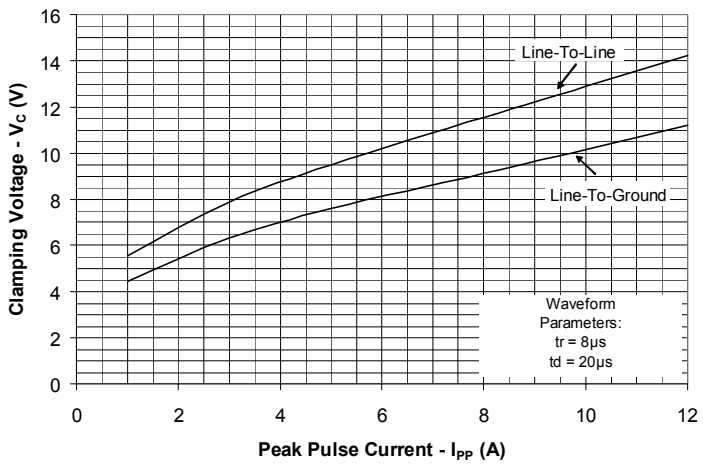
Power Derating Curve



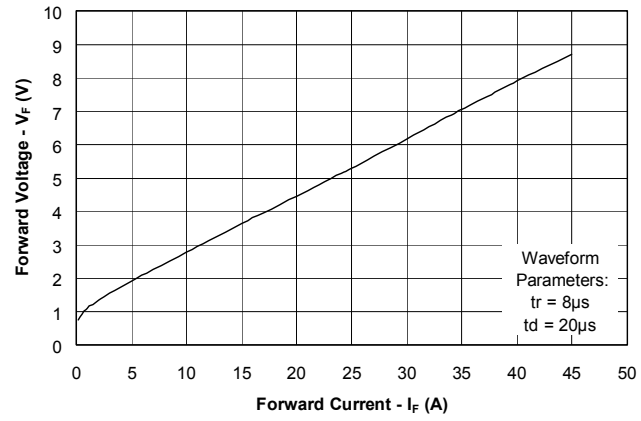
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Applications Information

Device Connection Options for Protection of Two High-Speed Data Lines

The SR3.3 TVS is designed to protect two data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 2 and 3. The negative reference (REF1) is connected at pin 1. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.
The positive reference (REF2) is connected at pin 4. The options for connecting the positive reference are as follows:

Note that pins 4 is connected internally to the cathode of the low voltage TVS. It is not recommended that this pin be directly connected to a DC source greater than the snap-back votlage (V_{SB}) as the device can latch on as described below.

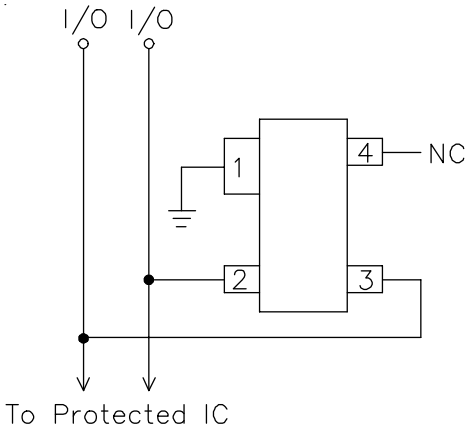
EPD TVS Characteristics

These devices are constructed using Semtech's proprietary EPD technology. By utilizing the EPD technology, the SR3.3 can effectively operate at 3.3V while maintaining excellent electrical characteristics.

The EPD TVS employs a complex nppn structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. Since the EPD TVS devices use a 4-layer structure, they exhibit a slightly different IV characteristic curve when compared to conventional devices. During normal operation, the device represents a high-impedance to the circuit up to the device working voltage (V_{RWM}). During an ESD event, the device will begin to conduct and will enter a low impedance state when the punch through voltage (V_{PT}) is exceeded. Unlike a conventional device, the low voltage TVS will exhibit a slight negative resistance characteristic as it conducts current. This characteristic aids in lowering the clamping voltage of the device, but must be considered in applications where DC voltages are present.

When the TVS is conducting current, it will exhibit a slight "snap-back" or negative resistance

Data Line Protection Using Internal TVS Diode as Reference



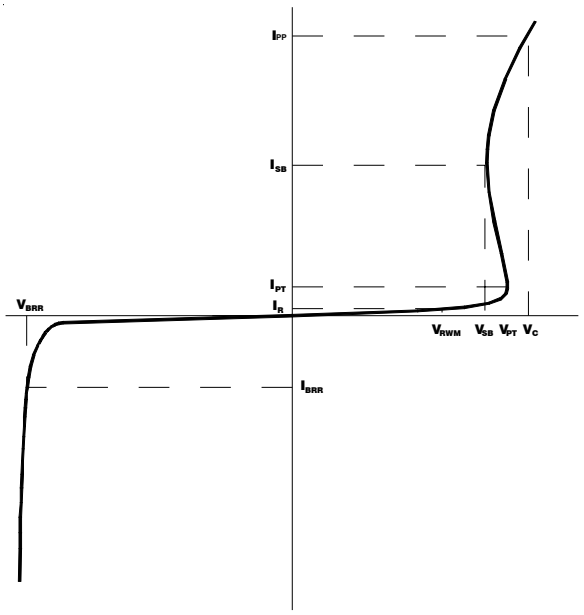


Figure 1 - EPD TVS IV Characteristic Curve

characteristics due to its structure. This point is defined on the curve by the snap-back voltage (V_{SB}) and snap-back current (I_{SB}). To return to a non-conducting state, the current through the device must fall below the I_{SB} (approximately <50mA) and the voltage must fall below the V_{SB} (normally 2.8 volts for a 3.3V device). If a 3.3V TVS is connected to 3.3V DC source, it will never fall below the snap-back voltage of 2.8V and will therefore stay in a conducting state.

Applications Information *(continued)*

Board Layout Considerations for ESD Protection

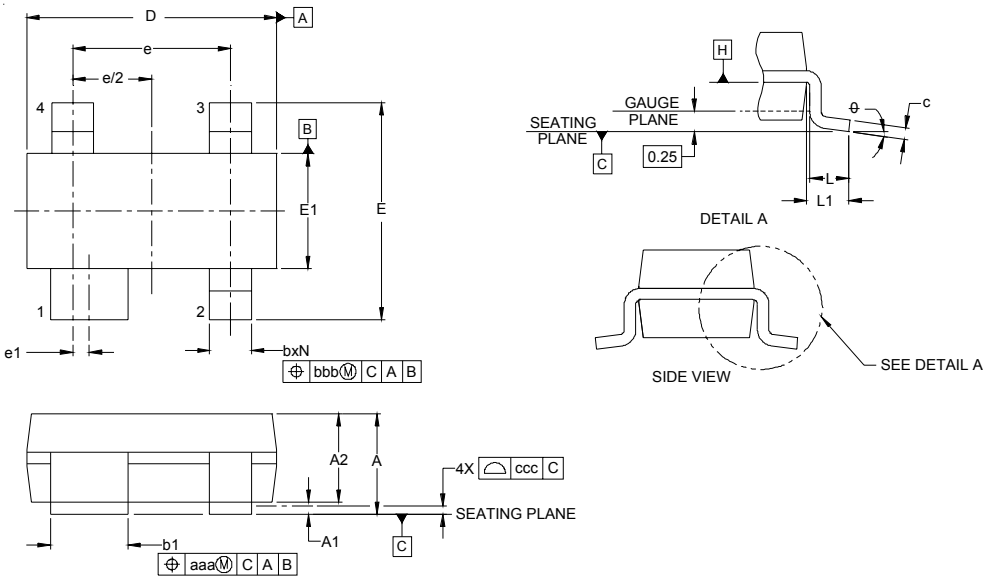
Board layout plays an important role in the suppression of extremely fast rise-time ESD transients. Recall that the voltage developed across an inductive load is proportional to the time rate of change of current through the load (V = L di/dt). The total clamping voltage seen by the protected load will be the sum of the TVS clamping voltage and the voltage due to the parasitic inductance ($V_{C(TOT)} = V_C + L\ di/dt$) . ***Parasitic inductance in the protection path can result in significant voltage overshoot, reducing the effectiveness of the suppression circuit.*** An ESD induced transient for example reaches a peak in approximately 1ns. For a 30A pulse (per IEC 61000-4-2 Level 4), 1nH of series inductance will increase the effective clamping voltage by 30V
($V = 1x10^{-9}\ (30/1x10^{-9})$). For maximum effectiveness, the following board layout guidelines are recommended:

- Minimize the path length between the SR3.3 and the protected line.
- Place the SR3.3 near the RJ45 connector to restrict transient coupling in nearby traces.
- Minimize the path length (inductance) between the RJ45 connector and the SR3.3.

Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Outline Drawing - SOT-143

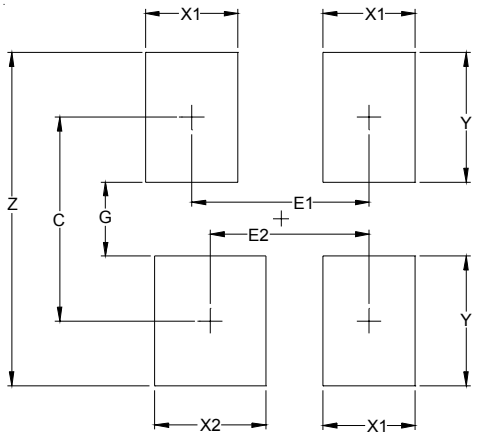


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.048	0.80	-	1.22
A1	.000	-	.006	0.013	-	0.15
A2	.029	.035	.042	0.75	0.90	1.07
b	.011	-	.020	0.30	-	0.51
b1	.029	-	.037	0.76	-	0.94
c	.003	-	.008	0.08	-	0.20
D	.110	.114	.120	2.80	2.90	3.04
E	.082	.093	.104	2.10	2.37	2.64
E1	.047	.051	.055	1.20	1.30	1.40
e	.075			1.92 BSC		
e1	.008			0.20 BSC		
L	.015	.020	.024	0.40	0.50	0.60
L1	(.021)			(0.54)		
N	4			4		
θ	0°	-	8°	0°	-	8°
aaa	.006			0.15		
bbb	.008			0.20		
ccc	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD TO-253, VARIATION D.

Land Pattern - SOT-143



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.087)	(2.20)
E1	.076	1.92
E2	.068	1.72
G	.031	0.80
X1	.039	1.00
X2	.047	1.20
Y	.055	1.40
Z	.141	3.60

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A.

Marking Codes

Part Number	Marking Code
SR3.3	R3.3

Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
SR3.3.TC	SnPb	3,000	7 Inch
SR3.3.TCT	Pb Free	3,000	7 Inch

Contact Information

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