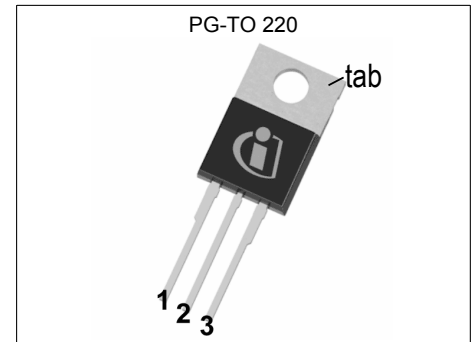


## MOSFET

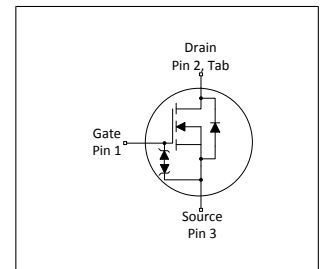
### 600V CoolMOS™ P7 Power Transistor

The CoolMOS™ 7th generation platform is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The 600V CoolMOS™ P7 series is the successor to the CoolMOS™ P6 series. It combines the benefits of a fast switching SJ MOSFET with excellent ease of use, e.g. very low ringing tendency, outstanding robustness of body diode against hard commutation and excellent ESD capability. Furthermore, extremely low switching and conduction losses make switching applications even more efficient, more compact and much cooler.



### Features

- Suitable for hard and soft switching (PFC and LLC) due to an outstanding commutation ruggedness
- Significant reduction of switching and conduction losses
- Excellent ESD robustness >2kV (HBM) for all products
- Better RDS(on)/package products compared to competition enabled by a low RDS(on)\*A (below 1Ohm\*mm<sup>2</sup>)
- Large portfolio with granular RDS(on) selection qualified for a variety of industrial and consumer grade applications according to JEDEC (J-STD20 and JESD22)



### Benefits

- Ease of use and fast design-in through low ringing tendency and usage across PFC and PWM stages
- Simplified thermal management due to low switching and conduction losses
- Increased power density solutions enabled by using products with smaller footprint and higher manufacturing quality due to >2 kV ESD protection
- Suitable for a wide variety of applications and power ranges



### Applications

PFC, hard switching PWM and resonant switching power stages. e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom & UPS

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	180	mΩ
$Q_{g,typ}$	25	nC
$I_{D,pulse}$	53	A
$E_{oss@400V}$	2.6	μJ
Body diode di/dt	900	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPP60R180P7	PG-TO 220-3	60R180P7	see Appendix A

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	4
Electrical characteristics .....	5
Electrical characteristics diagrams .....	7
Test Circuits .....	11
Package Outlines .....	12
Appendix A .....	13
Revision History .....	14
Trademarks .....	14
Disclaimer .....	14

## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	18 11	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	53	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	56	mJ	$I_D=4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.28	mJ	$I_D=4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	4.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	80	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	72	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	$I_S$	-	-	18	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	53	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 18\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	900	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 18\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	-	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.50$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_g$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	1.74	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	-	°C/W	-
Soldering temperature, wavesoldering only allowed at leads	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{V}$ , $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$ , $I_D=0.28\text{mA}$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=600$ , $V_{GS}=0\text{V}$ , $T_j=25^\circ\text{C}$ $V_{DS}=600$ , $V_{GS}=0\text{V}$ , $T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	1000	nA	$V_{GS}=20\text{V}$ , $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.145 0.341	0.180 -	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=5.6\text{A}$ , $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$ , $I_D=5.6\text{A}$ , $T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	11	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1081	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Output capacitance	$C_{oss}$	-	19	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=400\text{V}$ , $f=250\text{kHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	33	-	pF	$V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	314	-	pF	$I_D=\text{constant}$ , $V_{GS}=0\text{V}$ , $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=5.6\text{A}$ , $R_G=10\Omega$ ; see table 9
Rise time	$t_r$	-	12	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=5.6\text{A}$ , $R_G=10\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	85	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=5.6\text{A}$ , $R_G=10\Omega$ ; see table 9
Fall time	$t_f$	-	8	-	ns	$V_{DD}=400\text{V}$ , $V_{GS}=13\text{V}$ , $I_D=5.6\text{A}$ , $R_G=10\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{GS}$	-	6	-	nC	$V_{DD}=400\text{V}$ , $I_D=5.6\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate to drain charge	$Q_{gd}$	-	8	-	nC	$V_{DD}=400\text{V}$ , $I_D=5.6\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate charge total	$Q_g$	-	25	-	nC	$V_{DD}=400\text{V}$ , $I_D=5.6\text{A}$ , $V_{GS}=0$ to $10\text{V}$
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	$V_{DD}=400\text{V}$ , $I_D=5.6\text{A}$ , $V_{GS}=0$ to $10\text{V}$

<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=5.6A, T_j=25^\circ C$
Reverse recovery time	$t_{rr}$	-	175	-	ns	$V_R=400V, I_F=2A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	1.3	-	$\mu C$	$V_R=400V, I_F=2A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	15	-	A	$V_R=400V, I_F=2A, di_F/dt=100A/\mu s$ ; see table 8

### 4 Electrical characteristics diagrams

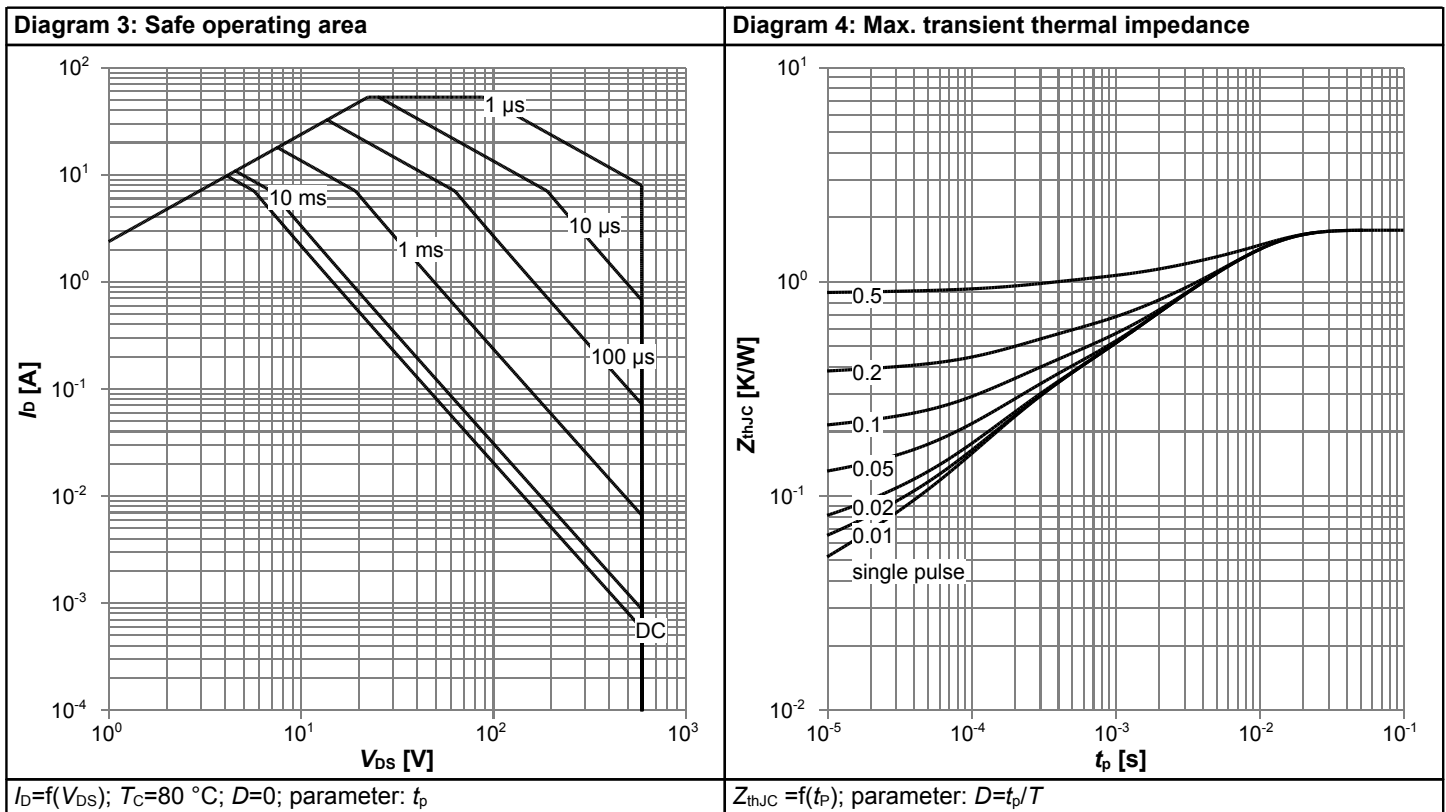
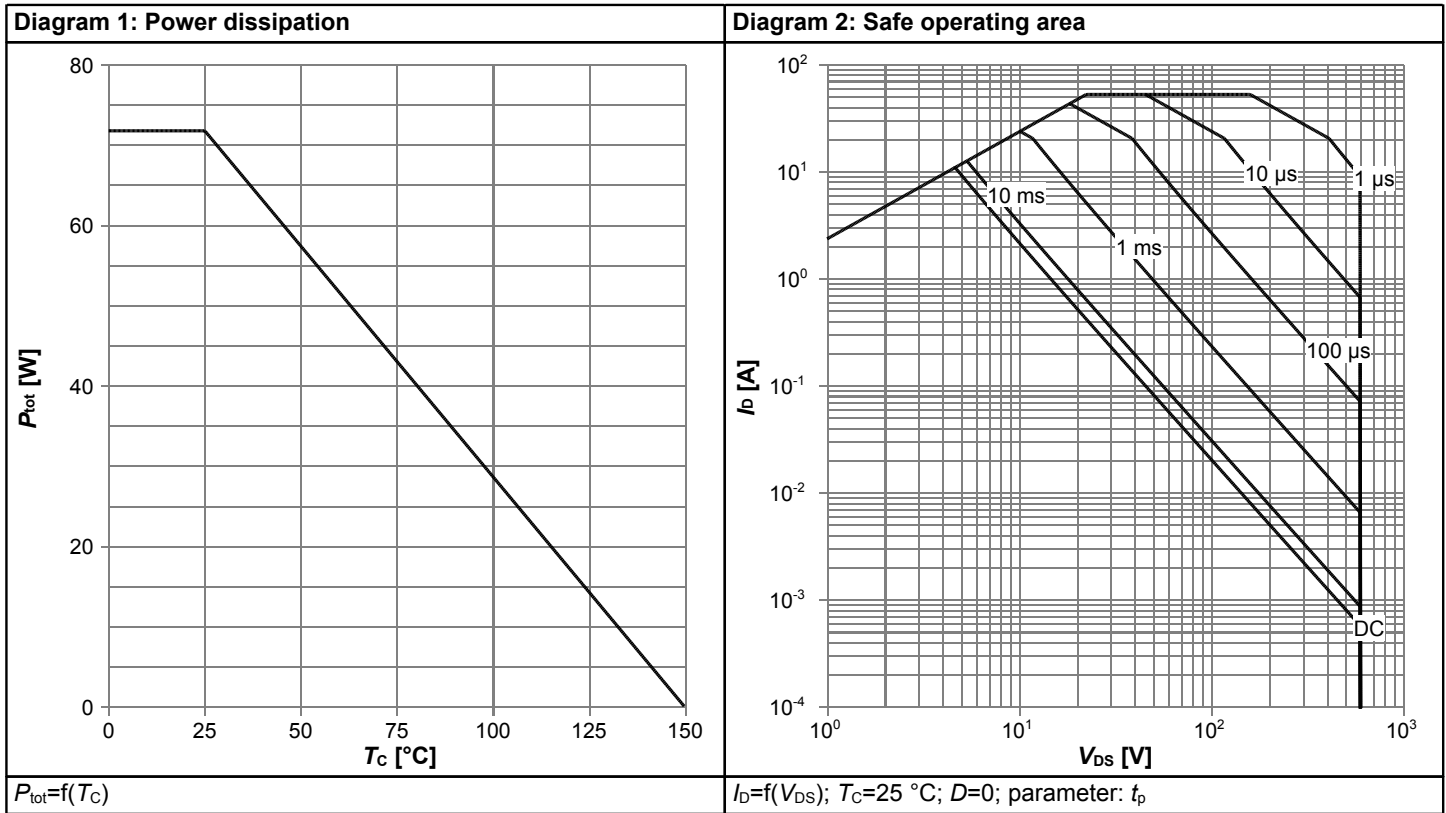
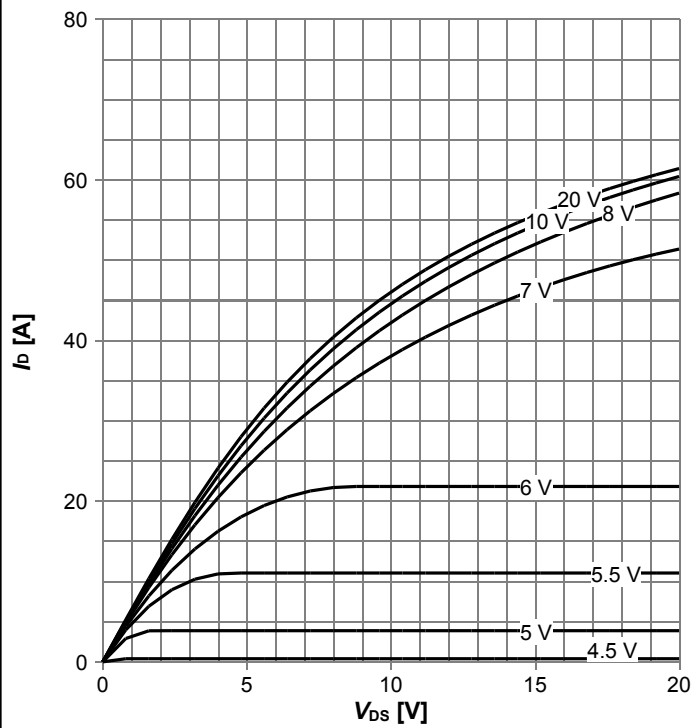
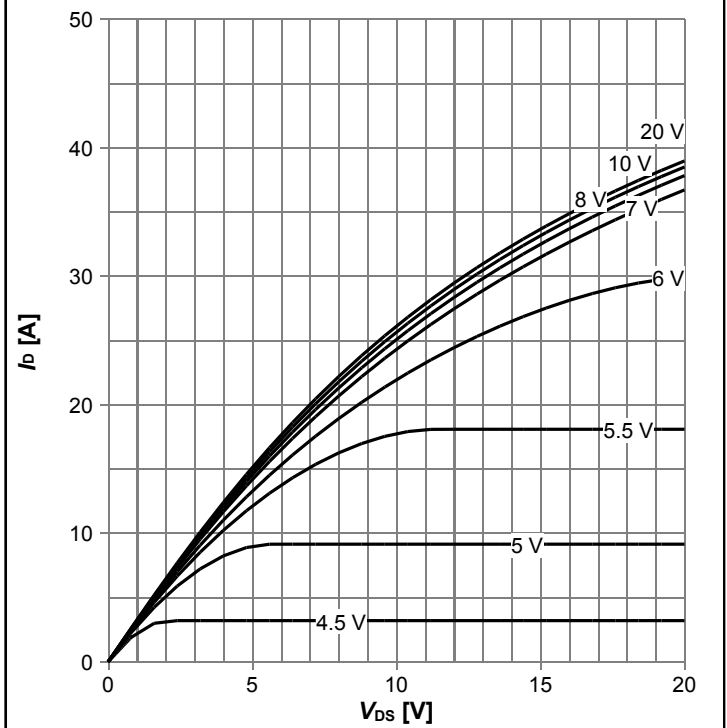


Diagram 5: Typ. output characteristics



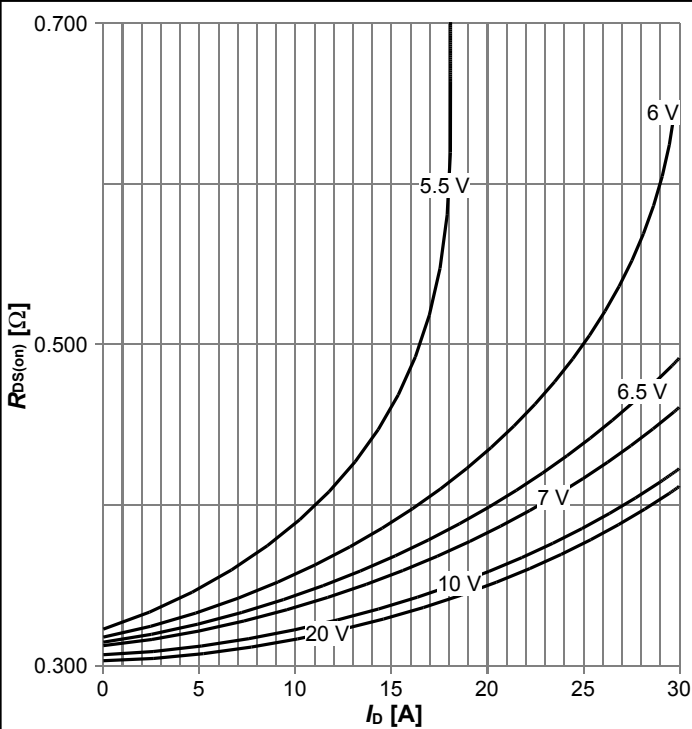
$I_D=f(V_{DS})$ ;  $T_j=25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



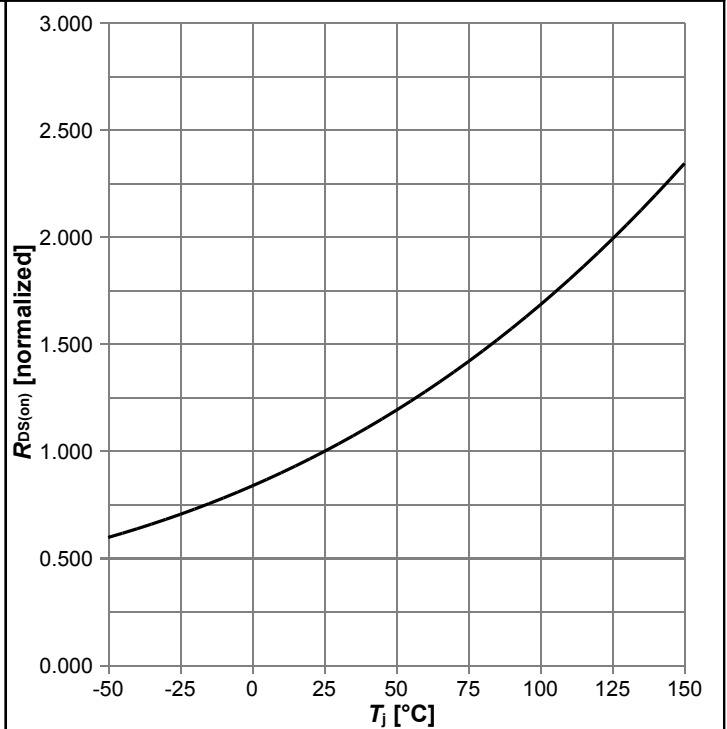
$I_D=f(V_{DS})$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D)$ ;  $T_j=125\text{ °C}$ ; parameter:  $V_{GS}$

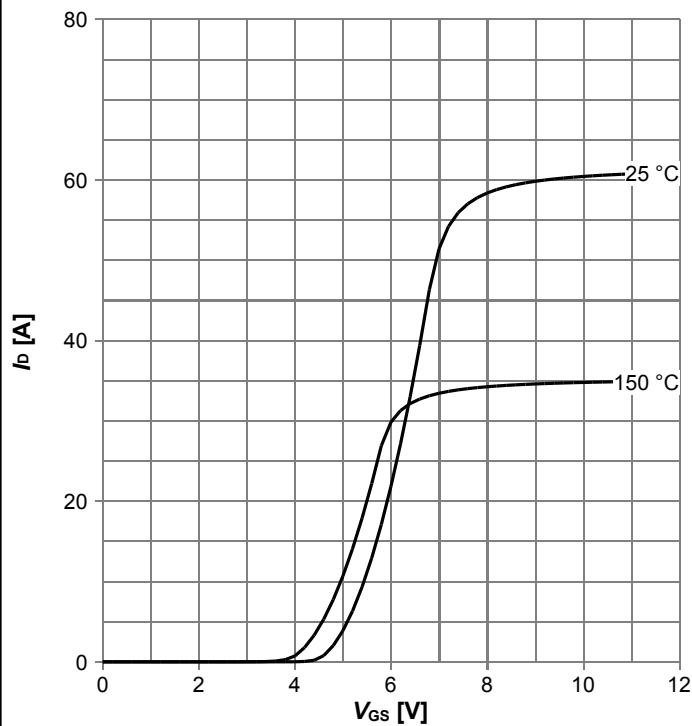
Diagram 8: Drain-source on-state resistance



$R_{DS(on)}=f(T_j)$ ;  $I_D=5.6\text{ A}$ ;  $V_{GS}=10\text{ V}$

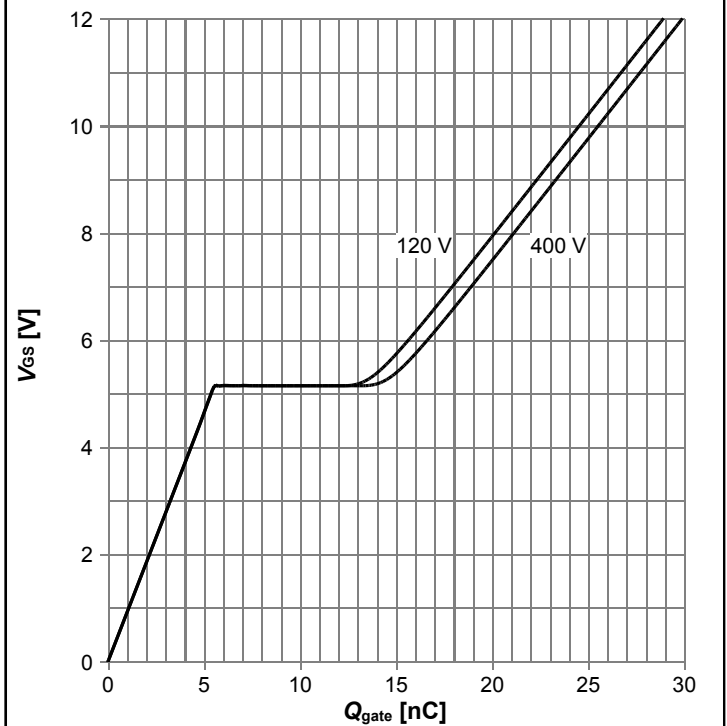


Diagram 9: Typ. transfer characteristics



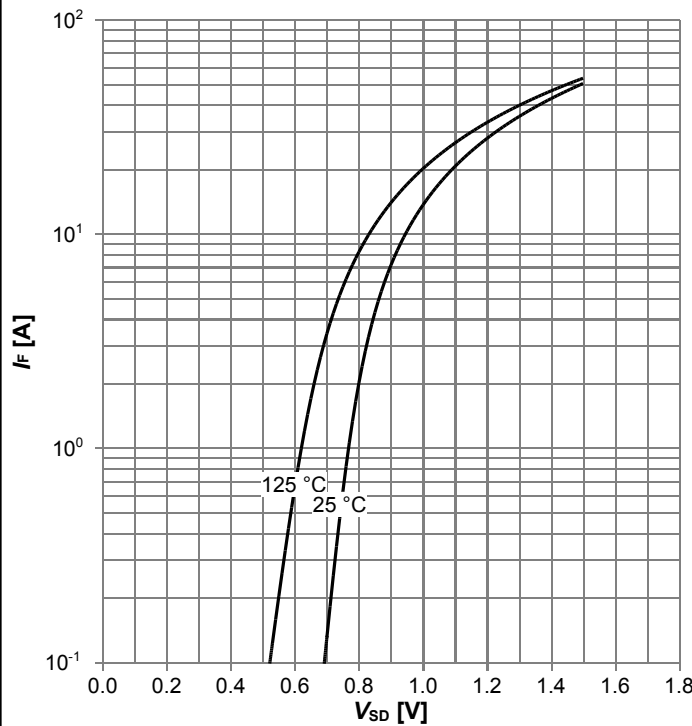
$I_D = f(V_{GS})$ ;  $V_{DS} = 20V$ ; parameter:  $T_j$

Diagram 10: Typ. gate charge



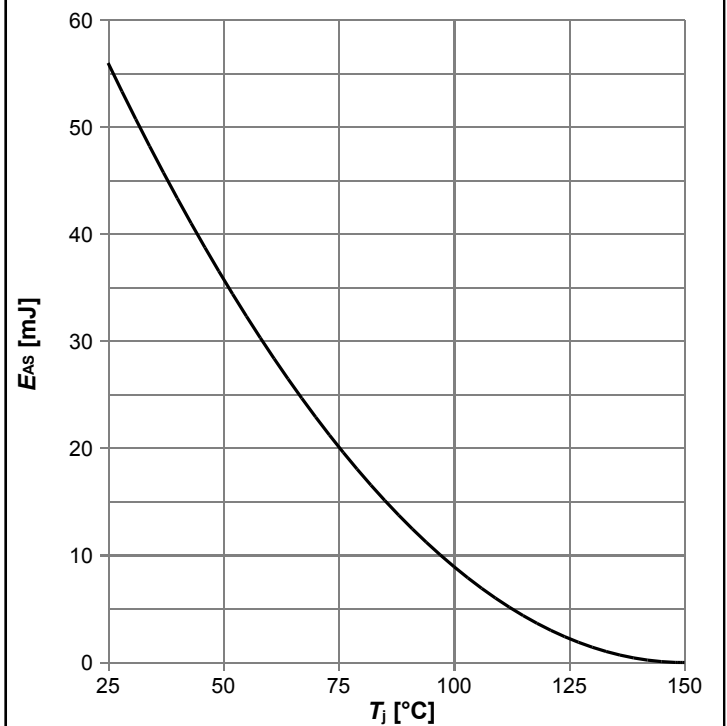
$V_{GS} = f(Q_{gate})$ ;  $I_D = 5.6 A$  pulsed; parameter:  $V_{DD}$

Diagram 11: Forward characteristics of reverse diode



$I_F = f(V_{SD})$ ; parameter:  $T_j$

Diagram 12: Avalanche energy



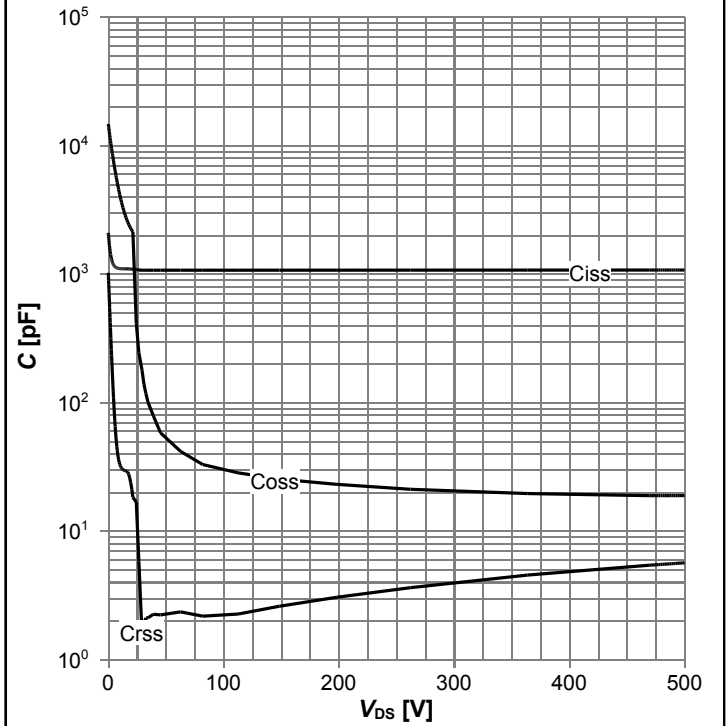
$E_{AS} = f(T_j)$ ;  $I_D = 4.0 A$ ;  $V_{DD} = 50 V$

**Diagram 13: Drain-source breakdown voltage**



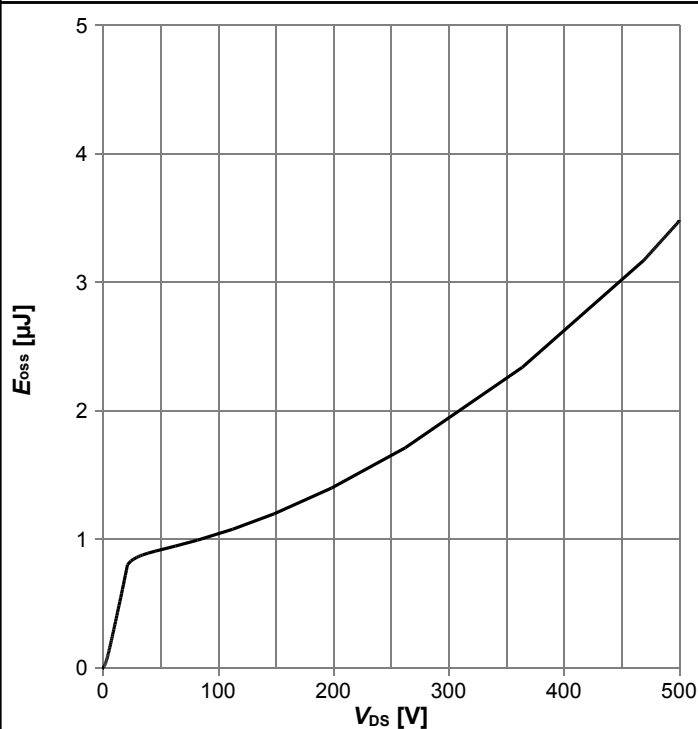
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

**Diagram 15: Typ. Coss stored energy**



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
<p><math>R_{g1} = R_{g2}</math></p>	<p><math>t_{tr} = t_F + t_S</math>  <math>Q_{tr} = Q_F + Q_S</math></p>

**Table 9 Switching times**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load**

Unclamped inductive load test circuit	Unclamped inductive waveform

**6 Package Outlines**



**Figure 1 Outline PG-TO 220-3, dimensions in mm/inches**

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS™ P7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ P7 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ P7 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

### Revision History

IPP60R180P7

**Revision: 2017-02-17, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-02-03	Release of final version
2.1	2017-02-17	Modified Safe Operating Area diagrams on page 7

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