19-1636; Rev 3; 8/05

EVALUATION KIT AVAILABLE

MAXIM

Dynamically Adjustable, Synchronous Step-Down Controller for Notebook CPUs

General Description

The MAX1717 step-down controller is intended for core CPU DC-DC converters in notebook computers. It features a dynamically adjustable output, ultra-fast transient response, high DC accuracy, and high efficiency needed for leading-edge CPU core power supplies. Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The output voltage can be dynamically adjusted through the 5-bit digital-to-analog converter (DAC) inputs over a 0.925V to 2V range. A unique feature of the MAX1717 is an internal multiplexer (mux) that accepts two 5-bit DAC settings with only five digital input pins. Output voltage transitions are accomplished with a proprietary precision slew-rate control that minimizes surge currents to and from the battery while guaranteeing "just-in-time" arrival at the new DAC setting.

High DC precision is enhanced by a two-wire remote-sensing scheme that compensates for voltage drops in the ground bus and output voltage rail. Alternatively, the remote-sensing inputs can be used together with the MAX1717's high DC accuracy to implement a voltage-positioned circuit that modifies the load-transient response to reduce output capacitor requirements and full-load power dissipation.

Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the +5V system supply instead of the battery) at a higher switching frequency allows the minimum possible physical size.

The MAX1717 is available in a 24-pin QSOP package.

Applications

Notebook Computers with SpeedStep™ or Other Dynamically Adjustable Processors

2-Cell to 4-Cell Li+ Battery to CPU Core Supply Converters

5V to CPU Core Supply Converters

Pin Configuration appears at end of data sheet.

Quick-PWM is a trademark of Maxim Integrated Products.
SpeedStep is a trademark of Intel Corp.

Features

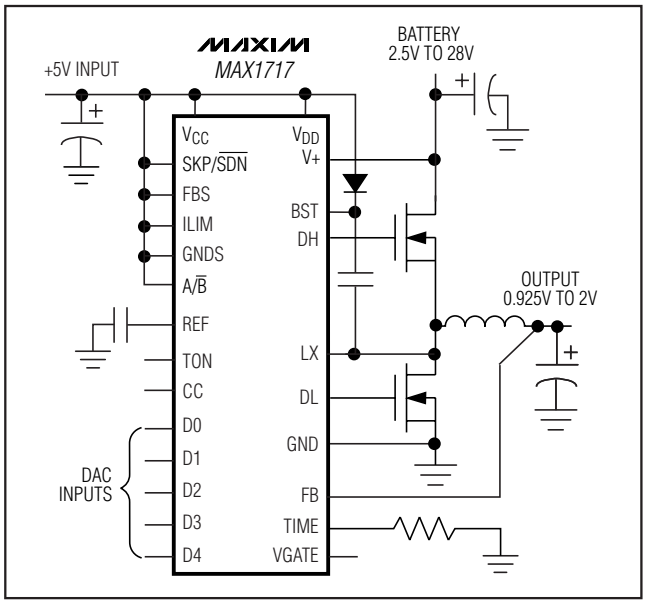
- ♦ **Quick-PWM Architecture**
- ♦ **±1% V_{OUT} Accuracy Over Line and Load**
- ♦ **5-Bit On-Board DAC with Input Mux**
- ♦ **Precision-Adjustable V_{OUT} Slew Control**
- ♦ **0.925V to 2V Output Adjust Range**
- ♦ **Supports Voltage-Positioned Applications**
- ♦ **2V to 28V Battery Input Range**
- ♦ **Requires a Separate +5V Bias Supply**
- ♦ **200/300/550/1000kHz Switching Frequency**
- ♦ **Over/Undervoltage Protection**
- ♦ **Drives Large Synchronous-Rectifier FETs**
- ♦ **700µA (typ) I_{CC} Supply Current**
- ♦ **2µA (typ) Shutdown Supply Current**
- ♦ **2V ±1% Reference Output**
- ♦ **VGATE Transition-Complete Indicator**
- ♦ **Small 24-Pin QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1717EEG	-40°C to +85°C	24 QSOP
MAX1717EEG+	-40°C to +85°C	24 QSOP

+ Denotes lead-free package.

Minimal Operating Circuit



Dynamically Adjustable, Synchronous Step-Down Controller for Notebook CPUs

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +30V
V_{CC}, V_{DD} to GND .....-0.3V to +6V
D0–D4, A/$\overline{B}$, VGATE, to GND .....-0.3V to +6V
SKP/$\overline{SDN}$ to GND .....-0.3V to +16V
ILIM, FB, FBS, CC, REF, GNDS, TON, TIME to GND .....-0.3V to (V_{CC} + 0.3V)
DL to GND .....-0.3V to (V_{DD} + 0.3V)
BST to GND .....-0.3V to +36V
DH to LX .....-0.3V to (BST + 0.3V)
LX to BST .....-6V to +0.3V
REF Short Circuit to GND .....Continuous
Continuous Power Dissipation
24-Pin QSOP (derate 9.5mW/°C above +70°C).....762mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range	Battery voltage, V+		2		28	V
	V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy (Note 1)	V+ = 4.5V to 28V, includes load regulation error	DAC codes from 1.3V to 2V	-1		1	%
		DAC codes from 0.925V to 1.275V	-1.2		1.2	%
Remote Sense Voltage Error	FB to FBS or GNDS to GND = 0 to 25mV			3		mV
Line Regulation Error	V_{CC} = 4.5V to 5.5V, V_{BATT} = 4.5V to 28V			5		mV
FB Input Resistance			115	180	265	kΩ
FBS Input Bias Current			-0.2		0.2	µA
GNDS Input Bias Current			-1		1	µA
TIME Frequency Accuracy	150kHz nominal, R_{TIME} = 120kΩ		-8		+8	%
	380kHz nominal, R_{TIME} = 47kΩ		-12		+12	
	38kHz nominal, R_{TIME} = 470kΩ		-12		+12	
On-Time (Note 2)	V+ = 5V, FB = 2V, TON = GND (1000kHz)		375	425	475	ns
	V+ = 24V, FB = 2V	TON = REF (550kHz)	135	155	173	
		TON = open (300kHz)	260	289	318	
		TON = V_{CC} (200kHz)	375	418	461	
Minimum Off-Time (Note 2)	TON = V_{CC}, open, or REF (200kHz, 300kHz, or 550kHz)			400	500	ns
Minimum Off-Time (Note 2)	TON = GND (1000kHz)			300	375	ns
BIAS AND REFERENCE						
Quiescent Supply Current (V_{CC})	Measured at V_{CC}, FB forced above the regulation point			700	1200	µA
Quiescent Supply Current (V_{DD})	Measured at V_{DD}, FB forced above the regulation point			<1	5	µA
Quiescent Battery Supply Current (V+)				25	40	µA
Shutdown Supply Current (V_{CC})	SKP/$\overline{SDN}$ = 0			2	5	µA
Shutdown Supply Current (V_{DD})	SKP/$\overline{SDN}$ = 0			<1	5	µA
Shutdown Battery Supply Current (V+)	SKP/$\overline{SDN}$ = 0, V_{CC} = V_{DD} = 0 or 5V			<1	5	µA
Reference Voltage	V_{CC} = 4.5V to 5.5V, no REF load		1.98	2	2.02	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Load Regulation	I_{REF} = 0 to 50µA				0.01	V
REF Sink Current	REF in regulation		10			µA
FAULT PROTECTION						
Overvoltage Trip Threshold	Measured at FB		2.20	2.25	2.30	V
Overvoltage Fault Propagation Delay	FB forced 2% above trip threshold			10		µs
Output Undervoltage Fault Protection Threshold	With respect to unloaded output voltage		65	70	75	%
Output Undervoltage Fault Propagation Delay	FB forced 2% below trip threshold			10		µs
Output Undervoltage Fault Blanking Time	From SKP/$\overline{SDN}$ signal going high, clock speed set by R_{TIME}			256		clks
Current-Limit Threshold (Positive, Default)	GND - LX, ILIM = V_{CC}	T_A = +25°C to +85°C	90	100	110	mV
		T_A = 0°C to +85°C	85		115	
Current-Limit Threshold (Positive, Adjustable)	GND - LX	ILIM = 0.5V	35	50	65	mV
		ILIM = REF (2V)	165	200	230	
Current-Limit Threshold (Negative)	LX - GND, ILIM = V_{CC}		-140	-110	-80	mV
Current-Limit Threshold (Zero Crossing)	GND - LX			4		mV
Current-Limit Default Switchover Threshold			3	V_{CC} - 1	V_{CC} - 0.4	V
Thermal Shutdown Threshold	Hysteresis = 10°C			150		°C
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V
VGATE Lower Trip Threshold	Measured at FB with respect to unloaded output voltage, rising edge, hysteresis = 1%		-8	-6.5	-5	%
VGATE Upper Trip Threshold	Measured at FB with respect to unloaded output voltage, rising edge, hysteresis = 1%		+10	+12	+14	%
VGATE Propagation Delay	FB forced 2% outside VGATE trip threshold			10		µs
VGATE Transition Delay	After X = Y, clock speed set by R_{TIME}			1		clk
VGATE Output Low Voltage	I_{SINK} = 1mA				0.4	V
VGATE Leakage Current	High state, forced to 5.5V				1	µA
GATE DRIVERS						
DH Gate Driver On-Resistance	BST - LX forced to 5V			1.0	3.5	Ω
DL Gate Driver On-Resistance	DL, high state (pullup)			1.0	3.5	Ω
	DL, low state (pulldown)			0.4	1.0	
DH Gate-Driver Source/Sink Current	DH forced to 2.5V, BST - LX forced to 5V			1.3		A
DL Gate-Driver Sink Current	DL forced to 2.5V			4		A

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DL Gate-Driver Source Current	DL forced to 2.5V			1.3		A
Dead Time	DL rising			35		ns
	DH rising			26		
LOGIC AND I/O						
Logic Input High Voltage	D0–D4, A/$\overline{B}$		2.4			
Logic Input Low Voltage	D0–D4, A/$\overline{B}$				0.8	
DAC B-Mode Programming Resistor, Low	D0–D4, 0 to 0.4V or 2.6V to 5.5V applied through resistor, A/$\overline{B}$ = GND				1.05	
DAC B-Mode Programming Resistor, High	D0–D4, 0 to 0.4V or 2.6V to 5.5V applied through resistor, A/$\overline{B}$ = GND		95			kΩ
D0–D4 Pullup/Pulldown	Entering B mode	Pull up		40		kΩ
		Pull down		8		
Logic Input Current	D0–D4, A/$\overline{B}$ = 5V		-1		1	µA
	A/$\overline{B}$		-1		1	
TON Input Levels	For TON = V_{CC} (200kHz operation)		V_{CC} - 0.4			V
	For TON = open (300kHz operation)		3.15		3.85	
	For TON = REF (550kHz operation)		1.65		2.35	
	For TON = GND (1000kHz operation)				0.5	
SKP/$\overline{SDN}$ and TON Input Current	SKP/$\overline{SDN}$, TON forced to GND or V_{CC}		-3		3	µA
SKP/$\overline{SDN}$ Input Levels	SKP/$\overline{SDN}$ = logic high (SKIP mode)		2.8		6	V
	SKP/$\overline{SDN}$ = open (PWM mode)		1.8		2.2	
	SKP/$\overline{SDN}$ = logic low (shutdown mode)				0.5	
	To enable no-fault mode		12		15	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Output Voltage Accuracy (Note 1)	V+ = 4.5V to 28V, includes load regulation error	DAC codes from 1.3V to 2V	-1.5		1.5	%
		DAC codes from 0.925V to 1.275V	-1.7		1.7	
TIME Frequency Accuracy	150kHz nominal, R_{TIME} = 120kΩ		-8		+8	%
	380kHz nominal, R_{TIME} = 47kΩ		-12		+12	
	38kHz nominal, R_{TIME} = 470kΩ		-12		+12	
On-Time (Note 2)	V+ = 5V, FB = 2V, TON = GND (1000kHz)		375		475	ns
On-Time (Note 2)	V+ = 24V, FB = 2V	TON = REF (550kHz)	136		173	ns
		TON = open (300kHz)	260		318	
		TON = V_{CC} (200kHz)	365		471	
Minimum Off-Time (Note 2)	TON = V_{CC}, open, or REF (200kHz, 300kHz, or 550kHz)				500	ns
Minimum Off-Time (Note 2)	TON = GND (1000kHz)				375	ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = +15V, V_{CC} = V_{DD} = SKP/$\overline{SDN}$ = +5V, V_{OUT} =1.6V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current (V_{CC})	Measured at V_{CC}, FB forced above the regulation point				1200	µA
Quiescent Supply Current (V_{DD})	Measured at V_{DD}, FB forced above the regulation point				5	µA
Quiescent Battery Supply Current (V+)					40	µA
Shutdown Supply Current (V_{CC})	SKP/$\overline{SDN}$ = 0				5	µA
Shutdown Supply Current (V_{DD})	SKP/$\overline{SDN}$ = 0				5	µA
Shutdown Battery Supply Current (V+)	SKP/$\overline{SDN}$ = 0, V_{CC} = V_{DD} = 0 or 5V				5	µA
Reference Voltage	V_{CC} = 4.5V to 5.5V, no REF load		1.98		2.02	V
Overvoltage Trip Threshold	Measured at FB		2.20		2.30	V
Output Undervoltage Protection Threshold	With respect to unloaded output voltage		65		75	%
Current-Limit Threshold (Positive, Default)	GND - LX, ILIM = V_{CC}		80		115	mV
Current-Limit Threshold (Positive, Adjustable)	GND - LX	ILIM = 0.5V	33		65	mV
		ILIM = REF (2V)	160		240	
Current-Limit Threshold (Negative)	LX - GND, ILIM = V_{CC}		-140		-80	mV
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V
DH Gate Driver On-Resistance	BST - LX forced to 5V				3.5	Ω
DL Gate Driver On-Resistance	DL, high state (pullup)				3.5	Ω
	DL, low state (pulldown)				1.0	Ω
Logic Input High Voltage	D0–D4, A/$\overline{B}$		2.4			V
Logic Input Low Voltage	D0–D4, A/$\overline{B}$				0.8	V
DAC B-Mode Programming Resistor, Low	D0–D4, 0 to 0.4V or 2.6V to 5.5V applied through resistor, A/$\overline{B}$ = GND				1	kΩ
DAC B-Mode Programming Resistor, High	D0–D4, 0 to 0.4V or 2.6V to 5.5V applied through resistor, A/$\overline{B}$ = GND		100			kΩ
VGATE Lower Trip Threshold	Measured at FB with respect to unloaded output voltage, falling edge, hysteresis = 1%		-8.4		-4.6	%
VGATE Upper Trip Threshold	Measured at FB with respect to unloaded output voltage, rising edge, hysteresis = 1%		+10		+15	%

Note 1: Output voltage accuracy specifications apply to DAC voltages from 0.925V to 2V. Includes load-regulation error.

Note 2: On-Time specifications are measured from 50% to 50% at the DH pin, with LX forced to 0, BST forced to 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

Note 3: Specifications to -40°C are guaranteed by design and not production tested.

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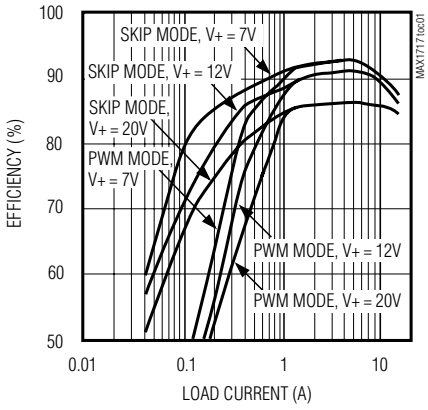
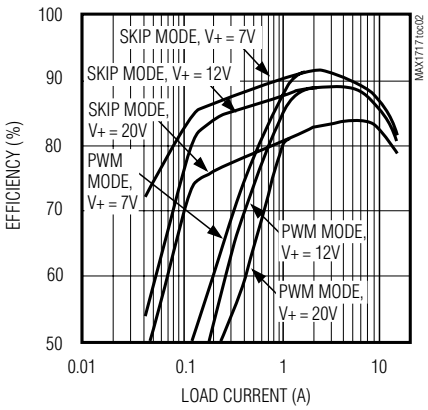
Typical Operating Characteristics

(Circuit of Figure 1, components of Table 1, V+ = +12V, V_{DD} = V_{CC} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, T_A = +25°C, unless otherwise noted.)

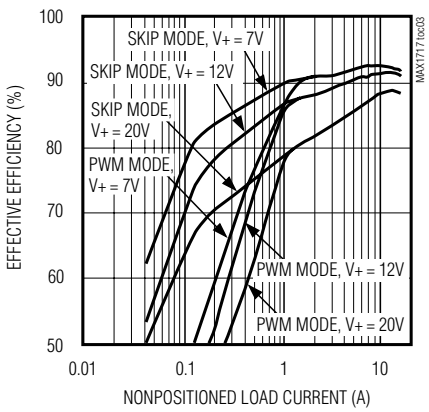
EFFICIENCY vs. LOAD CURRENT 300kHz STANDARD APPLICATION, CIRCUIT 1



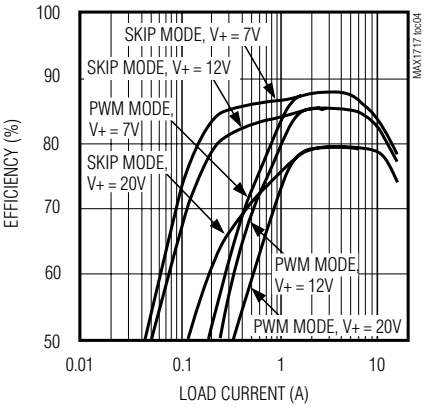
EFFICIENCY vs. LOAD CURRENT 300kHz VOLTAGE POSITIONED, CIRCUIT 2



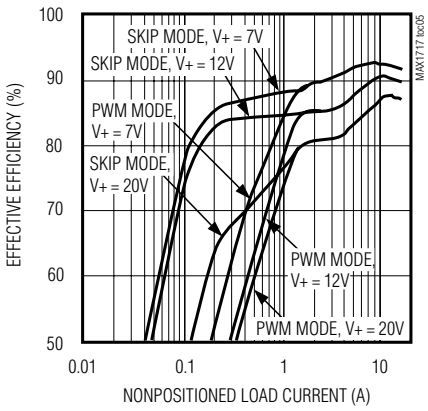
EFFECTIVE EFFICIENCY vs. LOAD CURRENT 300kHz VOLTAGE POSITIONED, CIRCUIT 2



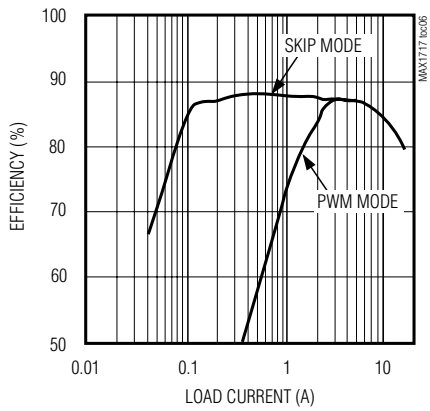
EFFICIENCY vs. LOAD CURRENT 550kHz VOLTAGE POSITIONED, CIRCUIT 3



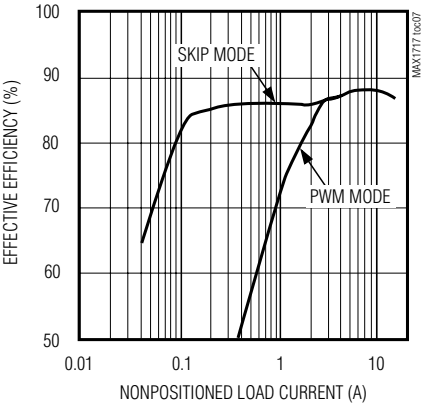
EFFECTIVE EFFICIENCY vs. LOAD CURRENT 550kHz VOLTAGE POSITIONED, CIRCUIT 3



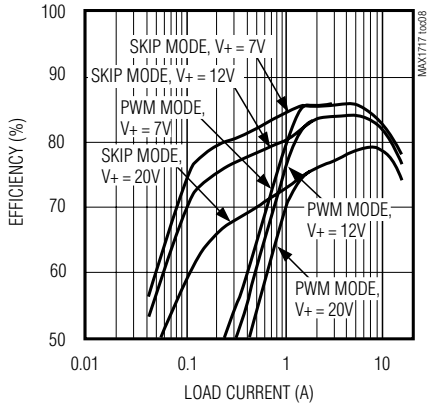
EFFICIENCY vs. LOAD CURRENT 1000kHz, +5V, CIRCUIT 4



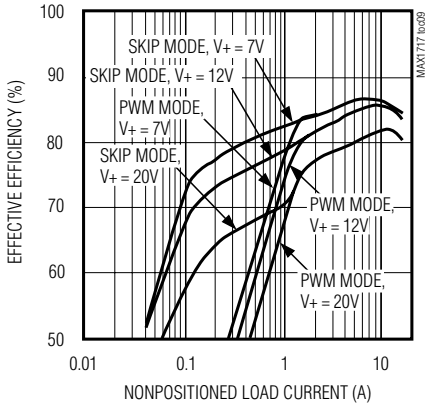
EFFECTIVE EFFICIENCY vs. LOAD CURRENT 1000kHz, +5V, CIRCUIT 4



EFFICIENCY vs. LOAD CURRENT 1000kHz VOLTAGE POSITIONED, CIRCUIT 5



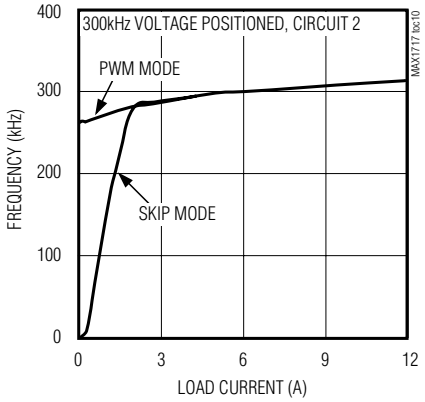
EFFECTIVE EFFICIENCY vs. LOAD CURRENT 1000kHz VOLTAGE POSITIONED, CIRCUIT 5



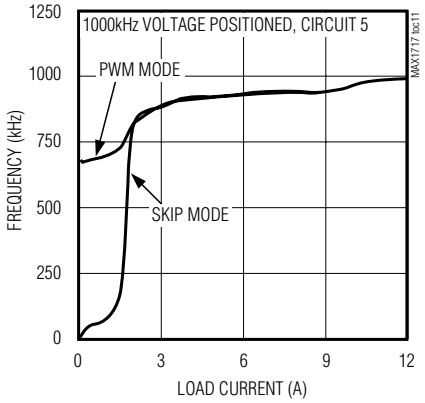
Typical Operating Characteristics (continued)

(Circuit of Figure 1, components of Table 1, V+ = +12V, V_{DD} = V_{CC} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, T_A = +25°C, unless otherwise noted.)

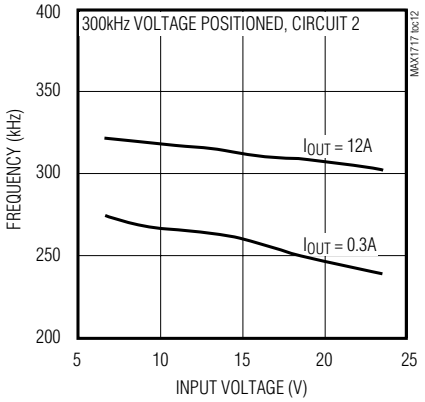
FREQUENCY vs. LOAD CURRENT



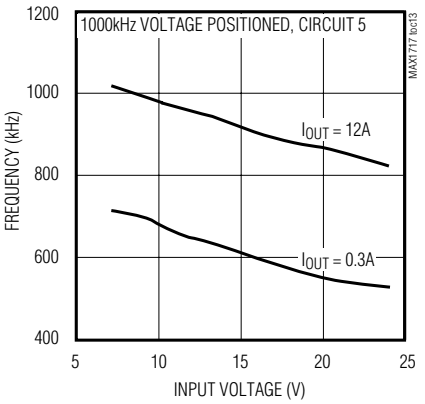
FREQUENCY vs. LOAD CURRENT



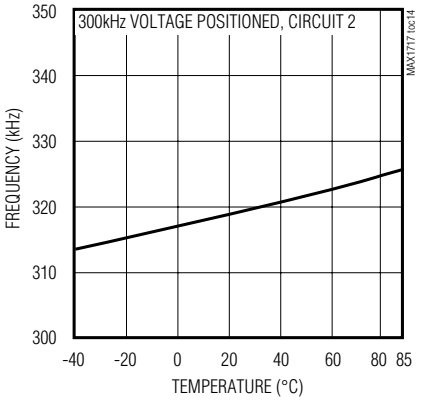
FREQUENCY vs. INPUT VOLTAGE



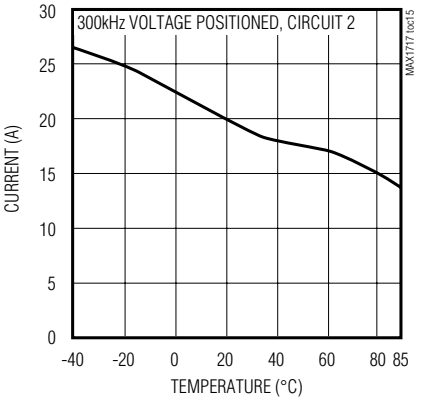
FREQUENCY vs. INPUT VOLTAGE



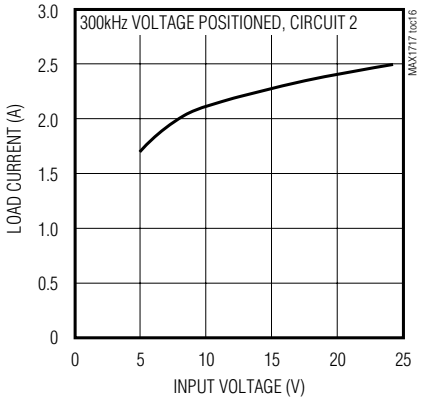
FREQUENCY vs. TEMPERATURE



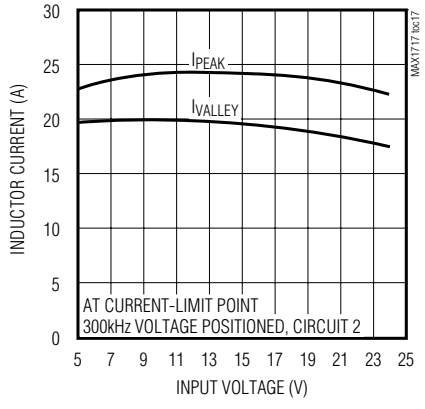
OUTPUT CURRENT AT CURRENT LIMIT vs. TEMPERATURE



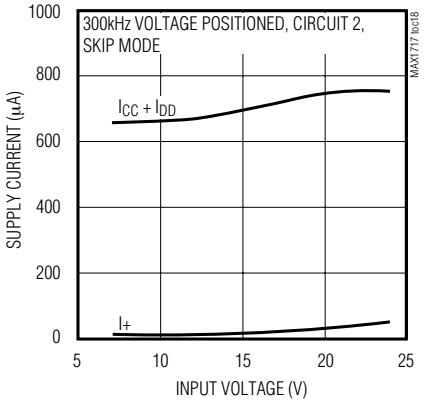
CONTINUOUS-TO-DISCONTINUOUS INDUCTOR CURRENT POINT



INDUCTOR CURRENT PEAKS AND VALLEYS vs. INPUT VOLTAGE



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE

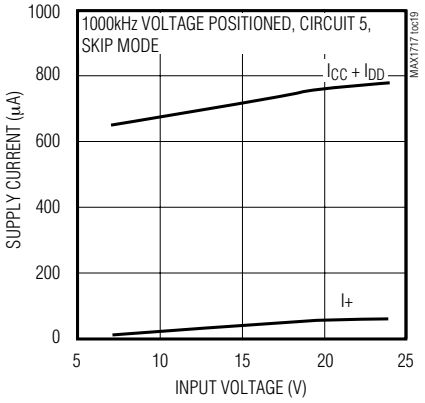


Dynamically Adjustable, Synchronous Step-Down Controller for Notebook CPUs

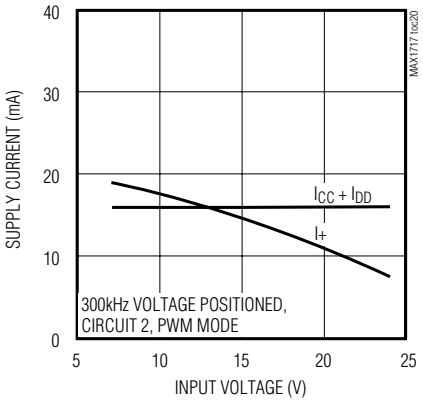
Typical Operating Characteristics (continued)

(Circuit of Figure 1, components of Table 1, V+ = +12V, V_{DD} = V_{CC} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, T_A = +25°C, unless otherwise noted.)

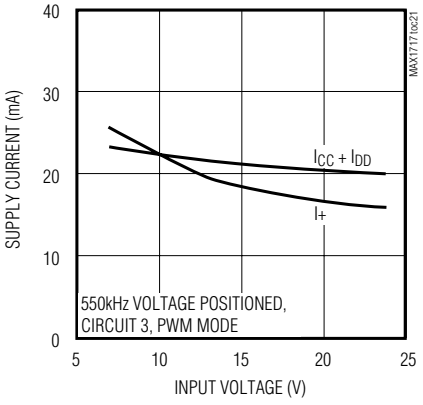
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



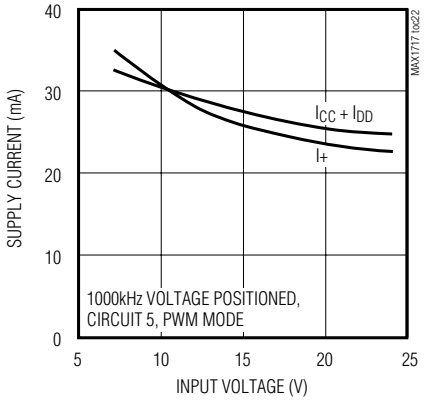
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



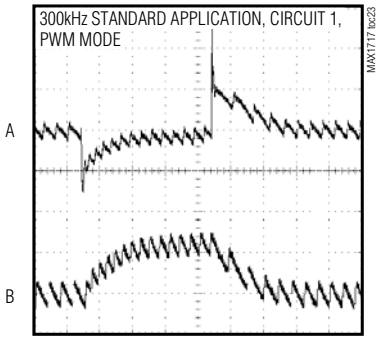
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



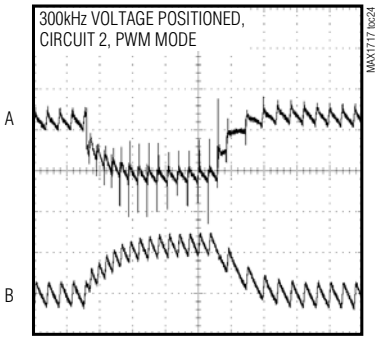
LOAD-TRANSIENT RESPONSE



10µs/div

A = V_{OUT}, 50mV/div, AC-COUPLED
B = INDUCTOR CURRENT, 10A/div

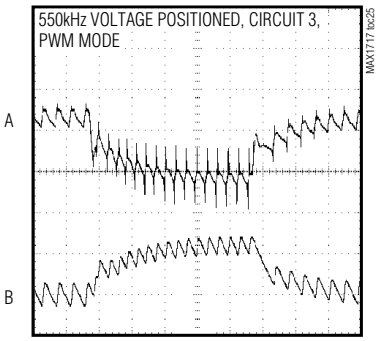
LOAD-TRANSIENT RESPONSE



10µs/div

A = V_{OUT}, 50mV/div, AC-COUPLED
B = INDUCTOR CURRENT, 10A/div

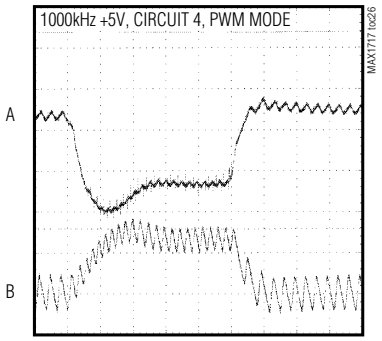
LOAD-TRANSIENT RESPONSE



5µs/div

A = V_{OUT}, 50mV/div, AC-COUPLED
B = INDUCTOR CURRENT, 10A/div

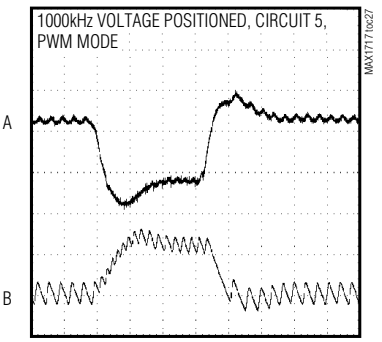
LOAD-TRANSIENT RESPONSE



4µs/div

A = V_{OUT}, 50mV/div, AC-COUPLED
B = INDUCTOR CURRENT, 10A/div

LOAD-TRANSIENT RESPONSE



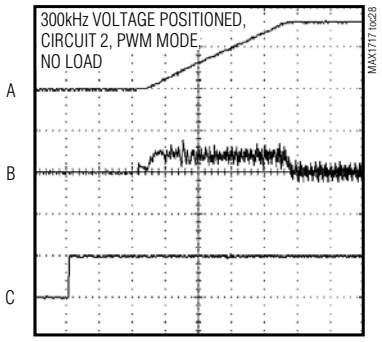
4µs/div

A = V_{OUT}, 50mV/div, AC-COUPLED
B = INDUCTOR CURRENT, 10A/div

Typical Operating Characteristics (continued)

(Circuit of Figure 1, components of Table 1, V+ = +12V, V_{DD} = V_{CC} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, T_A = +25°C, unless otherwise noted.)

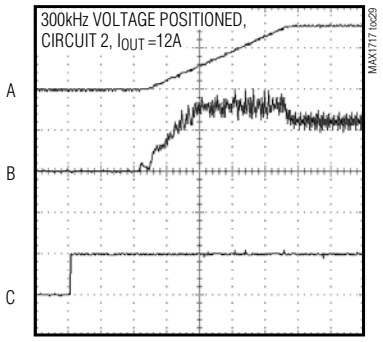
STARTUP WAVEFORM



100µs/div

A = V_{OUT}, 1V/div
B = INDUCTOR CURRENT, 10A/div
C = SKP/$\overline{SDN}$, 5V/div

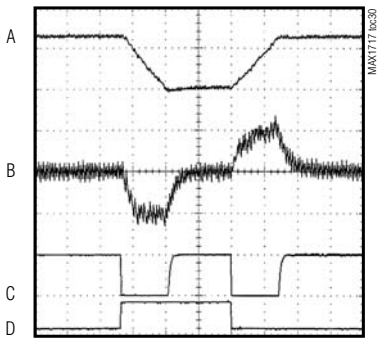
STARTUP WAVEFORM



100µs/div

A = V_{OUT}, 1V/div
B = INDUCTOR CURRENT, 10A/div
C = SKP/$\overline{SDN}$, 5V/div

DYNAMIC OUTPUT VOLTAGE TRANSITION

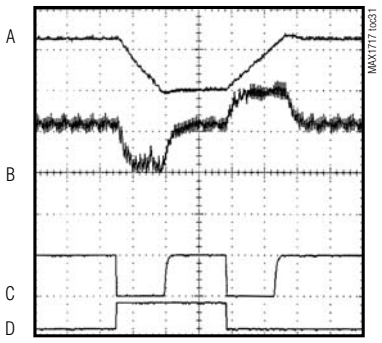


50µs/div

300kHz STANDARD APPLICATION, CIRCUIT 1,
PWM MODE, V_{OUT} = 1.35V TO 1.6V, I_{OUT} = 0.3A,
R_{TIME} = 120kΩ

A = V_{OUT}, 200mV/div, AC-COUPLED
B = INDUCTOR CURRENT, 10A/div
C = VGATE, 5V/div
D = A/$\overline{B}$, 5V/div

DYNAMIC OUTPUT VOLTAGE TRANSITION

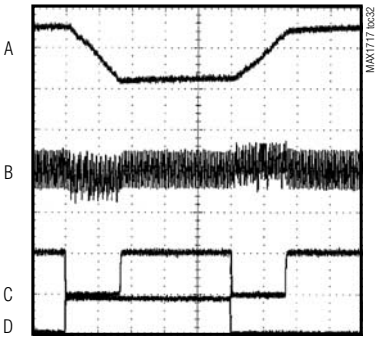


50µs/div

300kHz STANDARD APPLICATION, CIRCUIT 1,
PWM MODE, V_{OUT} = 1.35V TO 1.6V,
I_{OUT} = 12A, R_{TIME} = 120kΩ

A = V_{OUT}, 200mV/div, AC-COUPLED
B = INDUCTOR CURRENT, 10A/div
C = VGATE, 5V/div
D = A/$\overline{B}$, 5V/div

DYNAMIC OUTPUT VOLTAGE TRANSITION

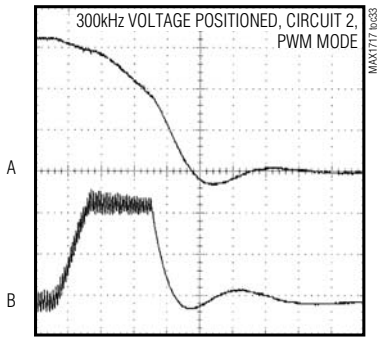


20µs/div

A = V_{OUT}, 200mV/div, AC-COUPLED
B = INDUCTOR CURRENT, 10A/div
C = VGATE, 5V/div
D = A/$\overline{B}$, 5V/div

1000kHz +5V, CIRCUIT 4,
PWM MODE, V_{OUT} = 1.35V TO 1.6V,
I_{OUT} = 0.3A, R_{TIME} = 51kΩ

OUTPUT OVERLOAD WAVEFORM



40µs/div

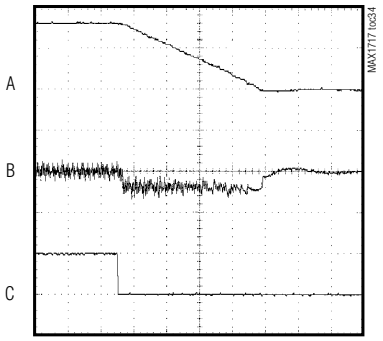
A = V_{OUT}, 500mV/div
B = INDUCTOR CURRENT, 10A/div

Dynamically Adjustable, Synchronous Step-Down Controller for Notebook CPUs

Typical Operating Characteristics (continued)

(Circuit of Figure 1, components of Table 1, V+ = +12V, V_{DD} = V_{CC} = SKP/$\overline{SDN}$ = +5V, V_{OUT} = 1.6V, T_A = +25°C, unless otherwise noted.)

SHUTDOWN WAVEFORM

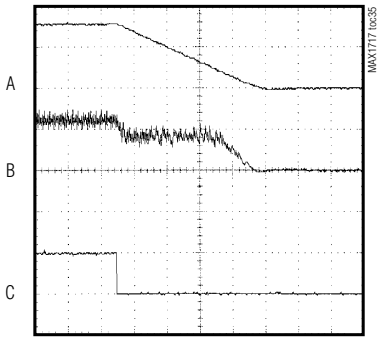


100µs/div

300kHz VOLTAGE POSITIONED, CIRCUIT 2,
PWM MODE, NO LOAD

A = V_{OUT}, 1V/div
B = INDUCTOR CURRENT, 10A/div
C = SKP/$\overline{SDN}$, 5V/div

SHUTDOWN WAVEFORM



100µs/div

300kHz VOLTAGE POSITIONED, CIRCUIT 2,
PWM MODE, I_{OUT} = 12A

A = V_{OUT}, 1V/div
B = INDUCTOR CURRENT, 10A/div
C = SKP/$\overline{SDN}$, 5V/div

Pin Description

PIN	NAME	FUNCTION
1	V+	Battery Voltage Sense Connection. Connect V+ to input power source. V+ is used only for PWM one-shot timing. DH on-time is inversely proportional to input voltage over a range of 2V to 28V.
2	SKP/$\overline{SDN}$	Combined Shutdown and Skip-Mode Control. Drive SKP/$\overline{SDN}$ to GND for shutdown. Leave SKP/$\overline{SDN}$ open for low-noise forced-PWM mode, or drive to V_{CC} for normal pulse-skipping operation. Low-noise forced-PWM mode causes inductor current recirculation at light loads and suppresses pulse-skipping operation. SKP/$\overline{SDN}$ can also be used to disable over/undervoltage protection circuits and clear the fault latch by forcing it to 12V < SKP/$\overline{SDN}$ < 15V (with otherwise normal PFM/PWM operation). Do not connect SKP/$\overline{SDN}$ to > 15V.
3	TIME	Slew-Rate Adjustment Pin. Connect a resistor from TIME to GND to set the internal slew-rate clock. A 470kΩ to 47kΩ resistor sets the clock from 38kHz to 380kHz, f_{SLEW} = 150kHz x 120kΩ / R_{TIME}.
4	FB	Fast Feedback Input. Connect FB to the junction of the external inductor and output capacitor for nonvoltage-positioned circuits (Figure 1). For voltage-positioned circuits, connect FB to the junction of the external inductor and the positioning resistor (Figure 3).
5	FBS	Feedback Remote-Sense Input. For nonvoltage-positioned circuits, connect FBS to V_{OUT} directly at the load. FBS internally connects to the integrator that fine tunes the DC output voltage. For voltage-positioned circuits, connect FBS directly to FB near the IC to disable the FBS remote-sense integrator amplifier. To disable all three integrator amplifiers, connect FBS to V_{CC}.
6	CC	Integrator Capacitor Connection. Connect a 100pF to 1000pF (470pF typ) capacitor from CC to GND to set the integration time constant. CC can be left open if FBS is tied to V_{CC}.
7	V_{CC}	Analog Supply Voltage Input for PWM Core. Connect V_{CC} to the system supply voltage (4.5V to 5.5V) with a series 20Ω resistor. Bypass to GND with a 0.22µF (min) capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
8	TON	On-Time Selection Control Input. This is a four-level input that sets the K factor (Table 3) to determine DH on-time. Connect TON to the following pins for the indicated operation: GND = 1000kHz REF = 550kHz Open = 300kHz V_{CC} = 200kHz
9	REF	2V Reference Output. Bypass to GND with 0.22µF (min) capacitor. Can source 50µA for external loads. Loading REF degrades FB accuracy according to the REF load-regulation error.
10	ILIM	Current-Limit Adjustment. The GND - LX current-limit threshold defaults to 100mV if ILIM is tied to V_{CC}. In adjustable mode, the current-limit threshold voltage is 1/10th the voltage seen at ILIM over a 0.5V to 3.0V range. The logic threshold for switchover to the 100mV default value is approximately V_{CC} - 1V. Tie ILIM to REF for a fixed 200mV threshold.
11	GNDS	Ground Remote-Sense Input. For nonvoltage-positioned circuits, connect GNDS to ground directly at the load. GNDS internally connects to the integrator that fine tunes the output voltage. The output voltage rises by an amount of GNDS - GND. For voltage-positioned circuits, increase the output voltage (24mV (typ)) by biasing GNDS with a resistor-divider from REF to GND.
12	VGATE	Open-Drain Power-Good Output. VGATE is normally high when the output is in regulation. VGATE goes low whenever the DAC code changes, and returns high one clock period after the slew-rate controller finishes and the output is in regulation. VGATE is low in shutdown.
13	GND	Analog and Power Ground. Also connects to the current-limit comparator.
14	DL	Low-Side Gate Driver Output. DL swings GND to V_{DD}.
15	V_{DD}	Supply Voltage Input for the DL Gate Driver, 4.5V to 5.5V. Bypass to GND with a 1µF capacitor.
16	A/$\overline{B}$	Internal MUX Select Input. When A/$\overline{B}$ is high, the DAC code is determined by logic-level voltages on D0–D4. On the falling edge of A/$\overline{B}$ (or during power-up with A/$\overline{B}$ low), the DAC code is determined by the resistor values at D0–D4.
17–21	D4–D0	DAC Code Inputs. D0 is the LSB and D4 is the MSB for the internal 5-bit DAC (see Table 4). When A/$\overline{B}$ is high, D0–D4 function as high-input-impedance logic inputs. On the falling edge of A/$\overline{B}$ (or during power-up with A/$\overline{B}$ low), the series resistance on each input sets its logic state as follows: (series resistance ≤ 1kΩ ±5%) = logic low (series resistance ≥ 100kΩ ±5%) = logic high
22	BST	Boost Flying Capacitor Connection. Connect BST to the external boost diode and capacitor as shown in the *Standard Application Circuit*. An optional resistor in series with BST allows the DH pullup current to be adjusted (Figure 5).
23	LX	Inductor Connection. LX is the internal lower supply rail for the DH high-side gate driver. It also connects to the current-limit comparator and the skip-mode zero-crossing comparator.
24	DH	High-Side Gate-Driver Output. DH swings LX to BST.

Dynamically Adjustable, Synchronous Step-Down Controller for Notebook CPUs

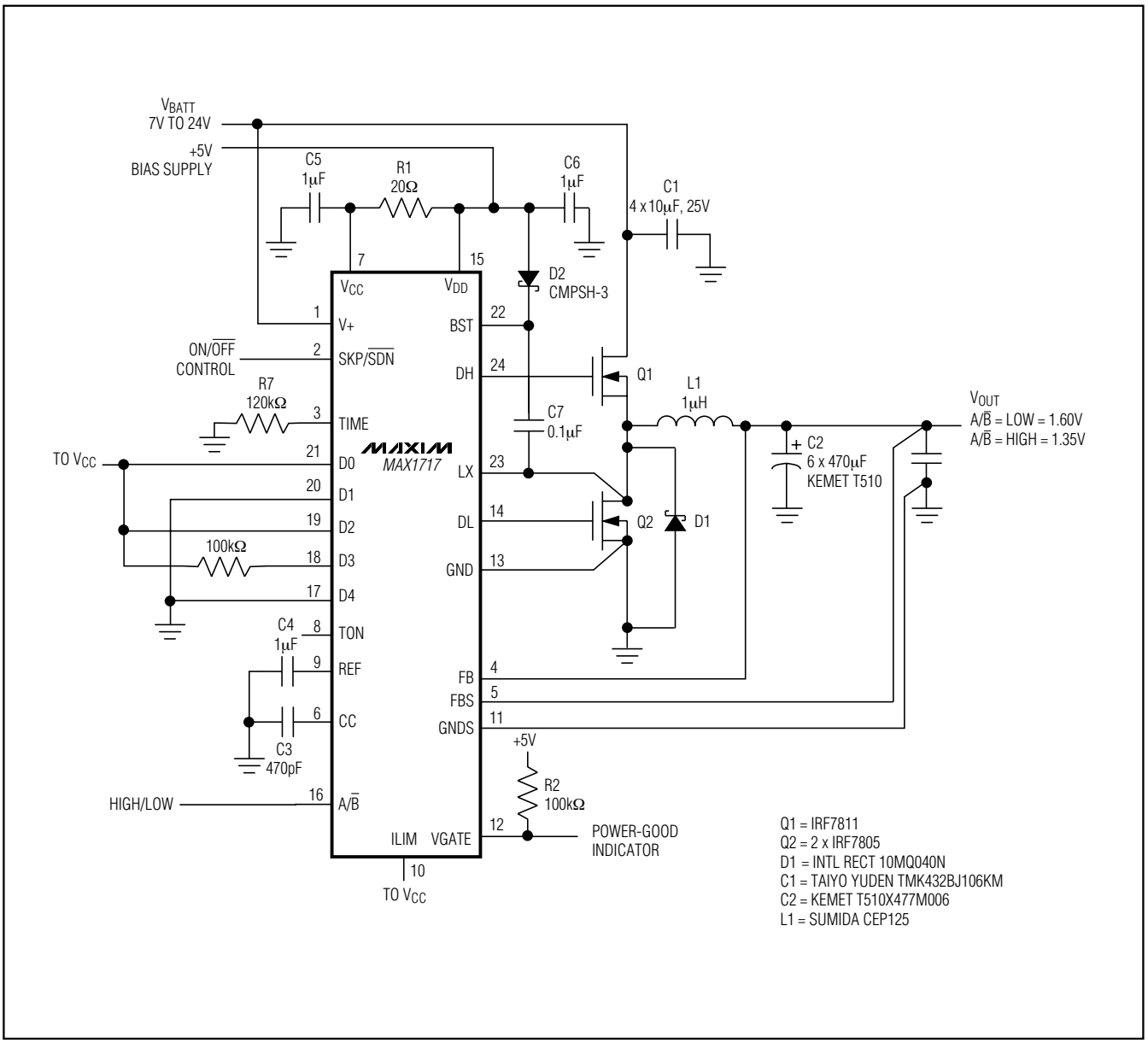


Figure 1. Standard Application Circuit

Table 1. Component Selection for Standard Applications

COMPONENT	300kHz, STANDARD APPLICATION, CIRCUIT 1	300kHz, VOLTAGE POSITIONED, CIRCUIT 2	550kHz, VOLTAGE POSITIONED, CIRCUIT 3	1000kHz, +5V, CIRCUIT 4	1000kHz, VOLTAGE POSITIONED, CIRCUIT 5
Figure Number	1	3	3	3	3
Input Range (V_{BATT})	7V to 24V	7V to 24V	7V to 24V	4.5V to 5.5V	7V to 24V
Output Current	14A	14A	14A	14A	14A
Frequency	300kHz	300kHz	550kHz	1000kHz	1000kHz
High-Side MOSFET Q1	International Rectifier IRF7811	International Rectifier IRF7811	International Rectifier IRF7811	International Rectifier IRF7811	International Rectifier IRF7811
Low-Side MOSFET Q2	(2) International Rectifier IRF7805, IRF7811, or IRF7811A	(2) International Rectifier IRF7805, IRF7811, or IRF7811A	(2) International Rectifier IRF7805, IRF7811, or IRF7811A	(2) International Rectifier IRF7805, IRF7811, or IRF7811A	(2) International Rectifier IRF7805, IRF7811, or IRF7811A
Input Capacitor C1	(4) 10µF, 25V ceramic Taiyo Yuden TMK432BJ106KM	(4) 10µF, 25V ceramic Taiyo Yuden TMK432BJ106KM	(4) 10µF, 25V ceramic Taiyo Yuden TMK432BJ106KM	(5) 22µF, 10V ceramic Taiyo Yuden LMK432BJ226KM	(4) 10µF, 25V ceramic Taiyo Yuden TMK432BJ106KM
Output Capacitor C2	(6) 470µF, 6.3V tantalum Kemet T510X477M006AS	(5) 220µF, 2.5V, 25mΩ specialty polymer Panasonic EEFUE0E221R	(4) 220µF, 2.5V, 25mΩ specialty polymer Panasonic EEFUE0E221R	(5) 47µF, 6.3V ceramic Taiyo Yuden JMK432BJ476MM	(5) 47µF, 6.3V ceramic Taiyo Yuden JMK432BJ476MM
Inductor L1	1µH Sumida CEP125-1R0MC or Panasonic ETQP6F1R1BFA	1µH Sumida CEP125-1R0MC or Panasonic ETQP6F1R1BFA	0.47µH Sumida CEP125-4712-T006	0.19µH Coilcraft X8357-A	0.3µH Sumida CEP12D38 4713-T001
Voltage-Positioning Resistor R6	—	5mΩ ±1%, 1W Dale WSL-2512-R005F	5mΩ ±1%, 1W Dale WSL-2512-R005F	5mΩ ±1%, 1W Dale WSL-2512-R005F	5mΩ ±1%, 1W Dale WSL-2512-R005F
Voltage-Positioning Offset	—	24mV	24mV	24mV	24mV
TON Level	Float	Float	REF	GND	GND

Dynamically Adjustable, Synchronous Step-Down Controller for Notebook CPUs

Table 2. Component Suppliers

MANUFACTURER	USA PHONE	FACTORY FAX [Country Code]
Coilcraft	847-639-6400	[1] 847-639-1469
Dale-Vishay	402-564-3131	[1] 402-563-6418
International Rectifier	310-322-3331	[1] 310-322-3332
Kemet	408-986-0424	[1] 408-986-1442
Panasonic	714-373-7939	[1] 714-373-7183
Sumida	847-956-0666	[81] 3-3607-5144
Taiyo Yuden	408-573-4150	[1] 408-573-4159

Detailed Description

+5V Bias Supply (V_{CC} and V_{DD})

The MAX1717 requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V supply can be generated with an external linear regulator.

The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f (Q_{G1} + Q_{G2}) = 10mA \text{ to } 40mA \text{ (typ)}$$

where I_{CC} is 700µA (typ), f is the switching frequency, and Q_{G1} and Q_{G2} are the MOSFET data sheet total gate-charge specification limits at V_{GS} = 5V.

V+ and V_{DD} can be tied together if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal (SKP/SDN going from low to high or open) must be delayed until the battery voltage is present to ensure startup.

Free-Running, Constant On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudofixed-frequency, constant-on-time current-mode type with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple.

$$\text{On-Time} = K (V_{OUT} + 0.075V) / V_{IN}$$

where K is set by the TON pin-strap connection and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch (Table 3).

The on-time one-shot has good accuracy at the operating points specified in the *Electrical Characteristics* (±10% at 200kHz and 300kHz, ±12% at 550kHz and 1000kHz). On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* can vary over a wide range. For example, the 1000kHz setting will typically run about 10% slower with inputs much greater than +5V due to the very short on-times required.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses in the output and ground tend to raise the switching frequency at higher output currents.

Table 3. Approximate K-Factors Errors

TON SETTING (kHz)	K FACTOR (µs)	APPROXIMATE K-FACTOR ERROR (%)	MIN RECOMMENDED V_{BATT} AT V_{OUT} = 1.6V (V)
200	5	±10	2.1
300	3.3	±10	2.3
550	1.8	±12.5	3.2
1000	1.0	±12.5	4.5

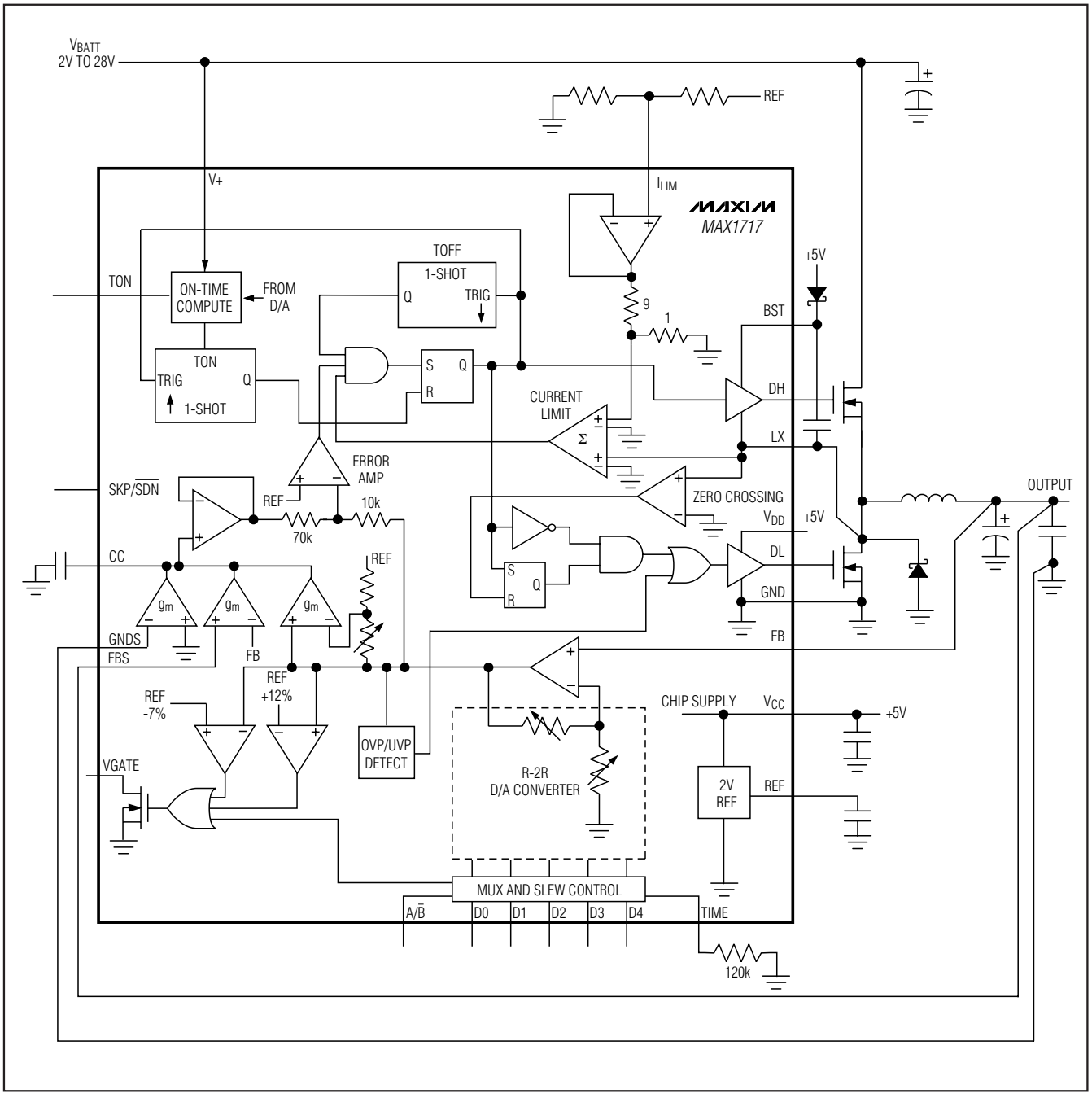


Figure 2. Functional Diagram

Dynamically Adjustable, Synchronous Step-Down Controller for Notebook CPUs

The dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in PWM mode (SKP/$\overline{SDN}$ = open) and dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time.

For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f = (V_{OUT} + V_{DROP1}) / t_{ON} (V_{IN} + V_{DROP1} - V_{DROP2})$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PC board resistances; t_{ON} is the on-time calculated by the MAX1717.

Integrator Amplifiers

Three integrator amplifiers provide a fine adjustment to the output regulation point. One amplifier integrates the difference between GNDS and GND, a second integrates the difference between FBS and FB. The third amplifier integrates the difference between REF and the DAC output. These three transconductance amplifiers' outputs are directly summed inside the chip, so the integration time constant can be set easily with one capacitor. The g_m of each amplifier is 160µS (typ).

The integrator block has the ability to lower the output voltage by 2% and raise it by 6%. For each amplifier, the differential input voltage range is at least ±70mV total, including DC offset and AC ripple. The integrator corrects for approximately 90% of the total error, due to finite gain.

The FBS amplifier corrects for DC voltage drops in PC board traces and connectors in the output bus path between the DC-DC converter and the load. The GNDS amplifier performs a similar DC correction task for the output ground bus. The third integrator amplifier corrects the small offset of the error amplifier and provides an averaging function that forces V_{OUT} to be regulated at the average value of the output ripple waveform.

Integrators have both beneficial and detrimental characteristics. Although they correct for drops due to DC bus resistance and tighten the DC output voltage tolerance limits by averaging the peak-to-peak output ripple, they can interfere with achieving the fastest possible load-transient response. The fastest transient response is achieved when all three integrators are disabled. This can work very well if the MAX1717 circuit is placed very close to the CPU.

All three integrators can be disabled by connecting FBS to V_{CC}. When the integrators are disabled, CC can be left unconnected, which eliminates a component, but leaves GNDS connected to any convenient ground. When the inductor is in continuous conduction, the output voltage will have a DC regulation higher than the trip level by 50% of the ripple. In discontinuous conduction (SKP/$\overline{SDN}$ open, light-loaded), the output voltage will have a DC regulation higher than the trip level by approximately 1.5% due to slope compensation.

There is often a connector, or at least many milliohms of PC board trace resistance, between the DC-DC converter and the CPU. In these cases, the best strategy is to place most of the bulk bypass capacitors close to the CPU, with just one capacitor on the other side of the connector near the MAX1717 to control ripple if the CPU card is unplugged. In this situation, the remote-sense lines (GNDS and FBS) and integrators provide a real benefit.

When operating the MAX1717 in a voltage-positioned circuit (Figure 3), GNDS can be offset with a resistor divider from REF to GND, which causes the GNDS integrator to increase the output voltage by 90% of the applied offset (27mV typ). A low-value (5mΩ typ) voltage-positioning resistor is added in series between the external inductor and the output capacitor. FBS is connected to FB directly at the junction of the external inductor and the voltage-positioning resistor. The net effect of these two changes is an output voltage that is slightly higher than the programmed DAC voltage at light loads, and slightly less than the DAC voltage at full-load current. For further information on voltage-positioning, see the *Applications* section.

Automatic Pulse-Skipping Switchover

In skip mode (SKP/$\overline{SDN}$ high), an inherent automatic switchover to PFM takes place at light loads (Figure 4). This switchover is effected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (see the Continuous-to-Discontinuous Inductor Current Point graph in the *Typical Operating Characteristics*).

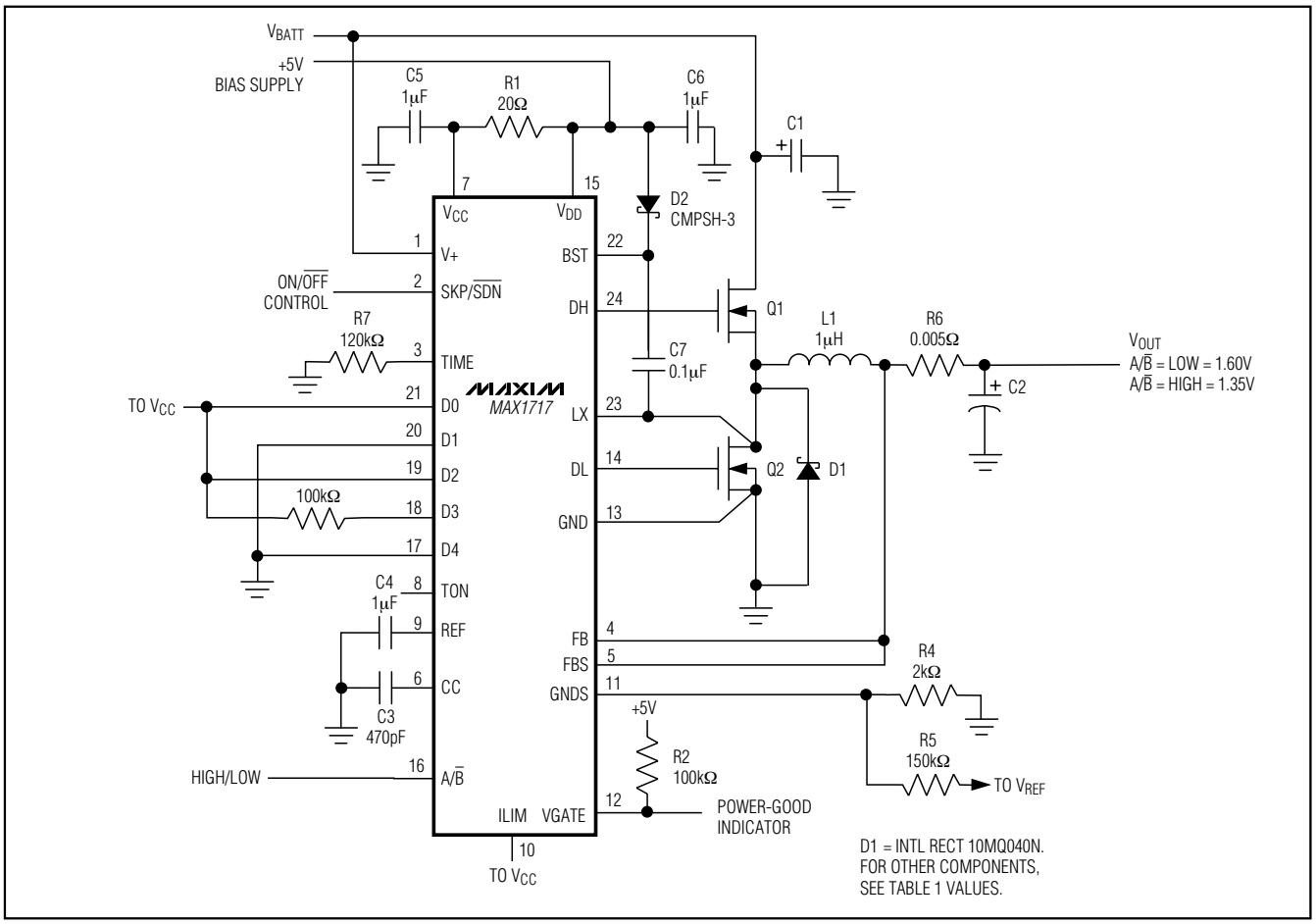


Figure 3. Voltage-Positioned Circuit

For a battery range of 7V to 24V, this threshold is relatively constant, with only a minor dependence on battery voltage:

$$I_{LOAD(SKIP)} \approx \frac{K \times V_{OUT}}{2 \times L} \times \frac{V_{BATT} - V_{OUT}}{V_{BATT}}$$

where K is the on-time scale factor (Table 3). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 4). For example, in the standard application circuit this becomes:

$$\frac{3.3\mu s \times 1.6V}{2 \times 1\mu H} \times \frac{12V - 1.6V}{12V} = 2.3A$$

The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

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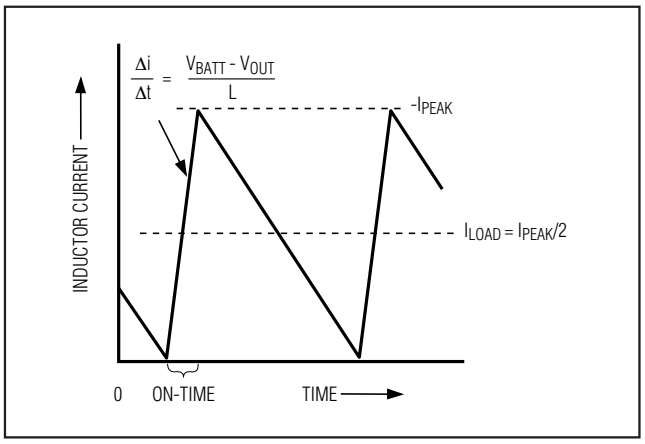

Figure 4. Pulse-Skipping/Discontinuous Crossover Point

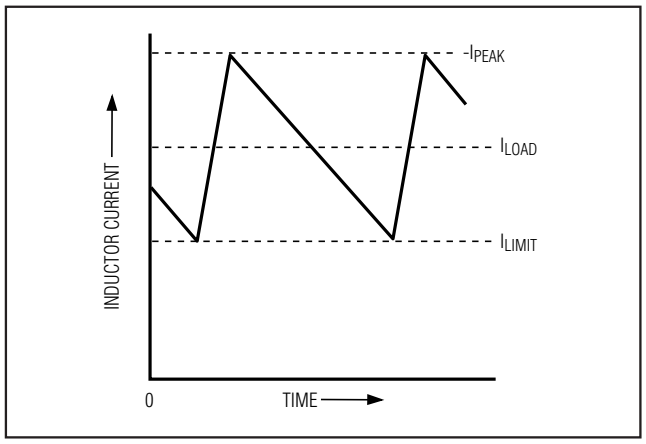

Figure 5. "Valley" Current-Limit Threshold Point

Forced-PWM Mode (SKP/$\overline{SDN}$ Open)

The low-noise forced-PWM mode (SKP/$\overline{SDN}$ open) disables the zero-crossing comparator that controls the low-side switch on-time. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop strives to maintain a duty ratio of V_{OUT}/V_{BATT}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: the no-load battery current can be 10mA to 40mA, depending on the external MOSFETs and switching frequency.

Forced-PWM mode is most useful for reducing audio-frequency noise and improving the cross-regulation of multiple-output applications that use a flyback transformer or coupled inductor.

Current-Limit Circuit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses the on-resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 5). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the MOSFET on-resistance, inductor value, and battery voltage. The reward for this uncertainty is robust, lossless overcurrent sensing. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit, and therefore tracks the positive current limit when ILIM is adjusted.

The current-limit threshold is adjusted with an external resistor-divider at ILIM. The current-limit threshold adjustment range is from 50mV to 300mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage seen at ILIM. The threshold defaults to 100mV when ILIM is connected to V_{CC}. The logic threshold for switchover to the 100mV default value is approximately V_{CC} - 1V.

The adjustable current limit accommodates MOSFETs with a wide range of on-resistance characteristics (see the *Design Procedure* section).

Carefully observe the PC board layout guidelines to ensure that noise and DC errors don't corrupt the current-sense signals seen by LX and GND. Place the IC close to the low-side MOSFET with short, direct traces, making a Kelvin sense connection to the source and drain terminals.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{BATT} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1717 will interpret the MOSFET gate as "off" while there is actually still charge left on the gate. Use very

short, wide traces measuring 10 to 20 squares (50 to 100 mils wide if the MOSFET is 1 inch from the MAX1717).

The dead time at the other edge (DH turning off) is determined by a fixed 35ns (typ) internal delay.

The internal pull-down transistor that drives DL low is robust, with a 0.5Ω typical on-resistance. This helps prevent DL from being pulled up during the fast rise-time of the inductor node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, you might still encounter some combinations of high- and low-side FETs that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BST, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 6).

POR

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and preparing the PWM for operation. V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching, forces VGATE low, and forces the DL gate driver high (to enforce output overvoltage protection). When V_{CC} rises above 4.2V, the DAC inputs are sampled and the output voltage begins to slew to the DAC setting.

For automatic startup, the battery voltage should be present before V_{CC}. If the MAX1717 attempts to bring the output into regulation without the battery voltage present, the fault latch will trip. The SKP/$\overline{SDN}$ pin can be toggled to reset the fault latch.

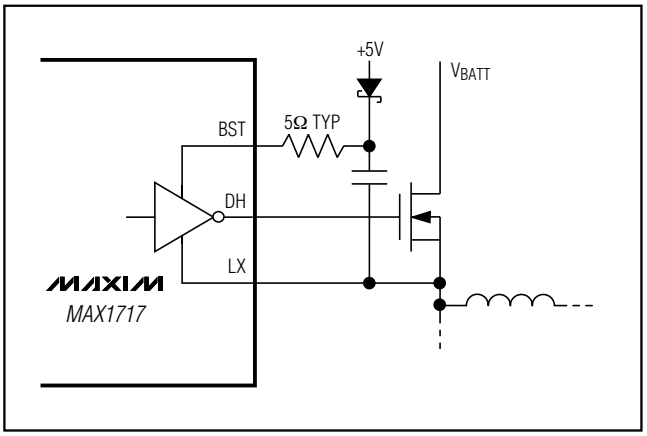

Figure 6. Reducing the Switching-Node Rise Time

Shutdown

When SKP/$\overline{SDN}$ goes low, the MAX1717 goes into low-power shutdown mode. VGATE goes low immediately. The output voltage ramps down to 0 in 25mV steps at the clock rate set by R_{TIME}. When the DAC reaches the 0V setting, DL goes high, DH goes low, the reference is turned off, and the supply current drops to about 2µA.

When SKP/$\overline{SDN}$ goes high or floats, the reference powers up, and after the reference UVLO is passed, the DAC target is evaluated and switching begins. The slew-rate controller ramps up from zero in 25mV steps to the currently selected code value (based on A/$\overline{B}$). There is no traditional soft-start (variable current limit) circuitry, so full output current is available immediately. VGATE goes high after the slew-rate controller has terminated and the output voltage is in regulation. As soon as VGATE goes high, full power is available.

UVLO

If the V_{CC} voltage drops low enough to trip the UVLO comparator, it is assumed that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, DL is forced high in this mode. This will force the output to GND, but it will not use the slew-rate controller. This results in large negative inductor current and possibly small negative output voltages. If V_{CC} is likely to drop in this fashion, the output can be clamped with a Schottky diode to GND to reduce the negative excursion.

DAC Inputs D0–D4

The digital-to-analog converter (DAC) programs the output voltage. It typically receives a preset digital code from the CPU pins, which are either hard-wired to GND or left open-circuit. They can also be driven by digital logic, general-purpose I/O, or an external mux. Do not leave D0–D4 floating—use 1MΩ or less pull-ups if the inputs may float. D0–D4 can be changed while the SMPS is active, initiating a transition to a new output voltage level. If this mode of DAC control is used, connect A/$\overline{B}$ high. Change D0–D4 together, avoiding greater than 1µs skew between bits. Otherwise, incorrect DAC readings may cause a partial transition to the wrong voltage level, followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages (Table 4) are compatible with Intel's mobile Pentium® III specification.

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A/$\overline{B}$ Internal Mux

The MAX1717 contains an internal mux that can be used to select one of two programmed DAC codes and output voltages. The internal mux is controlled with the A/$\overline{B}$ pin, which selects between the A mode and the B mode. In the A mode, the voltage levels on D0–D4 select the output voltage according to Table 4. Do not leave D0–D4 floating; there are no internal pull-up resistors.

The B mode is programmed by external resistors in series with D0–D4, using a unique scheme that allows two sets of data bits using only one set of pins (Figure 7). When A/$\overline{B}$ goes low (or during power-up with A/$\overline{B}$ low), D0–D4 are tested to see if there is a large resistance in series with the pin. If the voltage level on the pin is a logic low, an internal switch connects the pin to an internal 40kΩ pull-up for about 4µs to see if the pin voltage can be forced high (Figure 8). If the pin voltage cannot be pulled to a logic high, the pin is considered low impedance and its B-mode logic state is low. If the pin can be pulled to a logic high, the impedance is considered high and so is the B-mode logic state. Similarly, if the voltage level on the pin is a logic high, an internal switch connects the pin to an internal 8kΩ pull-down to see if the pin voltage can be forced low. If so, the pin is high-impedance and its B-mode logic state is high. Otherwise, its logic state is low.

A high pin impedance (and logic high) is 100kΩ or greater, and a low impedance (and logic low) is 1kΩ or less. The *Electrical Characteristics* guaranteed levels for these impedances are 95kΩ and 1.05kΩ to allow the use of standard 100kΩ and 1kΩ resistors with 5% tolerance.

If the output voltage codes are fixed at PC board design time, program both codes with a simple combination of pin-strap connections and series resistors (Figure 7). If the output voltage codes are chosen during PC board assembly, both codes can be independently programmed with resistors (Figure 9). This matrix of 10 resistor-footprints can be programmed to all possible A-mode and B-mode code combinations with only five resistors.

Often, one or more output-voltage codes are provided directly by the CPU's VID pins. If the CPU actively drives these pins, connect A/$\overline{B}$ high (A mode) and let the CPU determine the output voltages. If the B mode is needed for startup or other reasons, insert resistors in series with D0–D4 to program the B-mode voltage. Be sure that the VID pins are actively driven at all times.

If the CPU's VID pins float, the open-circuit pins can present a problem for the MAX1717's internal mux. The processor's VID pins can be used for the A-mode setting, together with suitable pull-up resistors. However, the B-mode VID code is set with resistors in series with D0–D4, and in order for the B-mode to work, any pins intended to be B-mode logic low must appear to be low impedance, at least for the 4µs sampling interval.

Table 4. Output Voltage vs. DAC Codes

D4	D3	D2	D1	D0	V_{OUT} (V)
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35
0	1	1	1	0	1.30
0	1	1	1	1	No CPU
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	No CPU

Note: *In the no-CPU state, DH and DL are held low and the slew-rate controller is set for 0.9V.*

This can be achieved in several ways, including the following two (Figure 10). By using low-impedance pull-up resistors with the CPU's VID pins, each pin provides the low impedance needed for the mux to correctly interpret the B-mode setting. Unfortunately, the low resistances cause several mA additional quiescent current for each of the CPU's grounded VID pins. This quiescent current can be avoided by taking advantage of the fact that D0–D4 need only appear low impedance briefly, not necessarily on a continuous DC basis. High-impedance pull-ups can also be used if they are bypassed with a large enough capacitance to make them appear low impedance for the 4µs sampling interval. As noted in Figure 10, 4.7nF capacitors allow the inputs to appear low impedance even though they are pulled up with 1MΩ resistors.

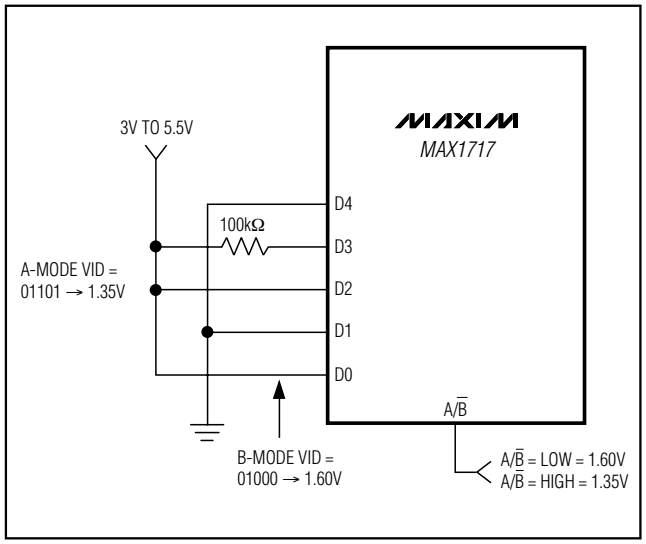

Figure 7. Using the Internal Mux with Hard-Wired A-Mode and B-Mode DAC Codes

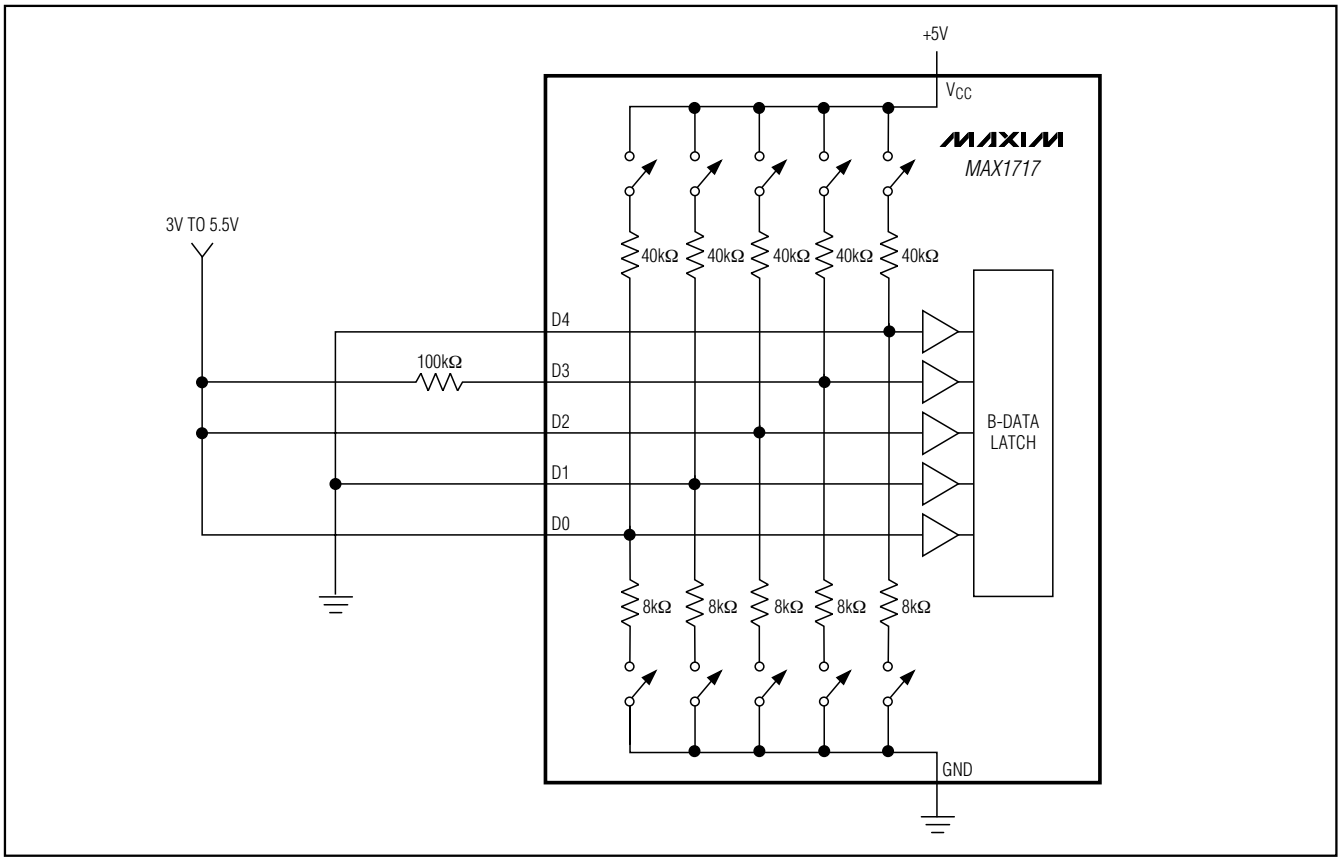

Figure 8. Internal Mux B-Mode Data Test and Latch

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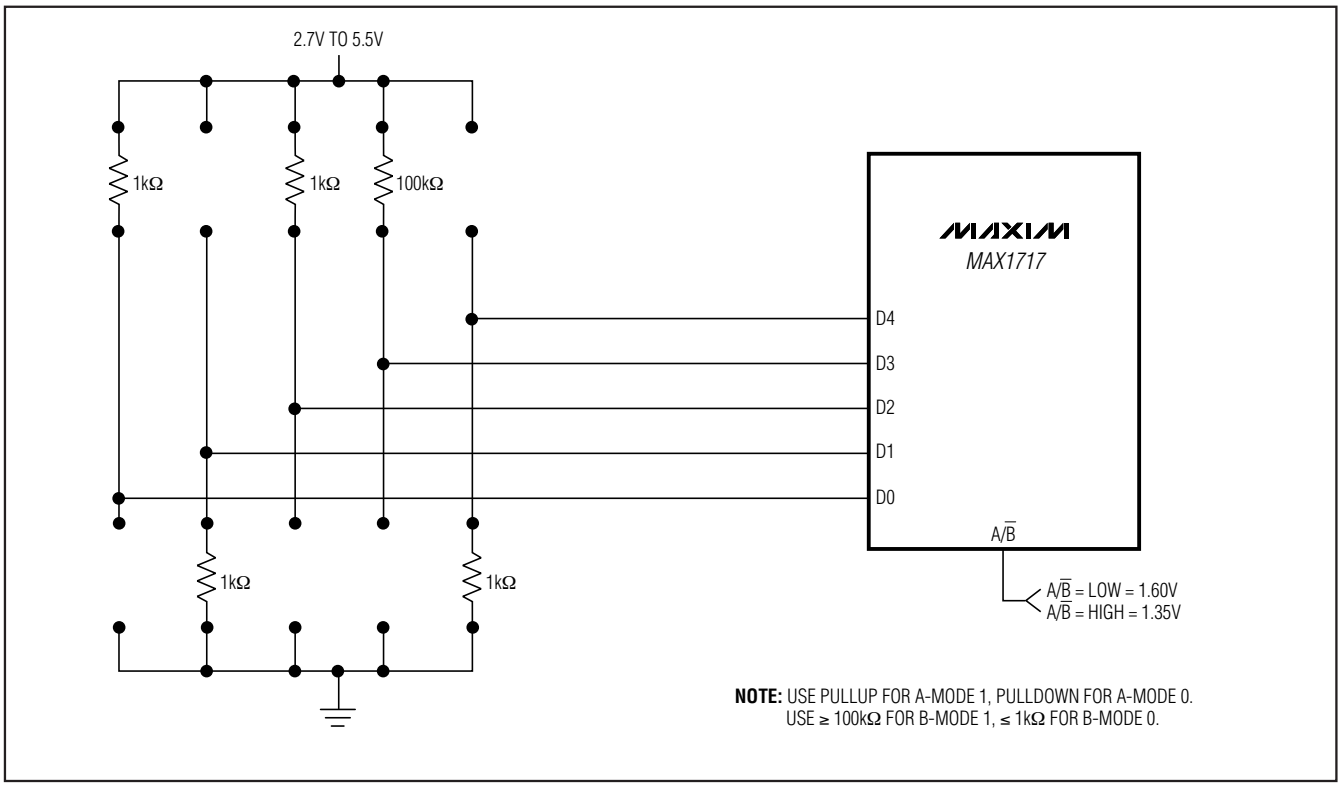

Figure 9. Using the Internal Mux with Both VID Codes Resistor Programmed

Output Voltage Transition Timing

The MAX1717 is designed to perform output voltage transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance. This makes the IC very suitable for CPUs featuring SpeedStep technology and other ICs that operate in two or more modes with different core voltage levels.

Intel's mobile Pentium III CPU with SpeedStep technology operates at two distinct clock frequencies and requires two distinct core voltages. When transitioning from one clock frequency to the other, the CPU first goes into a low-power state, then the output voltage and clock frequency are changed. The change must be accomplished in 100µs or the system may halt.

At the beginning of an output voltage transition, the MAX1717 brings the VGATE output low, indicating that a transition is beginning. VGATE remains low during the transition and goes high when the slew-rate controller has set the internal DAC to the final value and one additional slew-rate clock period has passed. The slew-rate clock frequency (set by resistor R_{TIME}) must be set fast enough to ensure that VGATE goes high within the allowed 100µs. Alternatively, the slew-rate clock can be set faster than necessary and VGATE's rising edge can be detected so that normal system operation can resume even earlier.

The output voltage transition is performed in 25mV steps, preceded by a 4µs delay and followed by one additional clock period after which VGATE goes high if the output voltage is in regulation. The total time for a transition depends on R_{TIME}, the voltage difference, and the accuracy of the MAX1717's slew-rate clock, and is not dependent on the total output capacitance. The greater the output capacitance, the higher the surge current required for the transition. The MAX1717 will automatically control the current to the minimum level required to complete the transition in the calculated time, as long as the surge current is less than the current limit set by ILIM.

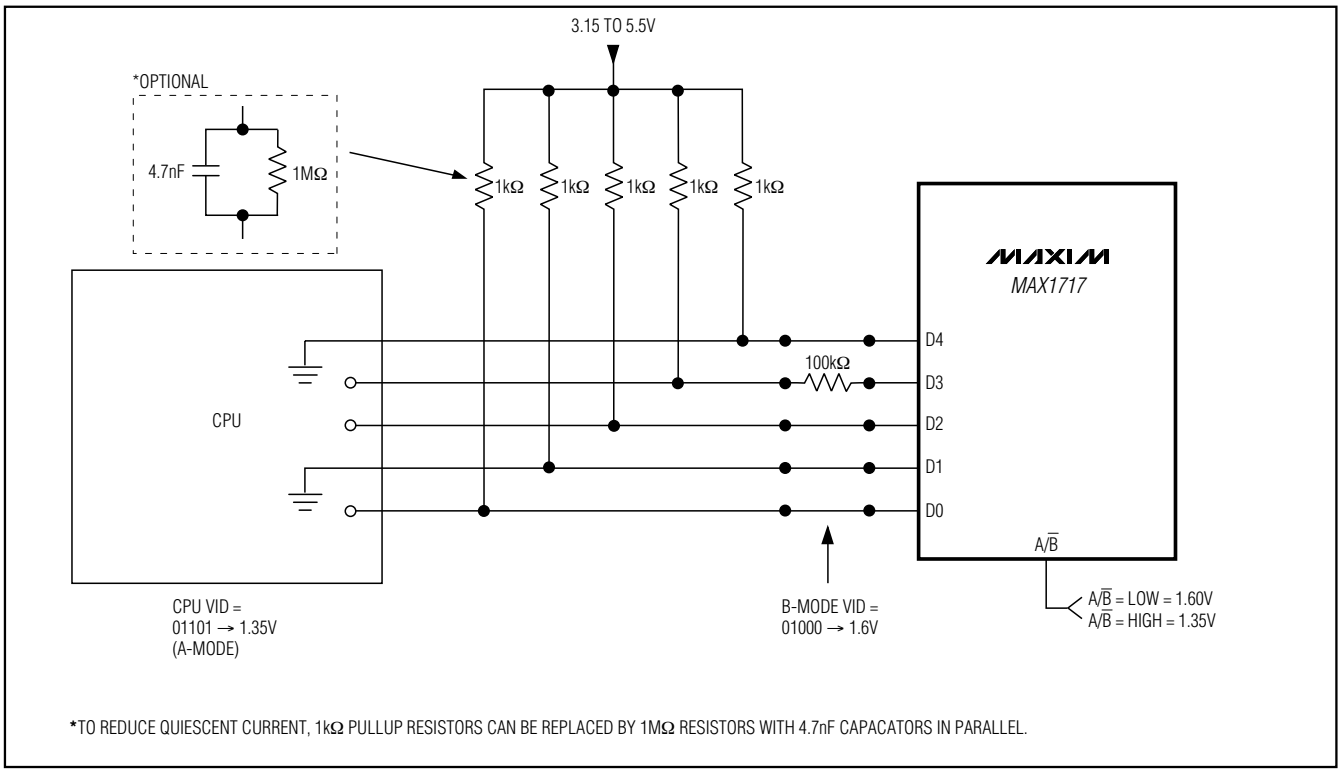

Figure 10. Using the Internal Mux with CPU Driving the A-Mode VID Code

The transition time is given by:

$$\leq 4\mu s + \left[\frac{1}{f_{SLEW}}\left(1 + \frac{V_{OLD} - V_{NEW}}{25mV}\right)\right]$$

where f_{SLEW} = 150kHz x 120kΩ / R_{TIME}, V_{OLD} is the original output voltage, and V_{NEW} is the new output voltage. See Time Frequency Accuracy in the *Electrical Characteristics* for f_{SLEW} accuracy.

The practical range of R_{TIME} is 47kΩ to 470kΩ, corresponding to 2.6µs to 26µs per 25mV step. Although the DAC takes discrete 25mV steps, the output filter makes the transitions relatively smooth. The average inductor current required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times 25mV \times f_{SLEW}$$

Output Overvoltage Protection

The overvoltage protection (OVP) circuit is designed to protect against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The output voltage is continuously monitored for overvoltage. If the output is more than 2.25V, OVP is triggered and the circuit shuts down. The DL low-side gate-driver output is then latched high until SKP/$\overline{SDN}$ is toggled or V_{CC} power is cycled below 1V. This action turns on the synchronous-rectifier MOSFET with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output to ground. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse will blow. DL is also kept high continuously when V_{CC} UVLO is active, as well as in shutdown mode (Table 5).

Overvoltage protection can be defeated through the NO FAULT test mode (see the *NO FAULT Test Mode* section).

Output Undervoltage Shutdown

The output UVP function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX1717 output voltage is under 70% of the nominal value, the PWM is latched off and won't restart until V_{CC} power is cycled or SKP/$\overline{SDN}$ is toggled. To allow startup, UVP is ignored during the undervoltage fault-blanking time (the first 256 cycles of the slew rate after startup).

UVP can be defeated through the NO FAULT test mode (see the *NO FAULT Test Mode* section).

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Table 5. Operating Mode Truth Table

SKP/$\overline{SDN}$	DL	MODE	COMMENT
GND	High	Shutdown	Low-power shutdown state. DL is forced to V_{DD}, enforcing OVP. I_{CC} + I_{DD} = 2µA (typ).
12V to 15V	Switching	No Fault	Test mode with faults disabled and fault latches cleared, including thermal shutdown. Otherwise, normal operation, with automatic PWM/PFM switchover for pulse-skipping at light loads.
Float	Switching	Run (PWM, low noise)	Low-noise operation with no automatic switchover. Fixed-frequency PWM action is forced regardless of load. Inductor current reverses at light load levels.
V_{CC}	Switching	Run (PFM/PWM, normal operation)	Normal operation with automatic PWM/PFM switchover for pulse-skipping at light loads.
V_{CC} or Float	High	Fault	Fault latch has been set by OVP, UVP, or thermal shutdown. Device will remain in FAULT mode until V_{CC} power is cycled or SKP/$\overline{SDN}$ is forced low.

NO FAULT Test Mode

The over/undervoltage protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a test mode is provided to disable totally the OVP, UVP, and thermal shutdown features, and clear the fault latch if it has been set. The PWM operates as if SKP/$\overline{SDN}$ were high (SKIP mode). The NO FAULT test mode is entered by forcing 12V to 15V on SKP/$\overline{SDN}$.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

1) **Input Voltage Range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

2) **Maximum Load Current.** There are two values to consider. The *peak load current* ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The *continuous load current* (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)}$ x 80%.

3) **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

4) **Inductor Operating Point.** This choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

   The MAX1717's pulse-skipping algorithm initiates skip mode at the critical conduction point. So, the inductor operating point also determines the load-current value at which PFM/PWM switchover occurs. The optimum point is usually found between 20% and 50% ripple current.

5) The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(I_{LOAD1} - I_{LOAD2})^2 \times L \left(K \frac{V_{OUT}}{V_{IN}} + t_{OFF(MIN)} \right)}{2 \times C_{OUT} \times V_{OUT} \left[K \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \right) - t_{OFF(MIN)} \right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see *Electrical Characteristics*) and K is from Table 3.

Inductor Selection

The switching frequency and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)}$ = 14A, V_{IN} = 7V, V_{OUT} = 1.6V, f_{SW} = 300kHz, 30% ripple current or LIR = 0.30.

$$L = \frac{1.6V(7V - 1.6V)}{7V \times 300kHz \times 0.30 \times 14A} = 0.98\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}).

$$I_{PEAK} = I_{LOAD(MAX)} + (LIR / 2)\ I_{LOAD(MAX)}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current; therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - (LIR / 2)\ I_{LOAD(MAX)}$$

where $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by the $R_{DS(ON)}$ of Q2. For the MAX1717, the minimum current-limit threshold (100mV default setting) is 90mV. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET Q2 data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise.

Examining the Figure 1 example with a Q_2 maximum $R_{DS(ON)}$ = 5.5mΩ at T_J = +25°C and 7.5mΩ at T_J = +100°C reveals the following:

$$I_{LIMIT(LOW)} = 90mV / 7.5m\Omega = 11.9A$$

and the required valley current limit is:

$$I_{LIMIT(LOW)} > 14A - (0.3012)\ 14A = 11.9A$$

Therefore, the circuit can deliver the full-rated 14A using the default ILIM threshold.

When delivering 14A of output current, the worst-case power dissipation of Q2 is 1.48W. With a thermal resistance of 60°C/W and each MOSFET dissipating 0.74W, the temperature rise of the MOSFETs is 60°C/W x 0.74W = 44.5°C, and the maximum ambient temperature is +100°C - 44.5°C = +55.5°C. To operate at a higher ambient temperature, choose lower $R_{DS(ON)}$ MOSFETs or reduce the thermal resistance. You could also raise the current-limit threshold, allowing operation with a higher MOSFET junction temperature.

Connect ILIM to V_{CC} for a default 100mV current-limit threshold. For an adjustable threshold, connect a resistor divider from REF to GND, with ILIM connected to the center tap. The external adjustment range of 0.5V to 3V corresponds to a current-limit threshold of 50mV to 300mV. When adjusting the current limit, use 1% tolerance resistors and a 10µA divider current to prevent a significant increase of errors in the current-limit tolerance.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le V_{STEP} / I_{LOAD(MAX)}$$

The actual microfarad capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology.

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Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, and other electrolytics).

When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} equation in the *Design Procedure* section). The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{L \times I_{PEAK}^2}{2 \times C \times V_{OUT}}$$

where I_{PEAK} is the peak inductor current.

Output Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The voltage-positioned circuits in this data sheet have their ESR zero frequencies lowered due to the external resistor in series with the output capacitor ESR, guaranteeing stability. For voltage-positioned circuits, the minimum ESR requirement of the output capacitor is reduced by the voltage-positioning resistor value.

For nonvoltage-positioned circuits, the following criteria must be satisfied. The boundary of instability is given by the following equation:

$$f_{ESR} \leq f_{SW} / \pi$$

where:

$$f_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 15kHz. In the standard application used for inductor selection, the ESR needed to support $50mV_{P-P}$ ripple is 50mV/4.2A = 11.9mΩ. Six 470µF/4V Kemet T510 low-ESR tantalum capacitors in parallel provide 5mΩ (max) ESR. Their typical combined ESR results in a zero at 17kHz, well within the bounds of stability.

Do not put high-value ceramic capacitors directly across the fast-feedback inputs (FB to GND) without taking precautions to ensure stability. Ceramic capacitors have a high ESR zero frequency and may cause erratic, unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the junction of the inductor and FB pin, or use a voltage-positioned circuit (see the *Voltage Positioning and Effective Efficiency* section).

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there isn't enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can cause the output voltage to rise above or fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Don't allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents defined by the following equation:

$$I_{RMS} = I_{LOAD} \frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}$$

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or a connector in series with the battery. If the MAX1717 is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>12A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

For maximum efficiency, choose a high-side MOSFET (Q1) that has conduction losses equal to the switching losses at the optimum battery voltage (15V). Check to ensure that the conduction losses at minimum input voltage don't exceed the package thermal limits or violate the overall thermal budget. Check to ensure that conduction losses plus switching losses at the maximum input voltage don't exceed the package ratings or violate the overall thermal budget.

Choose a low-side MOSFET (Q2) that has the lowest possible $R_{DS(ON)}$, comes in a moderate-sized package (i.e., one or two SO-8s, DPAK or D^2PAK), and is reasonably priced. Ensure that the MAX1717 DL gate driver can drive Q2; in other words, check that the dv/dt caused by Q1 turning on does not pull up the Q2 gate due to drain-to-gate capacitance, causing cross-conduction problems. Switching losses aren't an issue for the low-side MOSFET since it's a zero-voltage switched device when used in the buck topology.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation due to resistance occurs at minimum battery voltage:

$$PD\,(Q1\ Resistive) = \frac{V_{OUT}}{V_{IN}} \times I_{LOAD}^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses don't usually become an issue until the input is greater than approximately 15V.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2f_{SW} switching-loss equation. If the high-side MOSFET you've chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, reconsider your choice of MOSFET.

Calculating the power dissipation in Q1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on Q1:

$$PD\,(Q1\,Switching) = \frac{C_{RSS} \times V_{IN(MAX)}^2 \times f_{SW} \times I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q1 and I_{GATE} is the peak gate-drive source/sink current (1A typ).

For the low-side MOSFET (Q2), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD\,(Q2) = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) I_{LOAD}^2 \times R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT(HIGH)} + (LIR / 2) \times I_{LOAD(MAX)}$$

where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. This means that the MOSFETs must be very well heatsinked. If short-circuit protection without overload protection is enough, a normal I_{LOAD} value can be used for calculating component stresses.

Choose a Schottky diode (D1) having a forward voltage low enough to prevent the Q2 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional and can be removed if efficiency isn't critical.

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Application Issues

Voltage Positioning and Effective Efficiency

Powering new mobile processors requires new techniques to reduce cost, size, and power dissipation. Voltage positioning reduces the total number of output capacitors to meet a given transient response requirement. Setting the no-load output voltage slightly higher allows a larger step down when the output current suddenly increases, and regulating at the lower output voltage under load allows a larger step up when the output current suddenly decreases. Allowing a larger step size means that the output capacitance can be reduced and the capacitor's ESR can be increased.

The no-load output voltage is raised by adding a fixed offset to GNDS through a resistor divider from REF. A 27mV nominal value is appropriate for 1.6V applications. This 27mV corresponds to a 0.9 x 27mV = 24mV = 1.5% increase with a V_{OUT} of 1.6V. In the voltage-positioned circuit (Figure 3), this is realized with resistors R4 and R5. Use a 10µA resistor divider current.

Adding a series output resistor positions the full-load output voltage below the actual DAC programmed voltage. Connect FB and FBS directly to the inductor side of the voltage-positioning resistor (R6, 5mΩ). The other side of the voltage-positioning resistor should be tied directly to the output filter capacitor with a short, wide PC board trace. With a 14A full-load current, R6 causes a 70mV drop. This 70mV is a -4.4% error, but it is compensated by the +1.5% error from the GNDS offset, resulting in a net error of -2.9%. This is well within the typical specification for voltage accuracy.

An additional benefit of voltage positioning is reduced power consumption at high load currents. Because the output voltage is lower under load, the CPU draws less current. The result is lower power dissipation in the CPU, though some extra power is dissipated in R6. For a nominal 1.6V, 12A output, reducing the output voltage 2.9% gives an output voltage of 1.55V and an output current of 11.65A. Given these values, CPU power consumption is reduced from 19.2W to 18.1W. The additional power consumption of R6 is:

$$5m\Omega \times 11.65A^2 = 0.68W$$

and the overall power savings is as follows:

$$19.2 - (18.1 + 0.68) = 0.42W$$

In effect, 1W of CPU dissipation is saved and the power supply dissipates much of the savings, but both the net savings and the transfer of dissipation away from the hot CPU are beneficial.

Effective efficiency is defined as the efficiency required of a nonvoltage-positioned circuit to equal the total dissipation of a voltage-positioned circuit for a given CPU operating condition.

Calculate effective efficiency as follows:

1) Start with the efficiency data for the positioned circuit (V_{IN}, I_{IN}, V_{OUT}, I_{OUT}).
2) Model the load resistance for each data point:

$$R_{LOAD} = V_{OUT} / I_{OUT}$$

3) Calculate the output current that would exist for each R_{LOAD} data point in a nonpositioned application:

$$I_{NP} = V_{NP} / R_{LOAD}$$

where V_{NP} = 1.6V (in this example).

4) Calculate effective efficiency as:

Effective efficiency = (V_{NP} x I_{NP}) / (V_{IN} x I_{IN}) = calculated nonpositioned power output divided by the measured voltage-positioned power input.

5) Plot the efficiency data point at the nonpositioned current, I_{NP}.

The effective efficiency of voltage-positioned circuits is shown in the *Typical Operating Characteristics*.

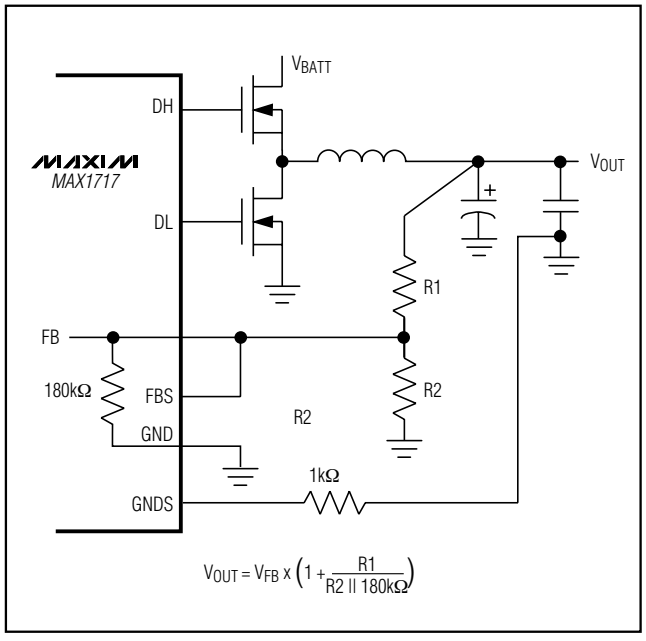

Figure 11. Adjusting V_{OUT} with a Resistor-Divider

Dropout Performance

The output voltage adjust range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot (375ns max at 1000kHz). For best dropout performance, use the slower (200kHz) on-time settings. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 3). Also, keep in mind that transient response performance of buck regulators operated close to dropout is poor, and bulk output capacitance must often be added (see the VSAG equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current will be less able to increase during each switching cycle and V_{SAG} will greatly increase unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but this may be adjusted up or down to allow tradeoffs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \frac{\left(V_{OUT} + V_{DROP1}\right)}{1-\left(\frac{T_{OFF(MIN)} \times h}{K}\right)} + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths (see On-Time One-Shot), $T_{OFF(MIN)}$ is from the *Electrical Characteristics*, and K is taken from Table 3. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then operating frequency must be reduced or output capacitance added to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout Design Example:

V_{OUT} = 1.6V

f_{SW} = 550kHz

K = 1.8µs, worst-case K = 1.58µs

$T_{OFF(MIN)}$ = 500ns

$V_{DROP1} = V_{DROP2}$ = 100mV

h = 1.5

$V_{IN(MIN)}$ = (1.6V + 0.1V) / (1-0.5µs x 1.5/1.58µs) + 0.1V - 0.1V = 3.2V

Calculating again with h = 1 gives the absolute limit of dropout:

$V_{IN(MIN)}$ = (1.6V + 0.1V) / (1-1.0 × 0.5µs/1.58µs) - 0.1V + 0.1V = 2.5V

Therefore, V_{IN} must be greater than 2.5V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 3.2V.

Adjusting V_{OUT} with a Resistor-Divider

The output voltage can be adjusted with a resistor-divider rather than the DAC if desired (Figure 11). The drawback is that the on-time doesn't automatically receive correct compensation for changing output voltage levels. This can result in variable switching frequency as the resistor ratio is changed, and/or excessive switching frequency. The equation for adjusting the output voltage is:

$$V_{OUT} = V_{FB}\left(1 + \frac{R_1}{R_2 \,||\, R_{INT}}\right)$$

where V_{FB} is the currently selected DAC value, and R_{INT} is the FB input resistance. When using external resistors, FBS remote sensing is not recommended, but GNDS remote sensing is still possible. Connect FBS to FB, and GNDS to a remote ground location. In resistor-adjusted circuits, the DAC code should be set as close as possible to the actual output voltage in order to minimize the shift in switching frequency.

Adjusting V_{OUT} Above 2V

The feed-forward circuit that makes the on-time dependent on battery voltage maintains a nearly constant switching frequency as V_{IN}, I_{LOAD}, and the DAC code are changed. This works extremely well as long as FB is connected directly to the output. When the output is adjusted with a resistor divider, the switching frequency is increased by the inverse of the divider ratio.

This change in frequency can be compensated with the addition of a resistor-divider to the battery-sense input (V+). Attach a resistor-divider from the battery voltage to V+ on the MAX1717, with the same attenuation factor as the output divider. The V+ input has a nominal input impedance of 600kΩ, which should be considered when selecting resistor values.

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One-Stage (Battery Input) vs. Two-Stage (5V Input) Applications

The MAX1717 can be used with a direct battery connection (one stage) or can obtain power from a regulated 5V supply (two stage). Each approach has advantages, and careful consideration should go into the selection of the final design.

The one-stage approach offers smaller total inductor size and fewer capacitors overall due to the reduced demands on the 5V supply. The transient response of the single stage is better due to the ability to ramp the inductor current faster. The total efficiency of a single stage is better than the two-stage approach.

The two-stage approach allows flexible placement due to smaller circuit size and reduced local power dissipation. The power supply can be placed closer to the CPU for better regulation and lower I^2R losses from PC board traces. Although the two-stage design has worse transient response than the single stage, this can be offset by the use of a voltage-positioned converter.

Ceramic Output Capacitor Applications

Ceramic capacitors have advantages and disadvantages. They have ultra-low ESR and are noncombustible, relatively small, and nonpolarized. They are also expensive and brittle, and their ultra-low ESR characteristic can result in excessively high ESR zero frequencies (affecting stability in nonvoltage-positioned circuits). In addition, their relatively low capacitance value can cause output overshoot when going abruptly from full-load to no-load conditions, unless the inductor value can be made small (high switching frequency), or there are some bulk tantalum or electrolytic capacitors in parallel to absorb the stored energy in the inductor. In some cases, there may be no room for electrolytics, creating a need for a DC-DC design that uses nothing but ceramics.

The MAX1717 can take full advantage of the small size and low ESR of ceramic output capacitors in a voltage-positioned circuit. The addition of the positioning resistor increases the ripple at FB, lowering the effective ESR zero frequency of the ceramic output capacitor.

Output overshoot (V_{SOAR}) determines the minimum output capacitance requirement (see *Output Capacitor Selection* section). Often the switching frequency is increased to 550kHz or 1000kHz, and the inductor value is reduced to minimize the energy transferred from inductor to capacitor during load-step recovery. The efficiency penalty for operating at 550kHz is about 2% to 3% and about 5% at 1000kHz when compared to the 300kHz voltage-positioned circuit, primarily due to the high-side MOSFET switching losses.

Table 1 and the *Typical Operating Characteristics* include two circuits using ceramic capacitors with 1000kHz switching frequencies. The efficiency of the +5V input circuit (circuit 4) is substantially higher than circuit 5, which accommodates the full battery voltage range. Circuit 4 is an excellent choice for two-stage conversion applications if the goal is to minimize size and power dissipation near the CPU.

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 12). If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
2) All analog grounding is done to a separate solid copper plane, which connects to the MAX1717 at the GND pin. This includes the V_{CC}, REF, and CC capacitors, the TIME resistor, as well as any other resistor-dividers.
3) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
4) LX and GND connections to Q2 for current limiting must be made using Kelvin sense connections to guarantee the current-limit accuracy. With SO-8 MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting GND and LX inside (underneath) the SO-8 package.
5) When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
6) Ensure the FB connection to the output is short and direct. In voltage-positioned circuits, the FB connection

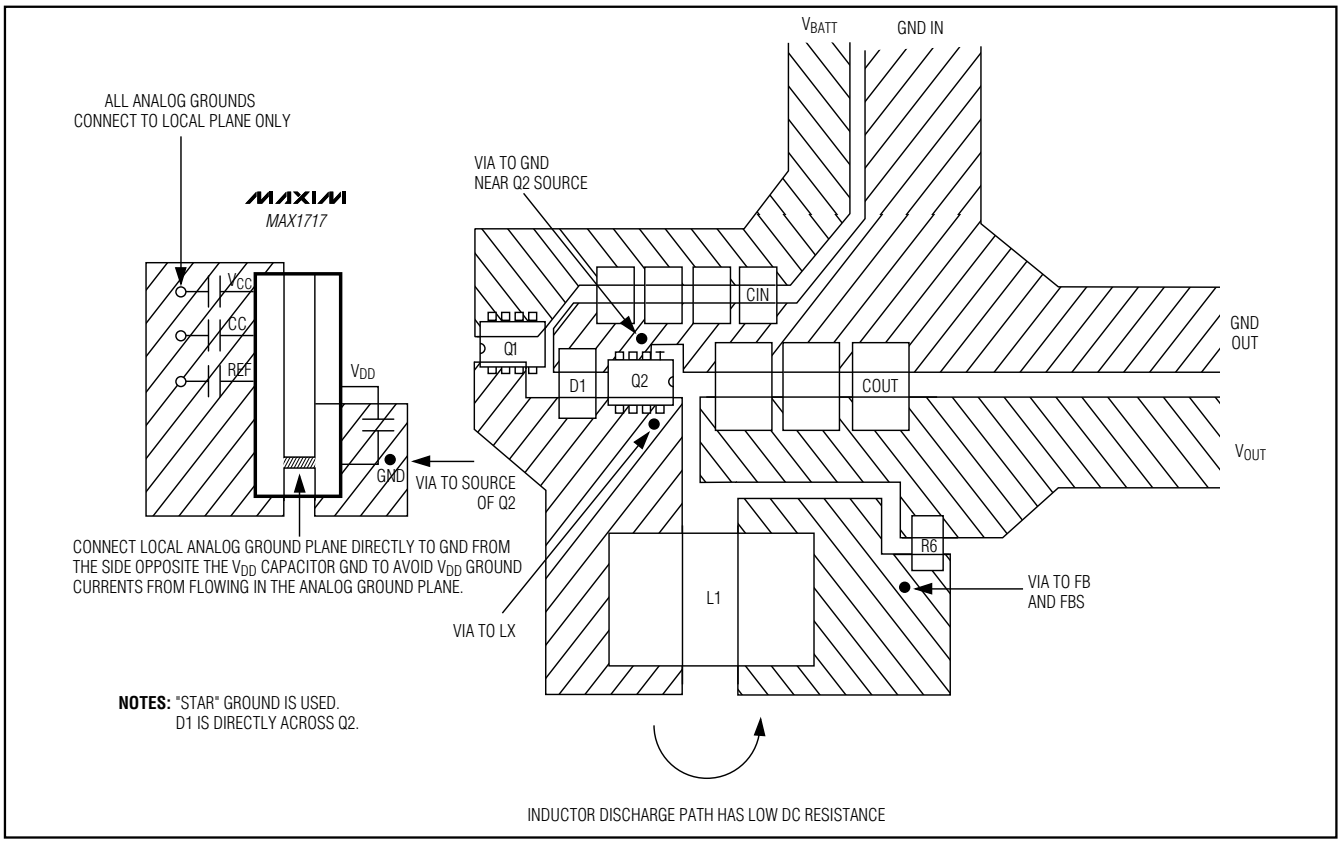

Figure 12. Power-Stage PC Board Layout Example

is at the junction of the inductor and the positioning resistor.

7) Route high-speed switching nodes away from sensitive analog areas (CC, REF, ILIM). Make all pin-strap control input connections (SKP/$\overline{SDN}$, ILIM, etc.) to analog ground or V_{CC} rather than power ground or V_{DD}.

Layout Procedure

1) Place the power components first, with ground terminals adjacent (Q2 source, CIN-, COUT-, D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to MOSFET Q2, preferably on the back side opposite Q2 in order to keep LX-GND current-sense lines and the DL drive line short and wide. The DL gate trace must be short and wide, measuring 10 to 20 squares (50mils to 100mils wide if the MOSFET is 1 inch from the controller IC).
3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 12. This diagram can be viewed as having three separate ground planes: output ground, where all the high-power components go; the GND plane, where the GND pin and V_{DD} bypass capacitors go; and an analog ground plane where sensitive analog components go. The analog ground plane and GND plane must meet only at a single point directly beneath the IC. These two planes are then connected to the high-power output ground with a short connection from GND to the source of the low-side MOSFET Q2 (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
5) Connect the output power planes (VCORE and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

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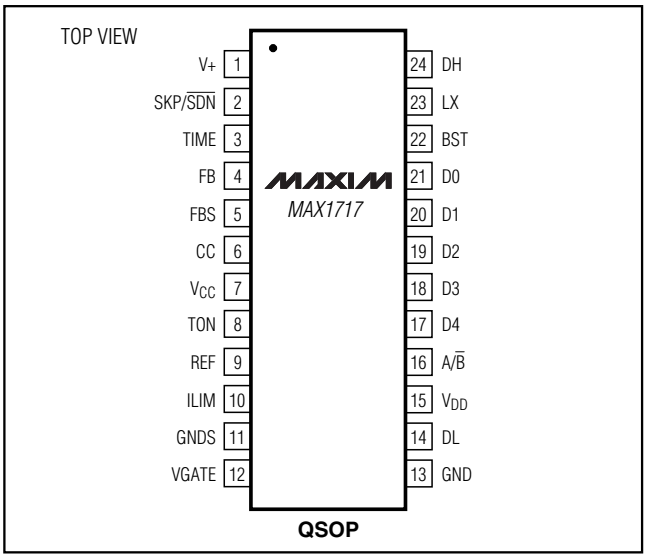
Pin Configuration

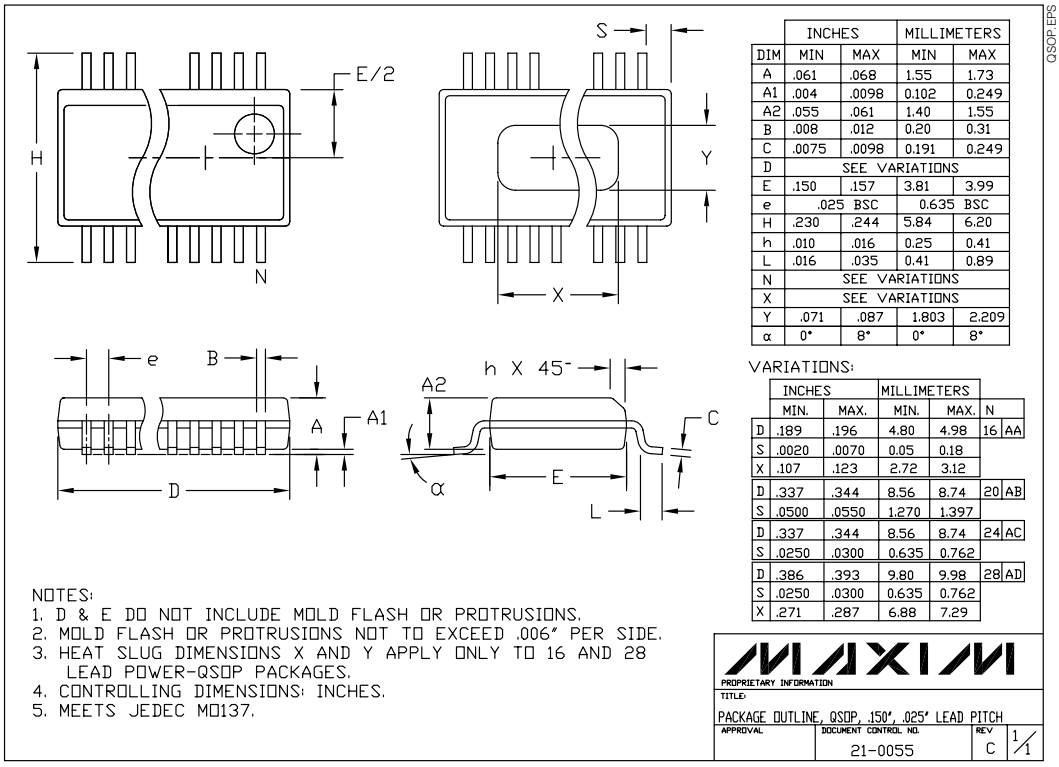


Chip Information

TRANSISTOR COUNT: 7151

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1