CDB4270

Evaluation Board for CS4270

Features

- Single-Ended Analog Audio Inputs and Outputs
- CS8416 S/PDIF Digital Audio Receiver
- Header for External Configuration of CS4270
- Header for External DSP Serial Audio I/O
- 3.3V Logic Interfaces
- Pre-Defined Software Scripts
- Demonstrates Recommended Layout
- Windows®-Compatible GUI Interface for Board Configuration and Control

Description

Using the CDB4270 is an excellent way to evaluate the CS4270 CODEC. Other equipment required includes analog/digital audio sources/analyzer, a 5V power supply and a Windows-compatible

PC for the GUI.

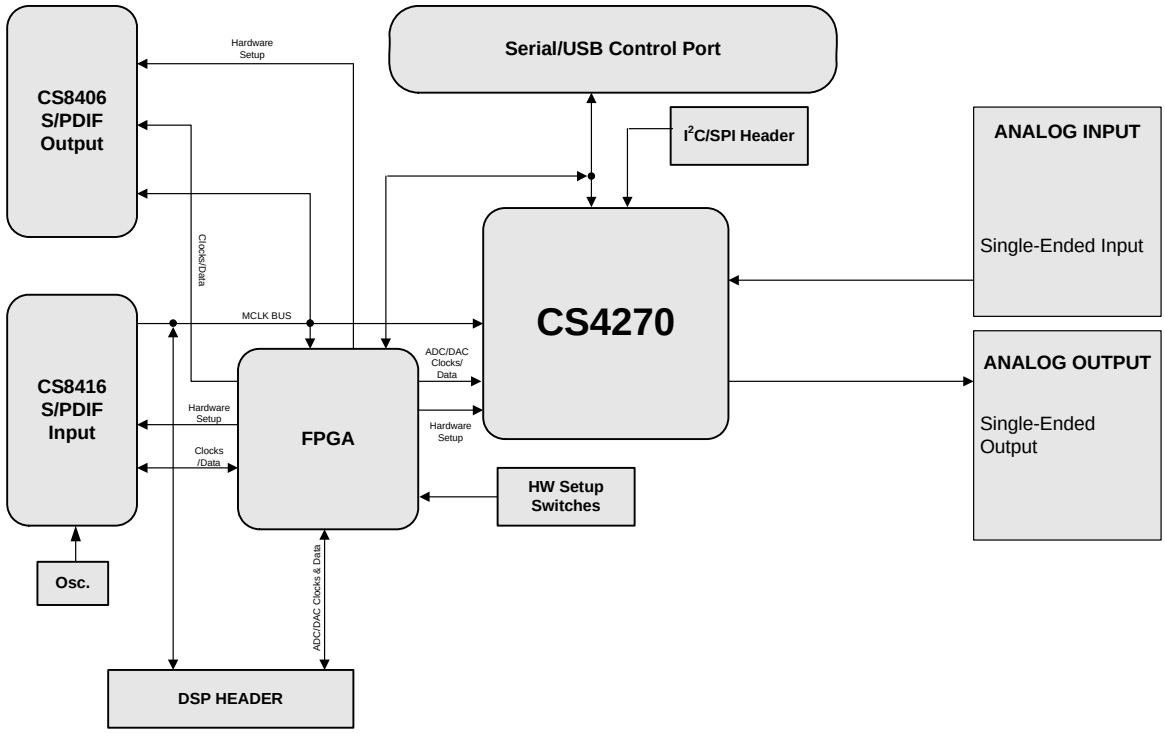
System timing for the I²S, Left-Justified or Right-Justified audio data formats can be provided by the CS4270, by the CS8416, or by a device connected to the on-board DSP I/O header. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

RCA jacks are provided for the analog audio inputs and outputs. Digital S/PDIF transmit or receive data I/O is available via either RCA jacks or optical connectors.

The Windows GUI software provided allows for easy configuration of the CDB4270. The GUI software communicates with the board via USB or serial port connections to configure the CS4270 registers.

ORDERING INFORMATION

CDB4270 Evaluation Board



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1. SYSTEM OVERVIEW

The CDB4270 evaluation board is an excellent tool for evaluating the CS4270 CODEC. The board features both analog and digital audio interfaces along with an FPGA for data/clk routing and an on-board microprocessor for configuration control. The board is easily configured in Software Mode using the supplied PC-to-DUT USB cable along with the Windows-based GUI configuration software or in Hardware Mode using the on-board dip switches.

The CDB4270 schematic set has been partitioned into nine pages and is shown in Figures 66 through 74.

1.1 Power

Power must be supplied to the evaluation board through the +5.0 V binding posts. The +5 V inputs must be referenced to the single black binding post ground connector (Figure 74 on page 45).

WARNING: Please refer to the CS4270 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

To optimize performance, PC board designs for the CS4270 require careful attention to power supply, grounding and signal routing arrangements. Figure 65 on page 36 shows the basic component/signal interconnect for the CDB4270. Figure 75 on page 46 shows the component placement. Figure 76 on page 47 shows the top layout. Figure 77 on page 48 shows the bottom layout. The decoupling capacitors are located as close to the CS4270 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

1.3 FPGA

See "FPGA Overview" on page 9 for a complete description of the FPGA (Figure 72 on page 43) that is used on the CDB4270.

1.4 CS4270 Audio CODEC

A complete description of the CS4270 (Figure 66 on page 37) is included in the CS4270 product data sheet.

The CS4270 codec performs stereo 24-bit A/D and D/A conversion at sample rates of up to 216 KHz. The part accommodates I²S, Left-Justified and Right-Justified serial audio formats.

1.5 CS8406 Digital Audio Transmitter

A complete description of the CS8406 transmitter (Figure 69 on page 40) and a discussion of the digital audio interface are included in the CS8406 data sheet.

The CS8406 converts the PCM data from either the CS4270, the DSP Header, or the CS8416 to a standard S/PDIF data stream. The CS8406 operates in either master or slave sub-clock mode and will accept either a 128 Fs, 256 Fs, or 512 Fs master clock on the OMCK input pin. The device will operate in either the Left-Justified or I²S interface data modes.

1.6 CS8416 Digital Audio Receiver

A complete description of the CS8416 receiver (Figure 70 on page 41) and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data that can be used by the CS4270 and CS8406. The device operates in either Master or Slave sub-clock modes and generates either a 128 Fs or 256 Fs master clock for output on the RMCK pin. Either Left-Justified or I²S interface output data formats can be selected

1.7 Canned Oscillator

Oscillator Y1 provides a system master clock. This clock is routed through the CS8416 and out of the RMCK pin when the S/PDIF input is disconnected (refer to the CS8416 data sheet for details on OMCK operation). To use the canned oscillator as the source of the MCLK signal, remove the S/PDIF input to the CS8416 and configure the CS8416 appropriately.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The board is shipped with a 12.288 MHz crystal oscillator populated at Y1.

1.8 External Control Headers

The evaluation board has been designed to allow interfacing with external systems via the J10 and J9 headers.

The 10-pin, 2-row header, J9, allows access to the serial audio signals required to interface with a DSP (see Figure 71 on page 42).

The 18-pin, 3-row header, J10, allows the user bidirectional access to the SPI™/I²C® control signals by simply removing all of the shunt jumpers from the “NORMAL” position. The user may then choose to connect a ribbon cable to the “EXTERNAL” position. A single “GND” row for the ribbon cable’s ground connection is provided to maintain signal integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB for the I²C power rail.

1.9 Analog Input

RCA connectors supply the CS4270 analog inputs through passive, AC-coupled, single-ended circuits. A 2 Vrms single-ended signal into the RCA connectors will drive the CS4270 inputs to full scale (1 Vrms). The input network on the CDB4270 was designed to demonstrate that the CS4270 will provide superior performance with up to 2.5 kΩ driving impedances (looking back from the CS4270 inputs) while allowing for 2 Vrms inputs. ADC performance varies depending upon the input impedance of the input network. Figures 1 and 2 show typical THD+N and Dynamic Range performance for the ADC as a function of input impedance.

THD+N Plot (1 kHz, Full-scale Input)

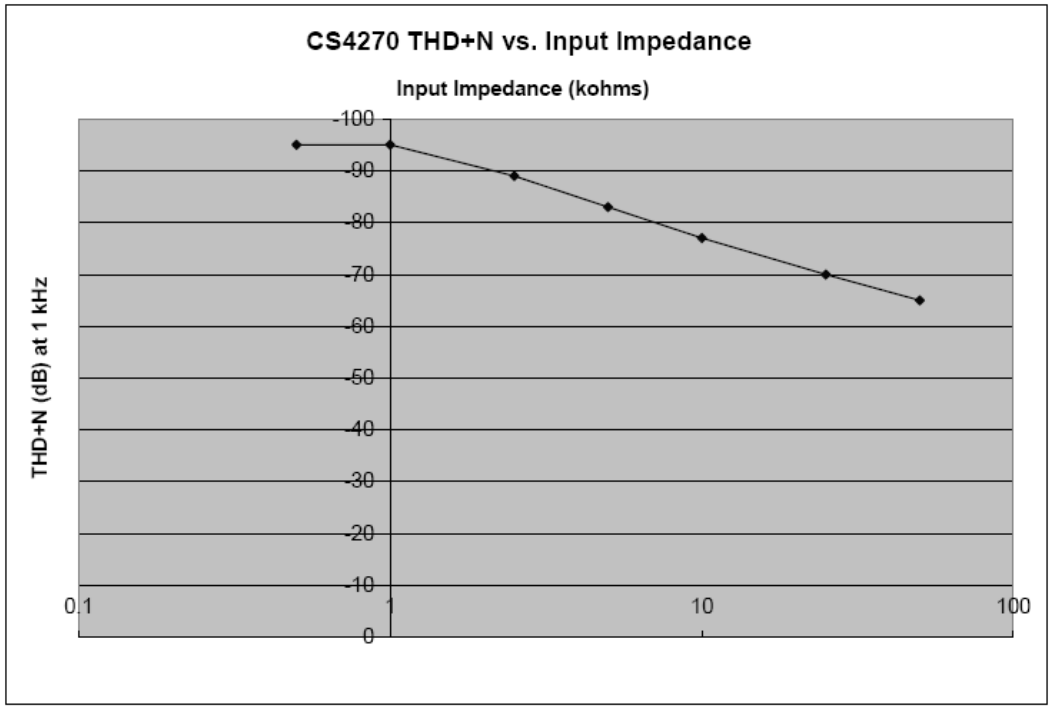

Figure 1. ADC THD+N

A-wtd Dynamic Range

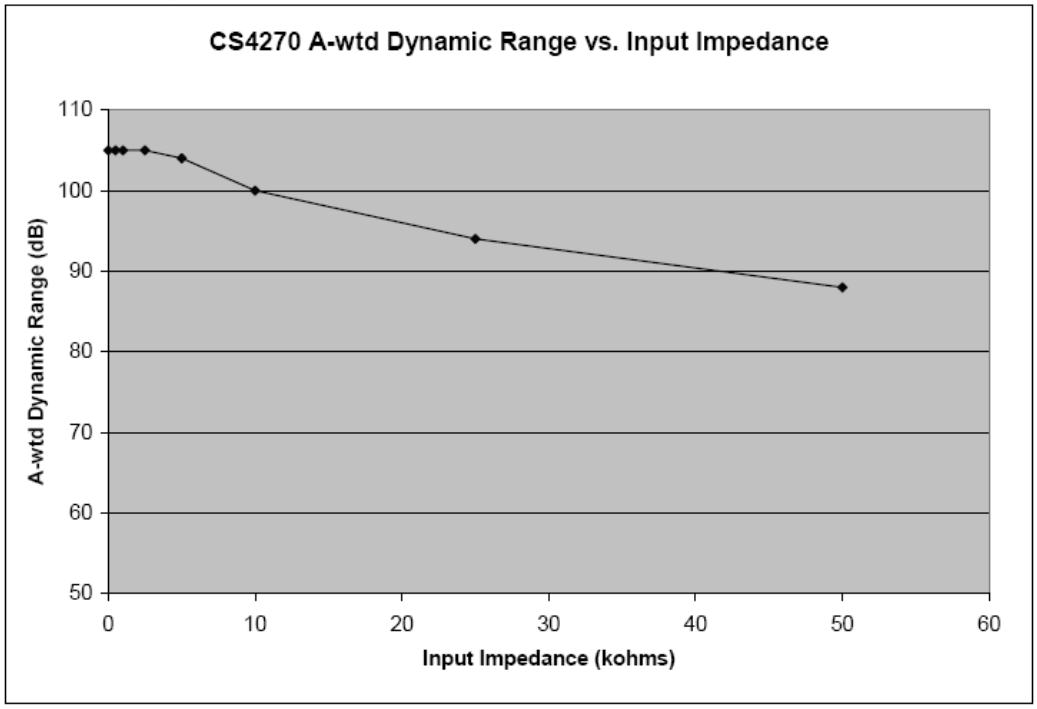

Figure 2. ADC Dynamic Range

1.10 Analog Outputs

The CS4270 analog outputs are AC-coupled and routed through a single-pole RC Low-Pass filter.

1.11 Control Port

A graphical user interface is included with the CDB4270 to allow easy manipulation of the registers in the CS4270 (see the CS4270 data sheet for register descriptions and the “FPGA GUI Register Description” on page 18). The GUI will run on a standard Windows-based PC. Connecting a USB cable from a PC to J15 or an RS-232 cable to J16 and launching the Cirrus Logic FlexGUI software enables control and configuration of the board.

Refer to “Software Mode” on page 13 for a description of the Graphical User Interface (GUI).

1.12 Hardware Mode Switches

The “HW Mode Config” and ”Clk/Data Config” switches control all Hardware Mode options. “Hardware Mode” on page 18 provides a description of each topology.

2. FPGA OVERVIEW

The FPGA (U11) controls all digital signal routing between the CS4270, CS8406, CS8416 and the DSP I/O Header. The device also generates all of the clock/data driver output enables and S/PDIF device mode controls. The FPGA internal registers can be configured either via the I²C (Software Mode) or via external dip switches (Hardware Mode). When using the CS4270 in Hardware Mode, the FPGA decodes some of these dip-switch settings and generates the CS4270 control signals. In addition, the FPGA distributes resets from the micro for all of the devices on the board.

2.1 FPGA Architecture

Figures 3 through 5 show the internal architecture of the FPGA. Figure 6 shows the MCLK routing to/from the FPGA and the other devices on the board. The FPGA has an I²C interface and internal registers for software control and can also read external dip-switch settings for hardware control. Refer to the FPGA GUI Register Description section of this document for a description of the FPGA registers.

2.2 Internal Sub-Clock Routing

Figure 3 shows the internal sub-clock (SCLK, LRCK) routing topology between the CS4270, CS8416, CS8406 and DSP Header. Refer to the FPGA GUI Register Description section of this document for a description of the sub-clock routing register settings.

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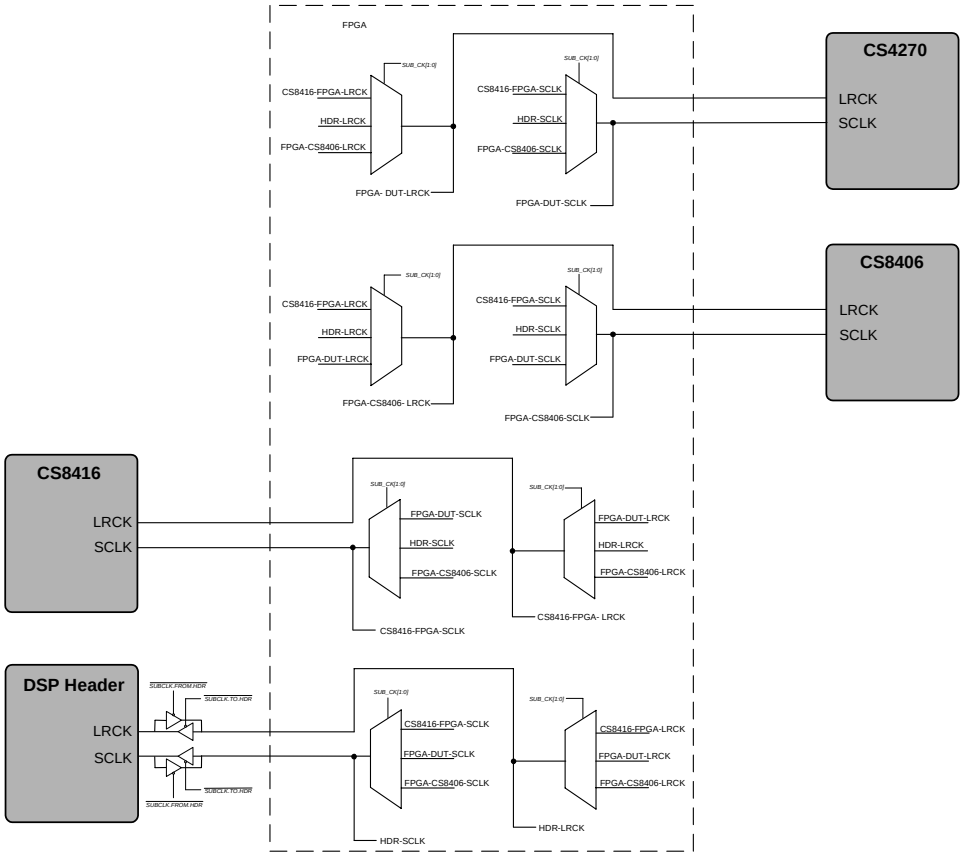

Figure 3. Internal Sub-Clock Routing

2.3 Internal Data Routing

Figure 4 shows the internal data routing topology between the CS4270, CS8416, CS8406 and the DSP Header. Refer to the FPGA GUI Register Description section of this document for a description of the audio data routing register settings.

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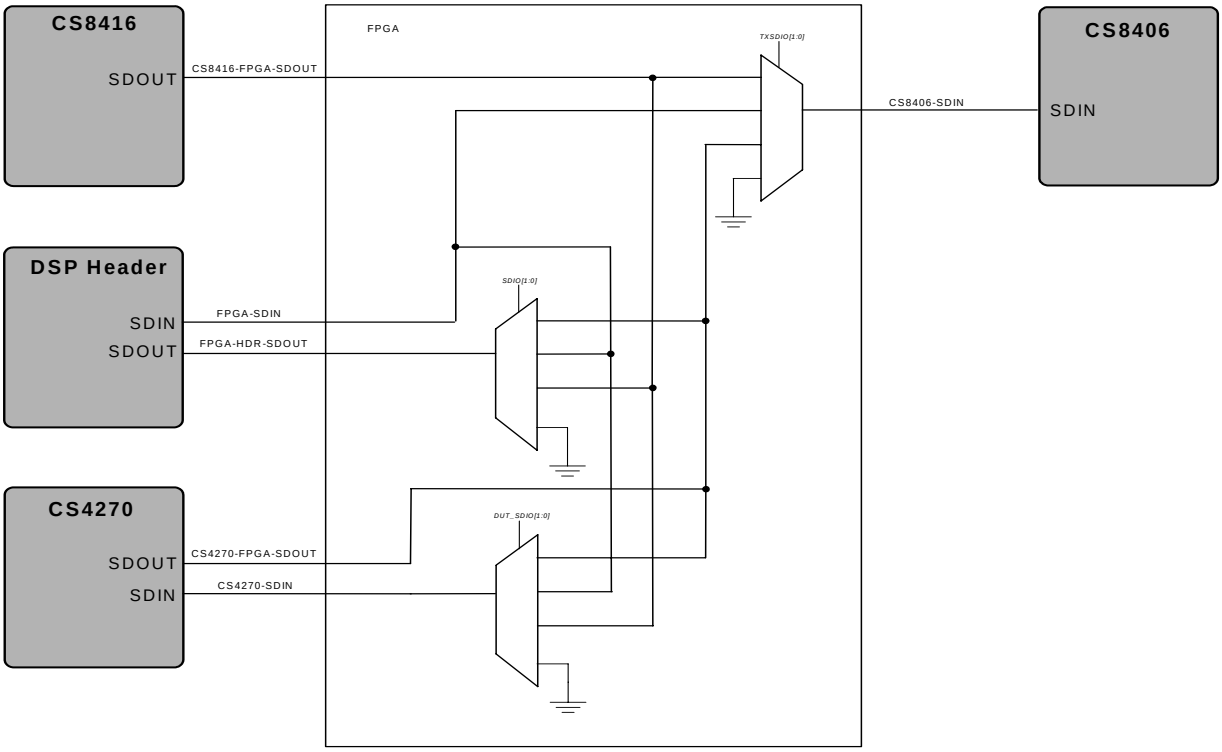

Figure 4. Internal Data Routing

2.4 Internal Drivers

Figure 5 shows the internal drivers and logic for board level selects/enables and so forth. Refer to the FPGA GUI Register Description section of this document for a description of the board level control register settings.

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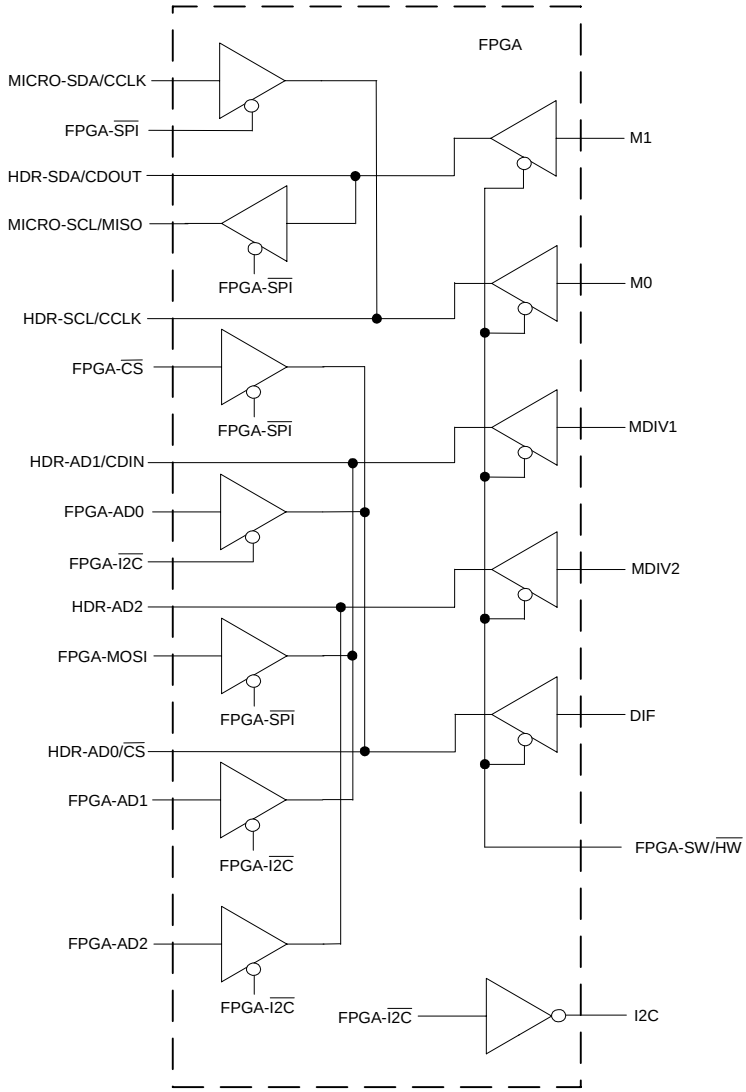

Figure 5. Internal Drivers

2.5 External MCLK Control

Several sources for MCLK exist on the CDB4270. The crystal oscillator, Y1, will master the MCLK bus when no S/PDIF signal is input to the CS8416 (refer to the CS8416 data sheet for details on OMCK operation).

When S/PDIF data is present at the CS8416 input, the CS8416 generates a master clock whenever its internal PLL is locked to the incoming S/PDIF stream.

The DSP Header can master the MCLK bus or be an observation point for MCLK depending upon the state of the driver control signals from the FPGA.

Refer to the Register Description section of this document for a description of the MCLK routing control registers.

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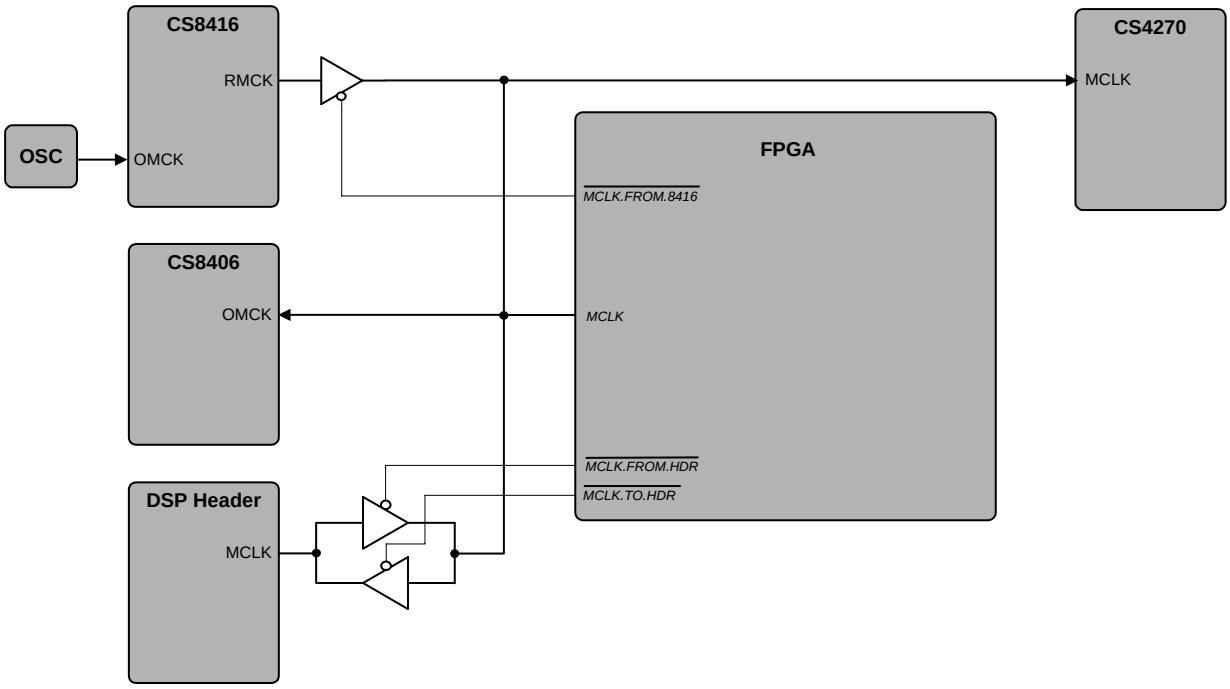


Figure 6. External MCLK Control

3. SOFTWARE MODE

The CDB4270 uses a Microsoft Windows-based GUI (download from Cirrus web site), which allows control of the CS4270 and FPGA registers. Interface to the GUI is provided via USB or RS-232 serial connection. Once the appropriate cable is connected between the CDB4270 and the host PC, run “FlexLoader.exe”. The software should automatically detect the board. If a board selection dialog is displayed, select “CDB4270” from the list. Once loaded, all registers are set to their default state. **Note:** The board is automatically set to Software Control Mode once the serial or USB cable is installed and the GUI is up and running. The GUI’s “File” menu provides the ability to save and load script files containing all of the register settings. Sample script files for basic mode operation can be downloaded from the archive at www.cirrus.com.

3.1 CDB4270 Control Scripts

Brief descriptions of the supplied scripts are given below.

3.1.1 S/PDIF In, Analog Out

When the SPDIF_IN_AOUT.FGS script is run, the CS8416 is the sub-clock (SCLK and LRCK) master and all other devices including the DSP Header are slaves. The CS8416 provides MCLK recovered from the S/PDIF data and SDOUT to the CS4270 DAC, DSP Header and CS8406.

3.1.2 Analog In, S/PDIF Out

When the AIN_SPDIF_OUT.FGS script is run, the crystal oscillator is the MCLK master. The CS8416 passes the clock from the crystal oscillator, Y1, through to the RMCK output (**Note:** the S/PDIF input must be disconnected) to the CS4270, the CS8406 and the DSP Header. The CS4270 provides SDOUT to the CS8406 and the DSP Header. The CS8406 generates sub-clocks derived from the CS4270 data and is the sub-clock master. All other devices including the DSP Header are sub-clock slave devices.

3.1.3 Analog In, Analog Out (Digital Loop-Back)

When the AIN_AOUT.FGS script is run, the crystal oscillator is the MCLK master. The CS8416 passes the clock from the crystal oscillator, Y1, through to the RMCK output (**Note:** the S/PDIF input must be disconnected) to the CS4270, the CS8406 and the DSP Header. The CS8416 generates sub-clocks derived from the crystal oscillator and is the sub-clock master. All other devices and the DSP Header are sub-clock slave devices. SDOUT from the CS4270 ADC is routed through the FPGA to the CS4270 DAC, to the DSP Header and to the CS8406.

3.1.4 DSP In, Analog Out

When the DSP_IN_AOUT.FGS script is run, the DSP Header is the MCLK, sub-clock and data master and all other devices are slaves. SDOUT at the header is the CS4270 SDOUT.

3.2 CDB4270 GUI

Brief descriptions of the GUI tab views are provided below.

The CDB4270 Controls tab provides high-level control of the CS4270, FPGA (Board Controls) and S/PDIF Tx and Rx devices. The “CS4270 Controls” group affects that device’s register settings. The “Board Controls” group allows the user to select MCLK and sub-clock source/routing as well as CS4270 and CS8406 SDIN sources. The “S/PDIF Receiver” and “S/PDIF Transmitter” control groups allow the user to select data formats, MCLK frequency and master or slave for each device. Reset push-buttons are also available along with a “Comm Mode” select drop box for CS4270 communication mode format selection.

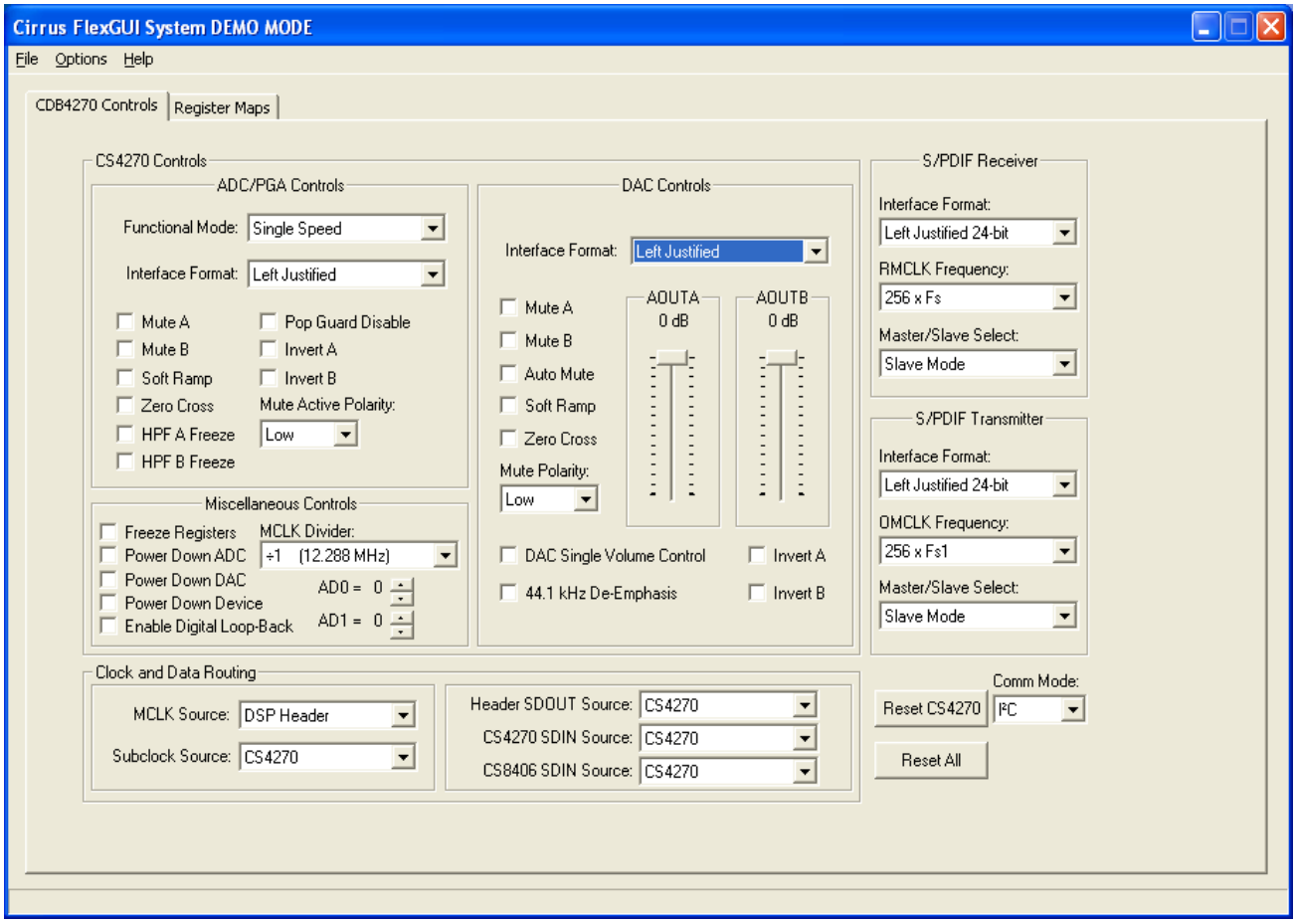


Figure 7. CDB4270 Controls Tab

3.3 Register Maps Control Tabs

Under this tab are the CS4270, Board Configuration (FPGA) and GPIO tabs. On each tab, register values can be modified bit-wise or byte-wise. For bit-wise modification, click the appropriate push-button for the desired bit. For byte-wise modification, the desired hex value can be typed directly into the register address box in the register map. Refer to the CS4270 device data sheet register settings section and the FPGA register information in this document for register definitions.

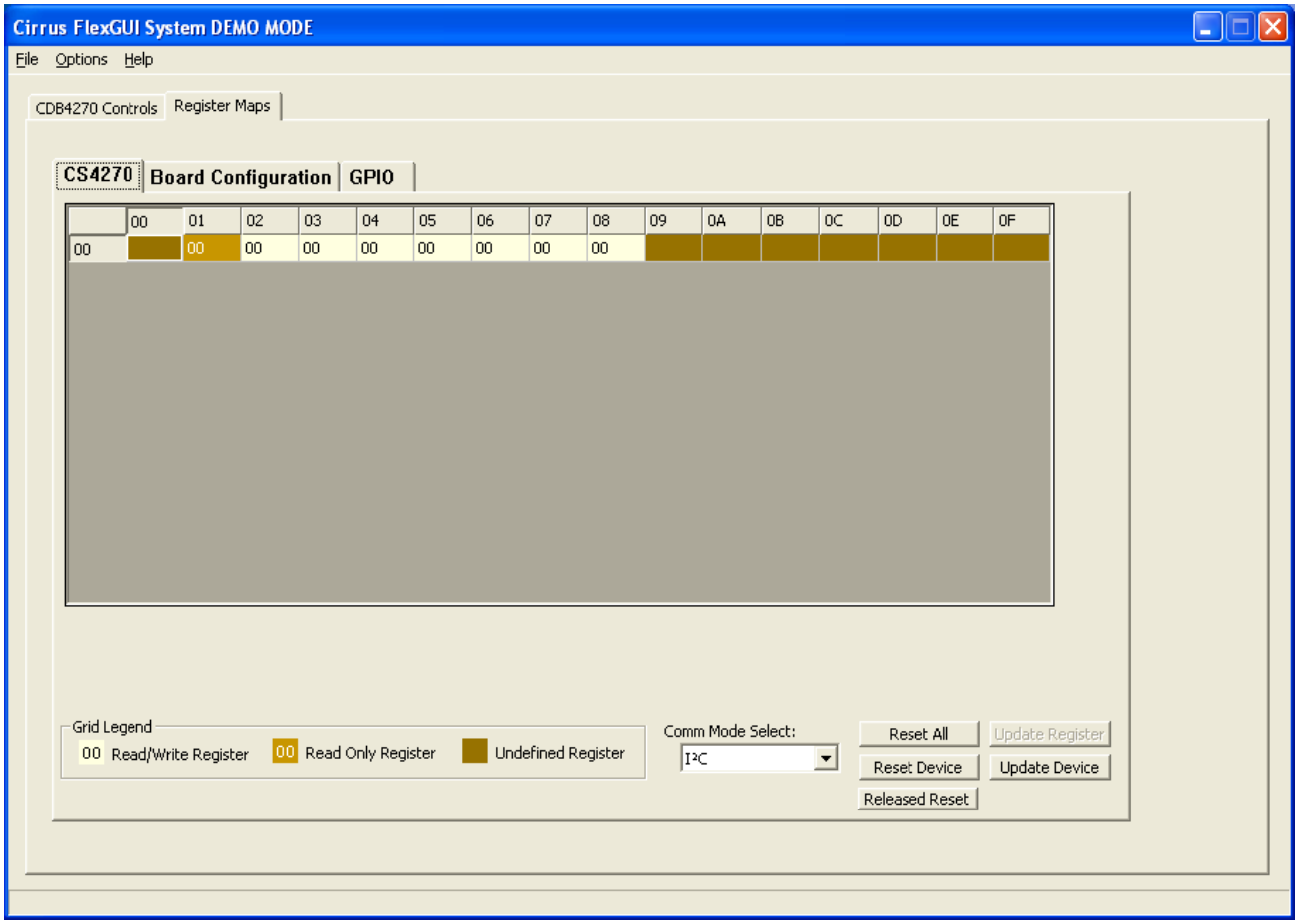


Figure 8. Register Maps Tab - CS4270

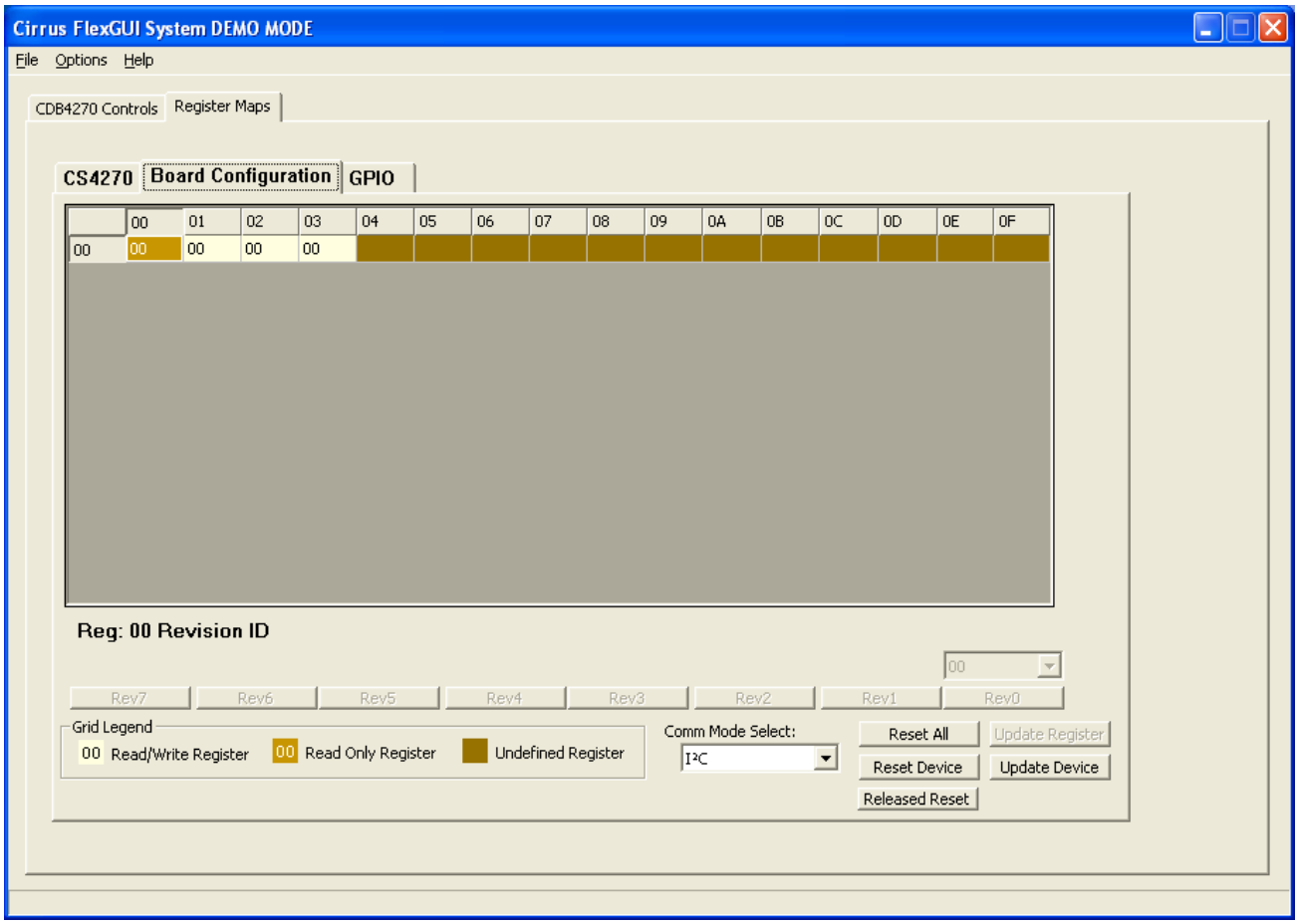


Figure 9. Register Maps Tab - Board Configuration

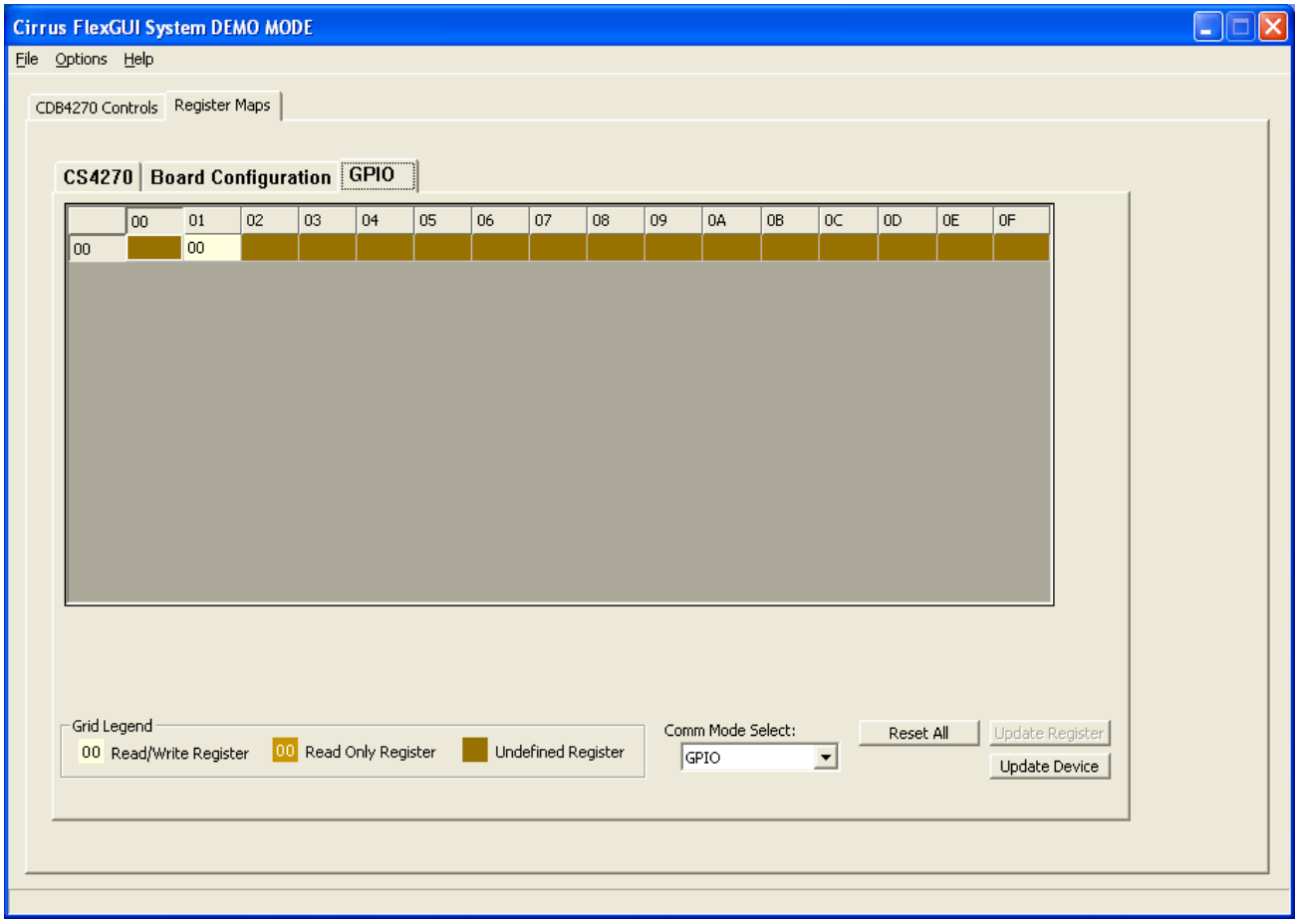


Figure 10. Register Maps Tab - GPIO

4. HARDWARE MODE

When the Flex GUI is not running on a PC or when the USB or serial port cables are not connected to the CDB4270 from the PC, the board is automatically in Hardware Control Mode. When in this control mode, dip switches S1 and S2 control the board's functionality. **Note:** Hardware Mode controls are a subset of Software Mode controls, and some FPGA or CS4270 register bits cannot be changed in Hardware Mode. See "CDB4270 Hardware Mode Settings" on page 24 of this document for a complete description of the Hardware Mode settings.

5. FPGA GUI REGISTER DESCRIPTION

As mentioned previously, the CS4270 and FPGA registers are directly accessible in Software Mode within the Flex GUI. In Hardware Mode, the FPGA registers control all board functions. The FPGA register descriptions for both modes are described below. For a description of the CS4270 registers, see the CS4270 data sheet.

5.1 FPGA REGISTER QUICK REFERENCE

The table below shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
00h	Code Rev. ID	REV.7	REV.6	REV.5	REV.4	REV.3	REV.2	REV.1	REV.0
		0	0	0	1	0	1	1	1
01h	SDIO/CLK/SW/HW Control	SDIO.1	SDIO.0	Reserved	MCLK	DUT_SDIO.1	DUT_SDIO.0	SUB_CK.1	SUB_CK.0
		0	0	0	1	0	0	0	0
02h	CS8406 Control	TXCLK.1	TXCLK.0	Reserved	TX_M/S	TX_FMT	Reserved	TXSDIO.1	TXSDIO.0
		0	0	0	0	0	0	0	1
03h	CS8416 Control	Reserved	RXCLK	Reserved	RX_M/S	RX_FMT	Reserved	Reserved	Reserved
		0	0	0	0	0	0	0	0

Note: Default "power on" bit states are shown.

5.2 FPGA CODE REVISION ID - ADDRESS 00H

7	6	5	4	3	2	1	0
REV.7	REV.6	REV.5	REV.4	REV.3	REV.2	REV.1	REV.0

5.2.1 Revision Number Bits (Bits 7:0)

Function:

Identifies FPGA code revision number. REV.7 - REV.4 indicate revision whole number, and REV.3 - REV.0 indicate revision decimal number. These register bits are Read-Only. See Table 1.

REV.7	REV.6	REV.5	REV.4	REV.3	REV.2	REV.1	REV.0	Revision Number
0	0	0	0	0	0	0	0	Not Used
0	0	0	1	0	0	0	1	Revision 1.1
0	0	0	1	0	0	1	0	Revision 1.2
0	0	0	1	0	0	1	1	Revision 1.3
0	0	0	1	0	1	0	0	Revision 1.4
0	0	0	1	0	1	0	1	Revision 1.5
0	0	0	1.	0	1	1	0	Revision 1.6
0	0	0	1	0	1	1	1	Revision 1.7
0	0	0	...	...	...	...	...	...
0	0	0	1	1	1	1	1	Revision 1.15
...	...	...	...	...	...	...	...	...
1	1	1	1	1	0	0	1	Revision 15.9
1	1	1	1	1	0	1	0	Revision 15.10
1	1	1	1	1	0	1	1	Revision 15.11
1	1	1	1	1	1	0	0	Revision 15.12
1	1	1	1	1	1	0	1	Revision 15.13
1	1	1	1	1	1	1	0	Revision 15.14
1	1	1	1	1	1	1	1	Revision 15.15

Table 1. Revision Number

5.3 CS4270 CONTROL - ADDRESS 01H

7	6	5	4	3	2	1	0
SDIO.1	SDIO.0	Reserved	MCLK	DUT_SDIO.1	DUT_SDIO.0	SUB_CK.1	SUB_CK.0

5.3.1 SDOUT Routing to Header (Bits 7:6)

Default = 00
Function:

These bits control the routing of SDOUT from the CS8416, CS4270 and the Header SDIN to the Header SDOUT. Table 2 shows the available settings.

SDIO.1	SDIO.0	SDIN/SDOUT Routing
0	0	CS4270 SDOUT source to DSP Header SDOUT
0	1	CS8416 SDOUT source to DSP Header SDOUT
1	0	SDIN from DSP Header to DSP Header SDOUT
1	1	Connect GND to DSP Header SDOUT

Table 2. SDOUT Routing to Header

5.3.2 MCLK Source (Bit 4)

Default = 1
Function:

This bit selects the source of the CS4270 MCLK signal. Table 3 shows the available settings.

MCLK	MCLK Source
0	MCLK from DSP Header
1	MCLK from Oscillator (through CS8416), MCLK to DSP Header

Table 3. MCLK Source

5.3.3 SDOUT Routing to DUT (Bits 3:2)

Default = 00
Function:

These bits control the routing of SDOUT from the CS8416, CS4270 and the Header SDIN to the CS4270. Table 4 shows the available settings.

DUT_SDIO.1	DUT_SDIO.0	SDIN/SDOUT Routing
0	0	CS4270 SDOUT source to CS4270 SDIN
0	1	CS8416 SDOUT source to CS4270 SDIN
1	0	SDIN from DSP Header to CS4270 SDIN
1	1	Connect GND to CS4270 SDIN

Table 4. SDOUT Routing to DUT

5.3.4 Subclock Routing (Bits 1:0)

Default = 00
Function:

These bits select SCLK and LRCK routing to/from the CS4270, CS8416, CS8406 and the Header. Table 5 shows the available settings.

SUB_CK.1	SUB_CK.0	Sub-Clock Routing
0	0	- CS4270 is Master - CS8416 and CS8406 are Slaves to CS4270 - DSP Header Sub-clocks are Outputs from CS4270
0	1	- CS4270 and CS8406 are Slaves to CS8416 - CS8416 is Master - DSP Header Sub-clocks are Outputs from CS8416
1	0	- CS4270 is Slave to DSP Header - CS8416 and CS8406 are Slaves to DSP Header - DSP Header sub clocks are Inputs
1	1	- CS4270 and CS8416 are Slave to CS8406 - CS8406 is Master - DSP Header Sub-clocks are Outputs from CS8406

Table 5. Sub-Clock Routing

5.4 CS8406 TX CONTROL - ADDRESS 02H

7	6	5	4	3	2	1	0
TXCLK.1	TXCLK.0	Reserved	TX_M/S	TX_FMT	Reserved	TXSDIO.1	TXSDIO.0

5.4.1 CS8406 OMCLK Divider Control (Bits 7:6)

Default = 00
Function:

These bits select the CS8406 OMCLK divider ratio. Table 6 shows the available settings.

TXCLK.1	TXCLK.0	CS8406 OMCLK Frequency
0	0	256 x Fs
0	1	128 x Fs
1	0	512 x Fs
1	1	256 x Fs

Table 6. CS8406 OMCLK Frequency

5.4.2 CS8406 Master/Slave Select (Bit 4)

Default = 0
Function:

This bit selects CS8406 Master Mode (SCLK, LRCK are outputs) or Slave Mode (SCLK, LRCK are inputs). See Table 7.

TX_M/S	CS8406 Master/Slave
0	CS8406 Slave Mode
1	CS8406 Master Mode

Table 7. CS8406 Master/Slave

5.4.3 CS8406 SDIN Format Select (Bit 3)

Default = 0
Function:

This bit selects the CS8406 SDIN format. See Table 8.

TX_FMT	CS8406 SDIN Format
0	24-bit Left-Justified
1	24-bit I²S

Table 8. CS8406 SDIN Format

5.4.4 CS8406 SDIN Source (Bits 1:0)

Default = 01
Function:

These bits select the source of the CS8406 SDIN Signal. Table 9 shows the available settings.

TXSDIO.1	TXSDIO.0	CS8406 SDIN Source
0	0	CS4270 SDOUT
0	1	CS8416 SDOUT
1	0	SDIN from Header
1	1	GND

Table 9. CS8406 SDIN Source

5.5 CS8416 RX CONTROL - ADDRESS 03H

7	6	5	4	3	2	1	0
Reserved	RXCLK	Reserved	RX_M/S	RX_FMT	Reserved	Reserved	Reserved

5.5.1 CS8416 RMCLK Divider Control (Bit 6)

Default = 0
Function:

This bit selects the CS8416 RMCLK divider ratio. Table 10.

RXCLK	CS8416 RMCLK Frequency
0	256 x Fs
1	128 x Fs

Table 10. CS8416 RMCLK Frequency

5.5.2 CS8416 Master/Slave Select (Bit 4)

Default = 0
Function:

This bit selects CS8416 Master Mode (SCLK, LRCK are outputs) or Slave Mode (SCLK, LRCK are inputs). See Table 11

RX_M/S	CS8416 Master/Slave
0	CS8416 Slave Mode
1	CS8416 Master Mode

Table 11. CS8416 Master/Slave

5.5.3 CS8416 SDOUT Format Select (Bit 3)

Default = 0
Function:

This bit selects the CS8416 SDOUT format. See.Table 12

RX_FMT	CS8416 SDOUT Format
0	24-bit Left-Justified
1	24-bit I²S

Table 12. CS8416 SDOUT Format

6. CDB4270 HARDWARE MODE SETTINGS

Schematic-Level Functional Description:

When the Flex GUI is not used and there is no serial port communication to the board, all devices are in HW Mode. FPGA SW control is disabled in this condition, and DIP switches S1 and S2 on the CDB4270 set the FPGA Registers to control board functionality. Note that the CS8406 and CS8416 are reset when SW/HW from the microprocessor goes low (going from SW to HW Mode). See the schematic for switch name labels, and see Table 13.

Dip Switch	Logic State b1, b0 nets	Functional Description
S1	0,0	As per Table 5. - CS4270 is Master - CS8416 and CS8406 are Slaves to CS4270 - DSP Header Sub-clocks are Outputs from CS4270
S1	0,1	As per Table 5. - CS8416 is Master - CS4270 and CS8406 are Slaves to CS8416 - DSP Header Sub-clocks are Outputs from CS8416
S1	1,0	As per Table 5. -DSP Header is Master - CS4270, CS8416 and CS8406 are Slaves to DSP Header - DSP Header Sub-clocks are Inputs
S1	1,1	As per Table 5. - CS8406 is Master - CS4270 and CS8416 are Slave to CS8406 - DSP Header Sub-clocks are Outputs from CS8406
Dip Switch	**Logic State b3, b2 nets**	**Functional Description**
S1	0,0	As per Table 2, Table 4, Table 9. CS4270 SDOUT to DSP Header SDOUT CS4270 SDOUT to CS4270 SDIN CS4270 SDOUT to CS8406 SDIN
S1	0,1	As per Table 2, Table 4, Table 9. CS8416 SDOUT to DSP Header SDOUT CS8416 SDOUT to CS4270 SDIN CS8416 SDOUT to CS8406 SDIN
S1	1,0	As per Table 2, Table 4, Table 9. DSP Header SDIN to DSP Header SDOUT DSP Header SDIN to CS4270 SDIN DSP Header SDIN to CS8406 SDIN
S1	1,1	As per Table 2, Table 4, Table 9. DSP Header SDIN to DSP Header SDOUT DSP Header SDIN to CS4270 SDIN DSP Header SDIN to CS8406 SDIN
Dip Switch	**Logic State b4 nets**	**FPGA Functional Description**
S1	0	As per Table 3. MCLK from DSP Header
S1	1	As per Table 3. MCLK from Oscillator (through CS8416), MCLK to DSP Header

Table 13. CDB4270 Hardware Mode - Functional Description

Dip Switch	(1) Logic State M1, M0, MDIV2, MDIV1	CS4270 Functional
S2	0,0,0,0	Sets CS4270 Single Speed MCLK divide by 1 Mode, no de-emphasis, CS8406 OMCLK=256xFs and CS8416 RMCLK=256xFs
S2	0,1,0,0	Sets CS4270 Single Speed MCLK divide by 1 Mode, w/de-emphasis, CS8406 OMCLK=256xFs and CS8416 RMCLK=256xFs
S2	1,0,0,0	Sets CS4270 Double Speed MCLK divide by 1 Mode, no de-emphasis, CS8406 OMCLK=128xFs and CS8416 RMCLK=128xFs
S2	1,0,1,0	Sets CS4270 Double Speed MCLK divide by 2 Mode, no de-emphasis, CS8406 OMCLK=256xFs and CS8416 RMCLK=256xFs
S2	1,1,10	Sets CS4270 Quad Speed MCLK divide by 2 Mode, no de-emphasis, CS8406 OMCLK=128xFs and CS8416 RMCLK=128xFs
S2	1,1,1,1	Sets CS4270 Quad Speed MCLK divide by 4 Mode, no de-emphasis, CS8406 OMCLK=256xFs and CS8416 RMCLK=256xFs
Dip Switch	**Logic State DIF net**	**CS4270 Functional Description**
S2	0	Sets CS4270 24-bit LJ Mode for SDIN and SDOUT. CS8406 set to LJ Mode for SDIN and CS8416 set to LJ Mode for serial data
S2	1	Sets CS4270 24-bit I²S Mode for SDIN and SDOUT. CS8406 set to I²S Mode for SDIN and CS8416 set to I²S Mode for serial data

Table 13. CDB4270 Hardware Mode - Functional Description

1. For other M1, M0, MDIV2, MDIV1 states, CS8406 OMCLK=256xFs and CS8416 RMCLK=256xFs.

Note: Whenever changes are made to the S/PDIF Receiver (CS8416), the FPGA (for CS4270 HW or SW Modes) generates a CS8416.RESET (CS8416 RESET) after the parameter is changed. Reg 03h (FPGA) shows the parameters that apply. Also, whenever CS4270-M/S (CS4270 master/slave) changes state, the FPGA generates a HDR-RESET (CS4270 RESET).

7. CDB CONNECTORS, SWITCHES, INDICATORS AND JUMPERS

CONNECTOR, SWITCH	Reference Designator	INPUT/OUTPUT	SIGNAL PRESENT
+5V	J1	Input	+5.0 V Power Supply
CLK/DATA CONTROL	S1	Input	HW Mode Clock/Data Routing Control Dip Switch
HW MODE CONFIG	S2	Input	HW Mode CS4270 Mode Control Switch
GND	J2	Input	Ground Reference
SPDIF OPTICAL OUT	OPT2	Output	CS8406 digital audio output via optical cable
SPDIF COAX OUT	J7	Output	CS8406 digital audio output via coaxial cable
SPDIF OPTICAL IN	OPT1	Input	CS8416 digital audio input via optical cable
SPDIF COAX IN	J5	Input	CS8416 digital audio input via coaxial cable
RS232	J16	Input/Output	Serial connection to PC for SPI / I²C Control Port signals
USB	J15	Input/Output	USB connection to PC for SPI / I²C Control Port signals
DSP HEADER	J9	Input/Output	I/O for Clocks & Data
SERIAL CONTROL	J10	Input/Output	I/O for external SPI / I²C Control Port signals
MICRO C2 HEADER	J14	Input/Output	I/O for programming the micro controller (U21)
FPGA JTAG	J12	Input/Output	I/O for programming the FPGA (U11)
MICRO RESET	S4	Input	Reset for the micro controller (U21)
AINA AINB	J13 J11	Input	RCA phono jacks for analog inputs
AOUTA AOUTB	J6 J4	Output	RCA phono jacks for analog outputs

Table 14. Connectors and Switches

JUMPER/ INDICATOR	PURPOSE	POSITION/ REF DES	FUNCTION SELECTED/INDICATION
CONTROL JUMPERS	SPI/I²C control Internal or external select	*J10, pins 1-2 J10, none	*Normal I²C/SPI Operation Connect to pins 2 (control) and 3 (gnd) for external control
MUTEA JUMPERS	Selects between $\overline{\text{MUTEA}}$ Enable and MUTEA LED Indicator Enable	*J8, pins 1-2 J8, pins 2-3	* $\overline{\text{MUTEA}}$ Enable MUTEA LED Enable
MUTEB JUMPERS	Selects between $\overline{\text{MUTEB}}$ Enable and MUTEB LED Indicator Enable	*J3, pins 1-2 J3, pins 2-3	* $\overline{\text{MUTEB}}$ Enable MUTEB LED Enable
MUTEA LED	Indicates that CS4270 $\overline{\text{MUTEA}}$ signal is present	D3	$\overline{\text{MUTEA}}$ from CS4270 is present when LED is on
MUTEB LED	Indicates that CS4270 $\overline{\text{MUTEB}}$ signal is present	D1	$\overline{\text{MUTEB}}$ from CS4270 is present when LED is on
$\overline{\text{INIT}}$ INDICATOR	Indicates FPGA program INIT	D5	FPGA is being programmed when on
DONE	Indicates FPGA program complete	D4	FPGA has been programmed when on
RCVR ERROR	Indicates CS8416 Data Receive Error	D2	Indicates Data Receive Error when on
USB PRESENT	Indicates USB Connection	D7	Indicates USB connection when on

*Default factory settings

Table 15. Jumpers and Indicators

8. ADC PERFORMANCE PLOTS

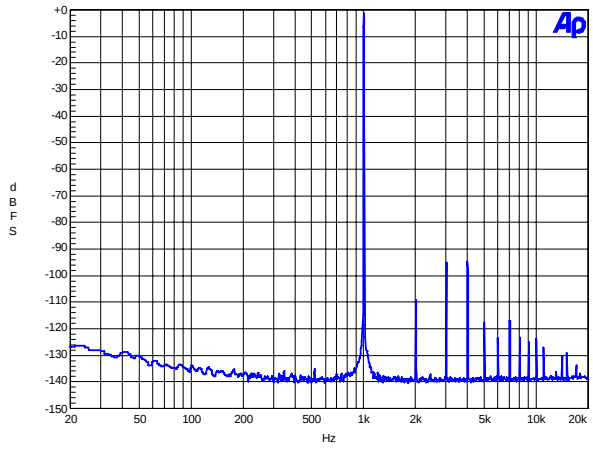


Figure 11. FFT (-1 dB 48 kHz)

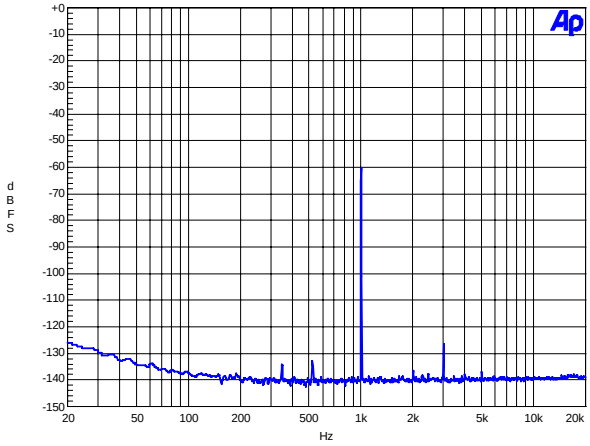


Figure 12. FFT (-60 dB, 48 kHz)

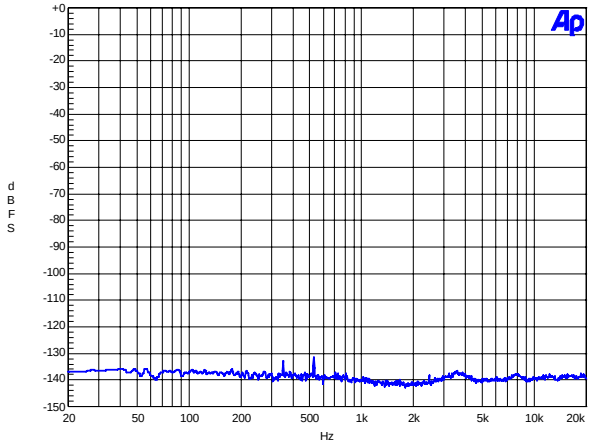


Figure 13. FFT (48 kHz, No Input)

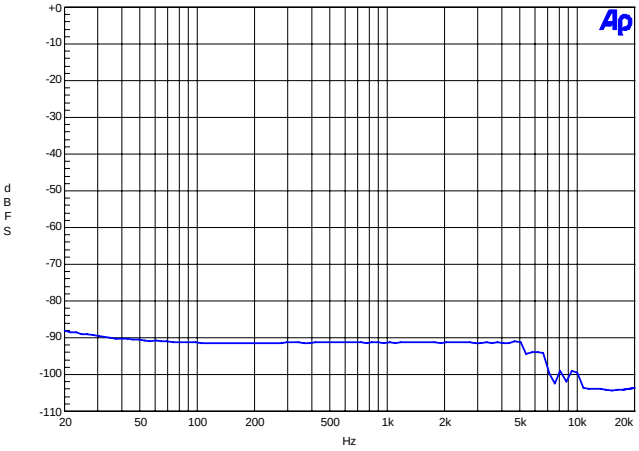


Figure 14. 48 kHz, THD+N vs. Input Freq

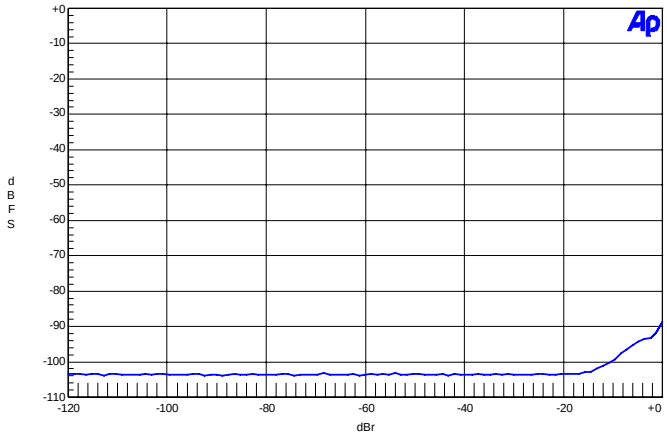


Figure 15. 48 kHz, THD+N vs. Level

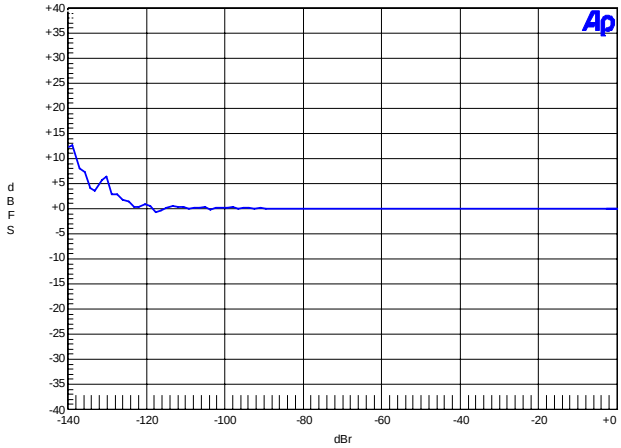


Figure 16. 48 kHz, Fade-to-Noise Linearity

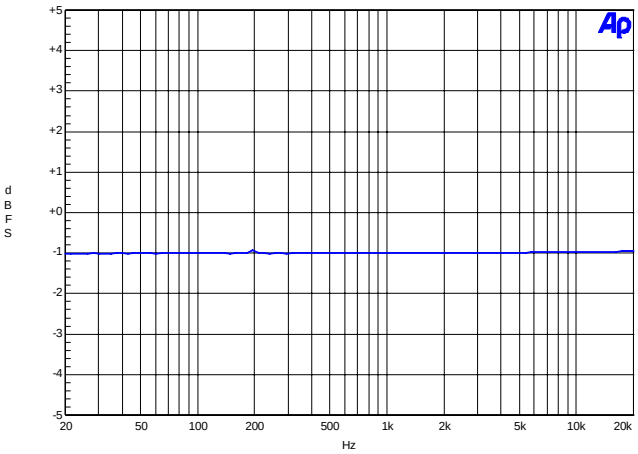


Figure 17. 48 kHz, Frequency Response

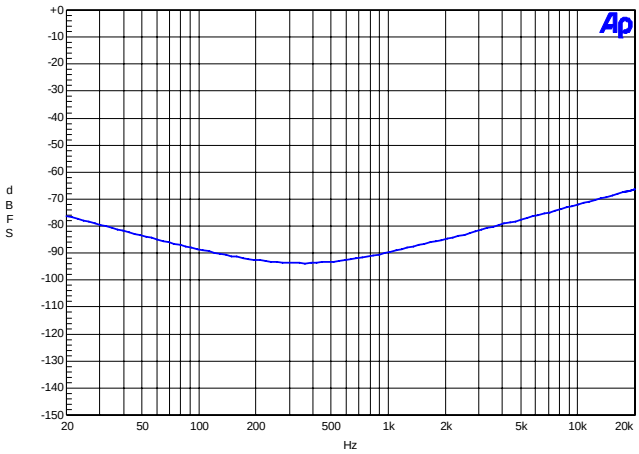


Figure 18. 48 kHz, Crosstalk

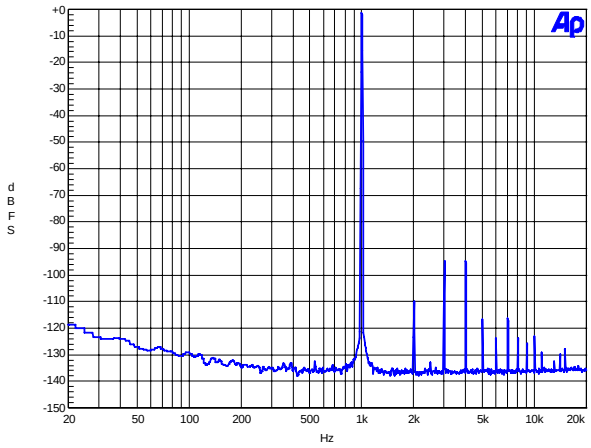


Figure 19. FFT (-1 dB 96 kHz)

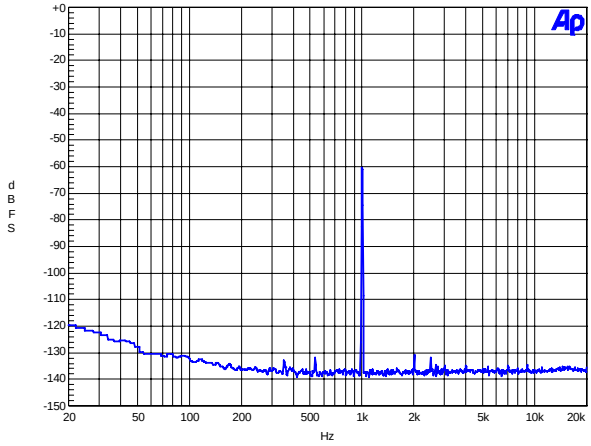


Figure 20. FFT (-60 dB, 96 kHz)

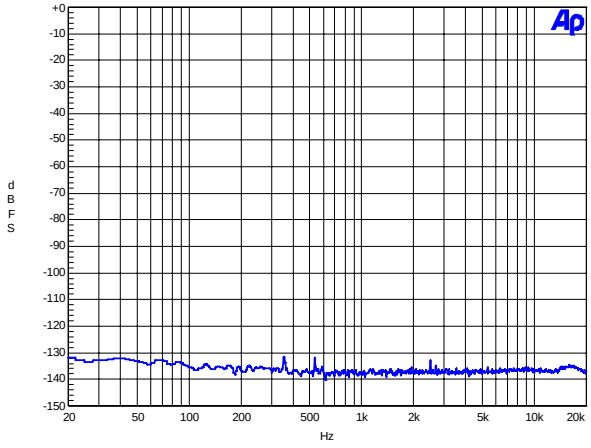


Figure 21. FFT (96 kHz, No Input)

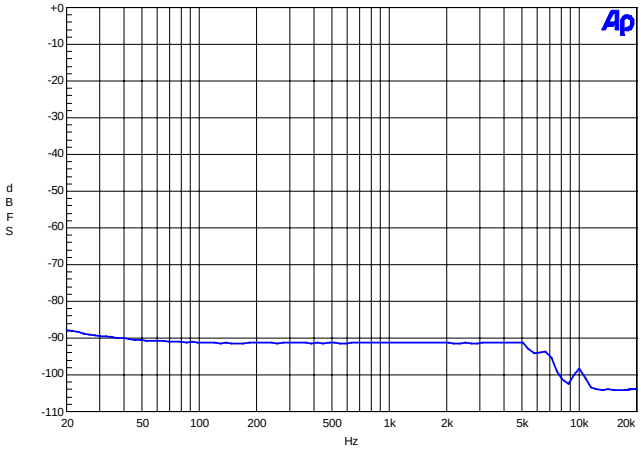


Figure 22. 96 kHz, THD+N vs. Input Freq

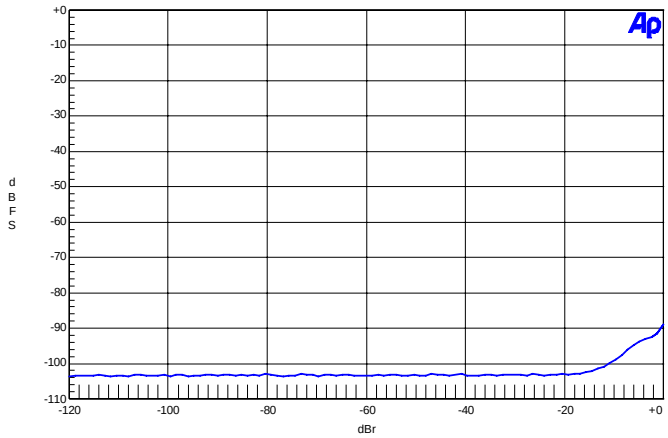


Figure 23. 96 kHz, THD+N vs. Level

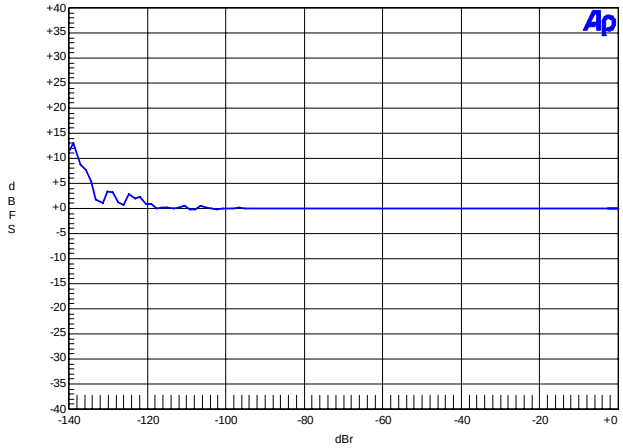


Figure 24. 96 kHz, Fade-to-Noise Linearity

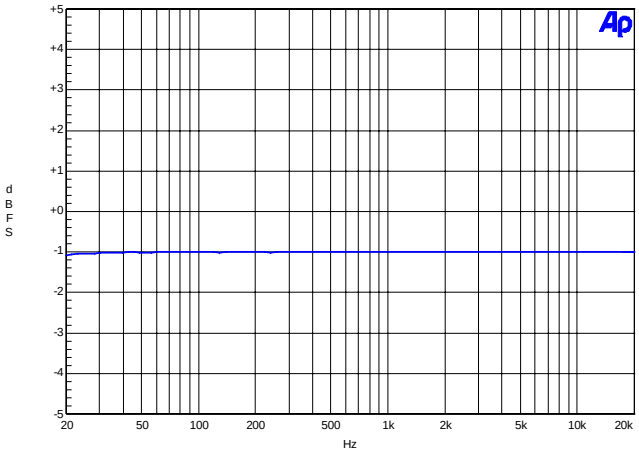


Figure 25. 96 kHz, Frequency Response

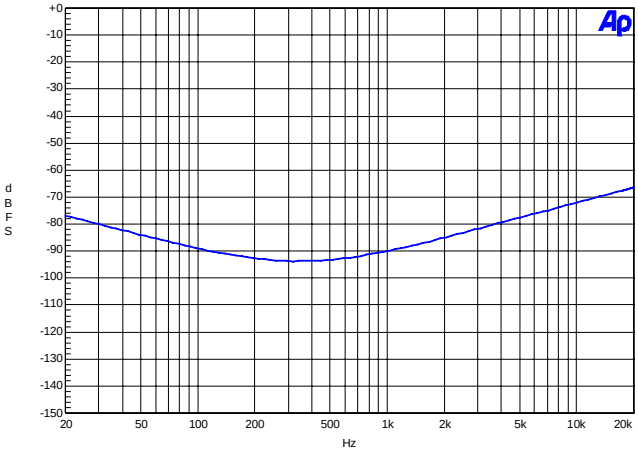


Figure 26. 96 kHz, Crosstalk

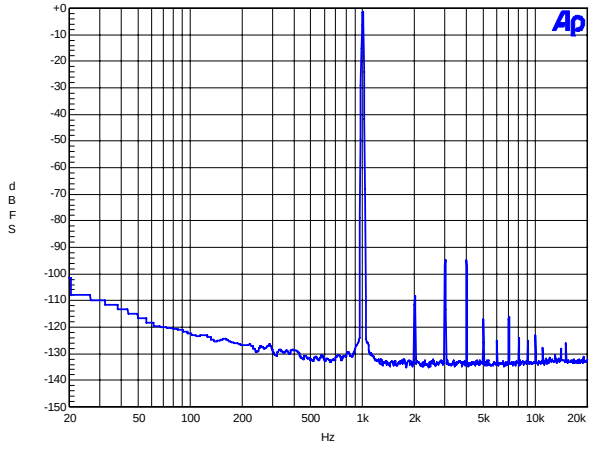


Figure 27. FFT (-1 dB 192 kHz)

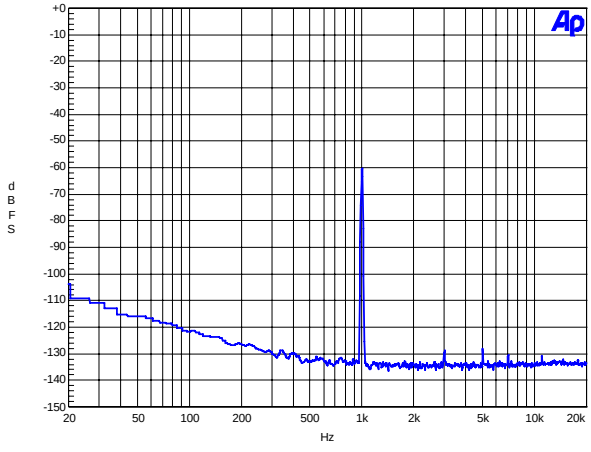


Figure 28. FFT (192 kHz, -60 dB)

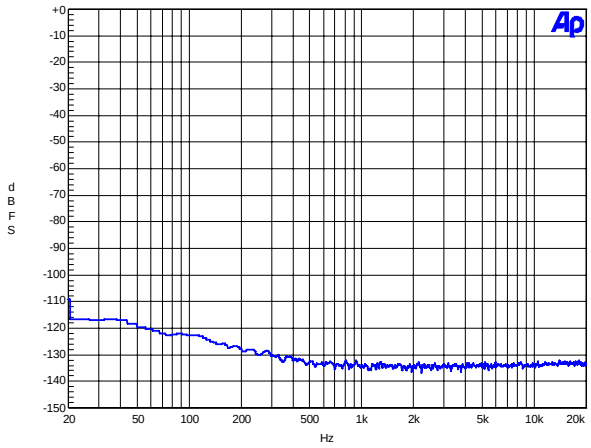


Figure 29. FFT (192 kHz, No Input)

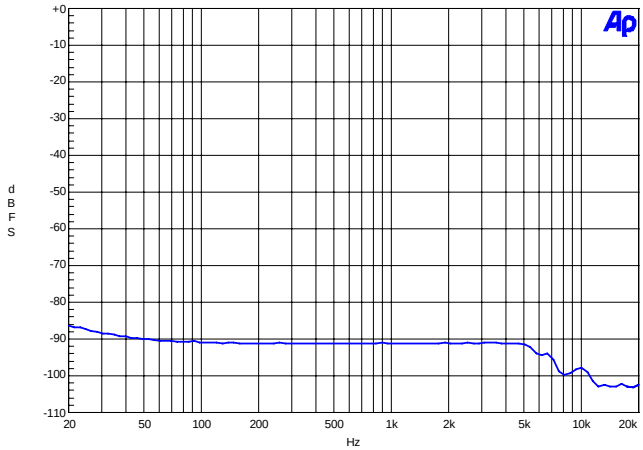


Figure 30. 192 kHz, THD+N vs. Input Freq

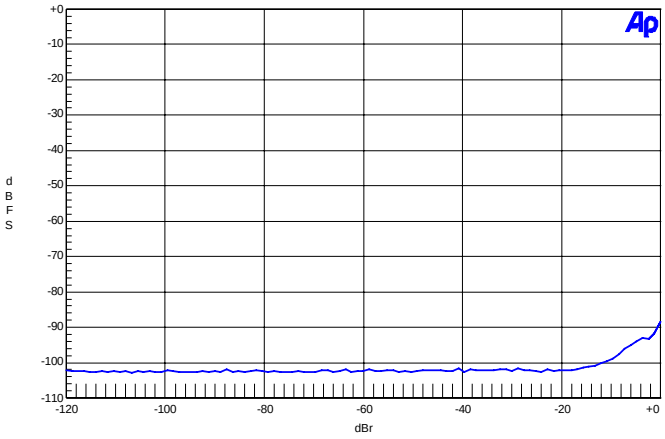


Figure 31. 192 kHz, THD+N vs. Level

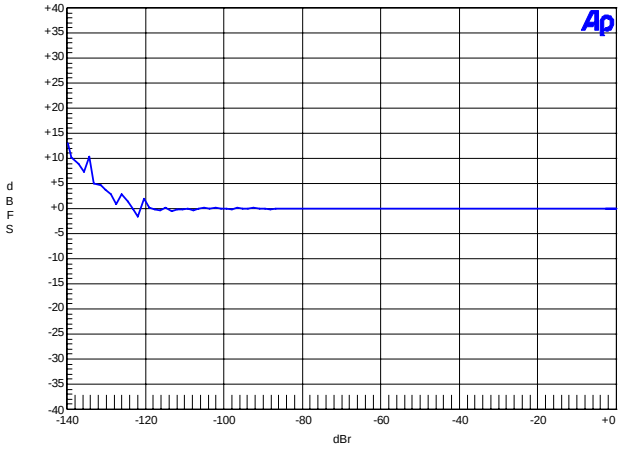


Figure 32. 192 kHz, Fade-to-Noise Linearity

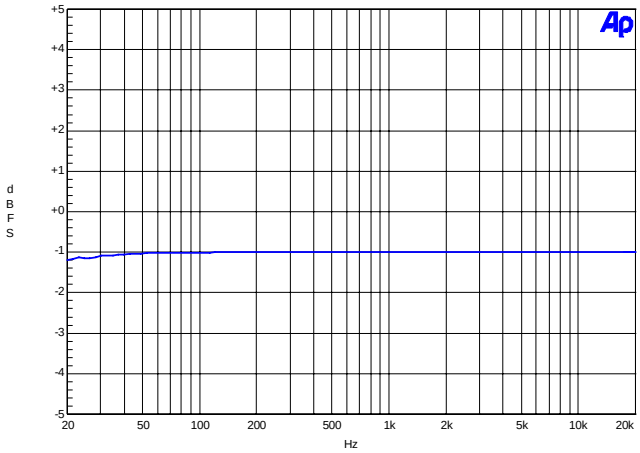


Figure 33. 192 kHz, Frequency Response

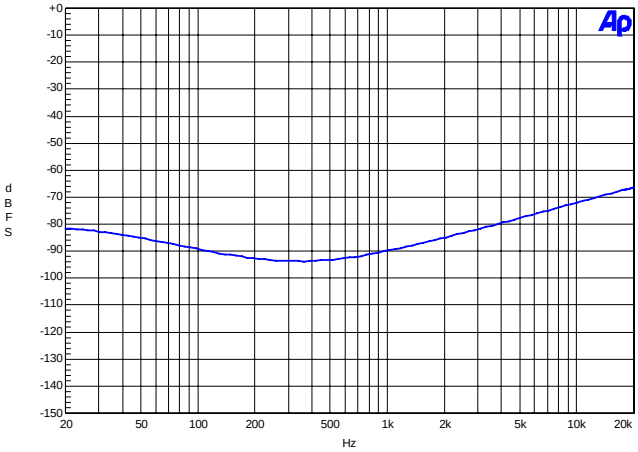


Figure 34. 192 kHz, Crosstalk

9. DAC PERFORMANCE PLOTS

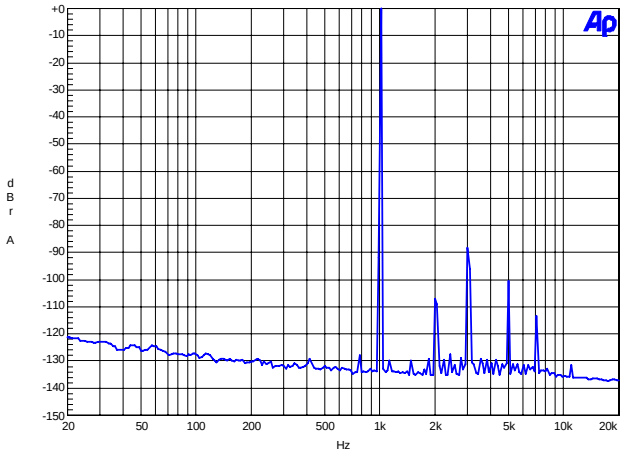


Figure 35. FFT (48 kHz, 0 dB)

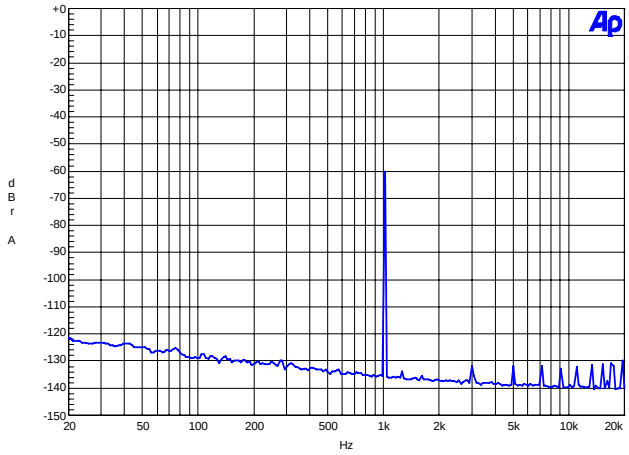


Figure 36. FFT (48 kHz, -60 dB)

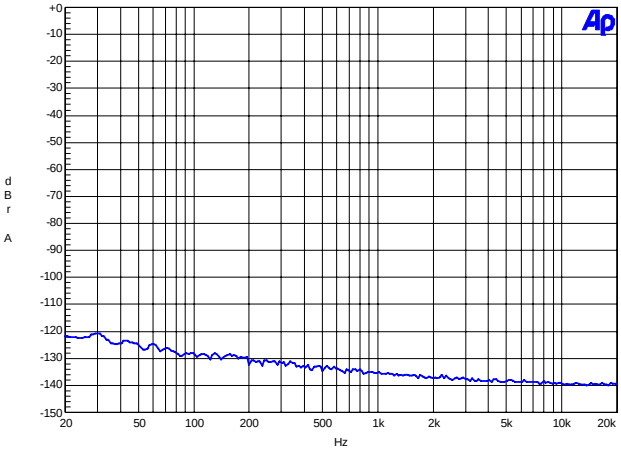


Figure 37. FFT (48 kHz, No Input)

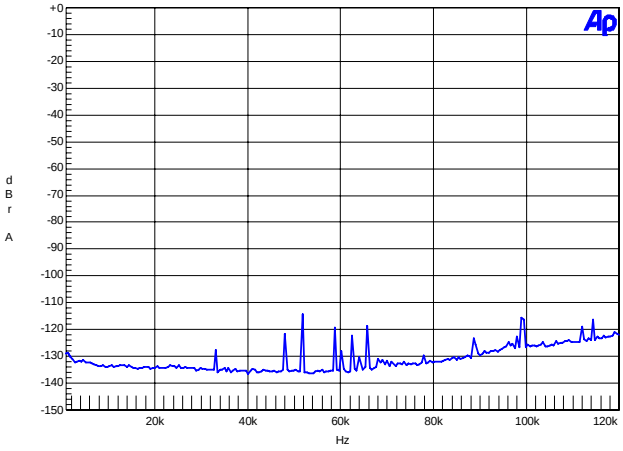


Figure 38. FFT (48 kHz Out-of-Band, No Input)

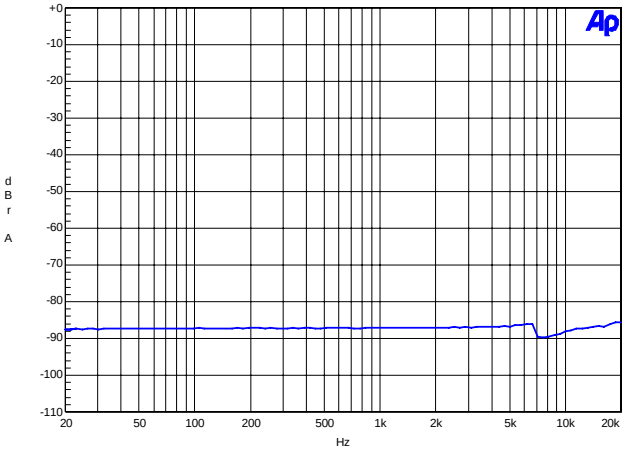


Figure 39. 48 kHz, THD+N vs. Input Freq

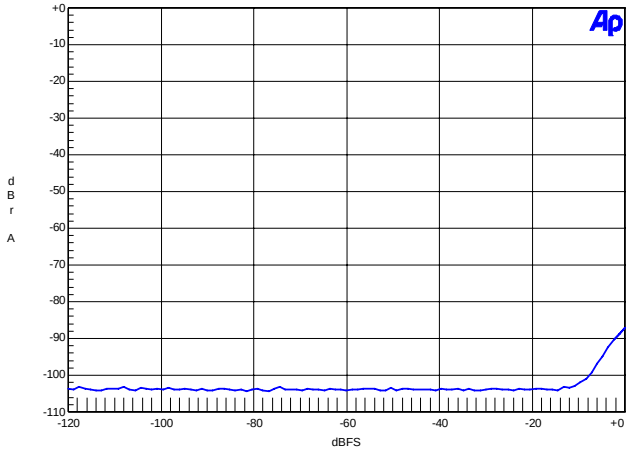


Figure 40. 48 kHz, THD+N vs. Level

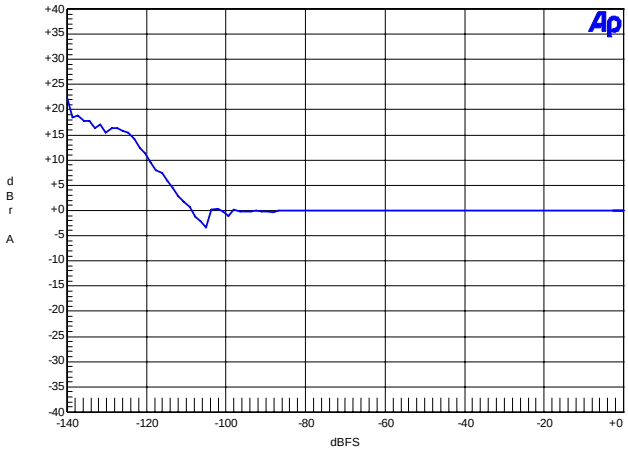


Figure 41. 48 kHz, Fade-to-Noise Linearity

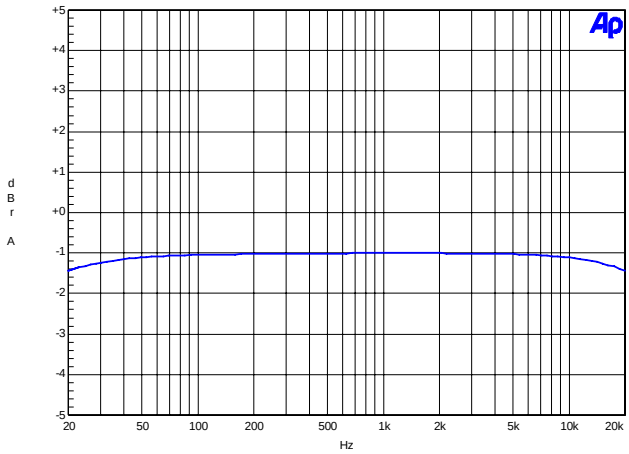


Figure 42. 48 kHz, Frequency Response

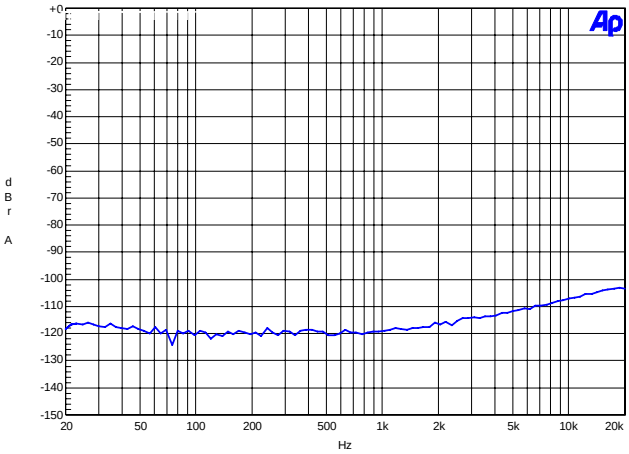


Figure 43. 48 kHz, Crosstalk

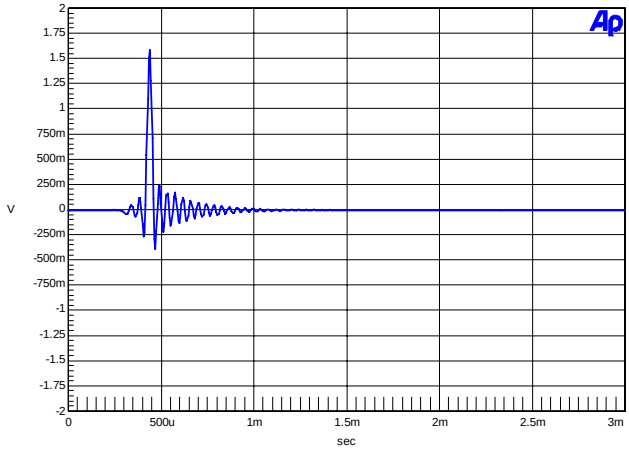


Figure 44. 48 kHz, Impulse Response

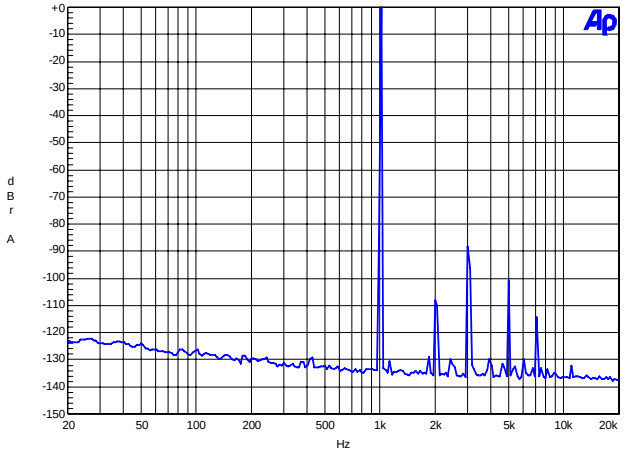


Figure 45. FFT (96 kHz, 0 dB)

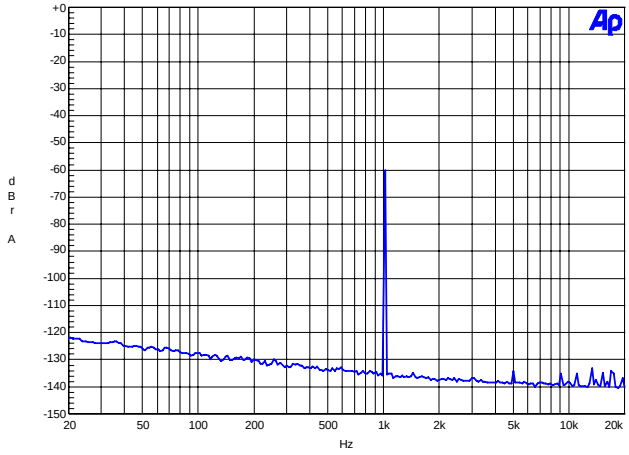


Figure 46. FFT (96 kHz, -60 dB)

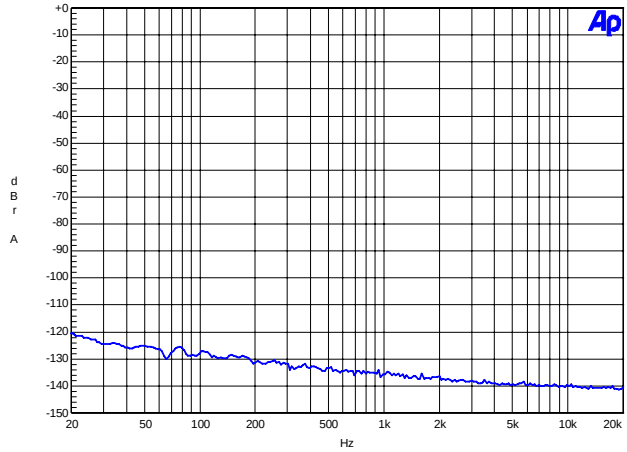


Figure 47. FFT (96 kHz, No Input)

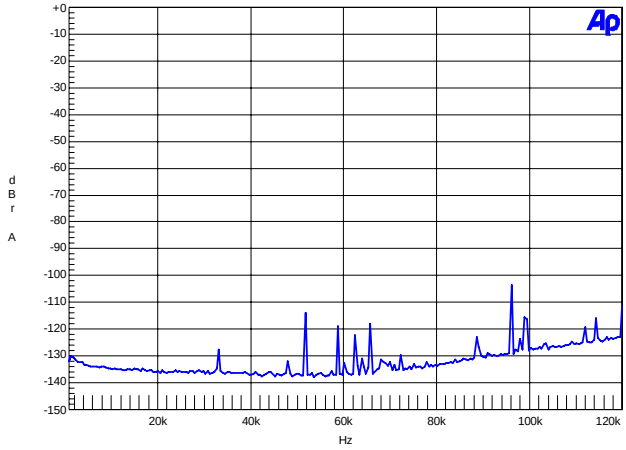


Figure 48. FFT (96 kHz Out-of-Band, No Input)

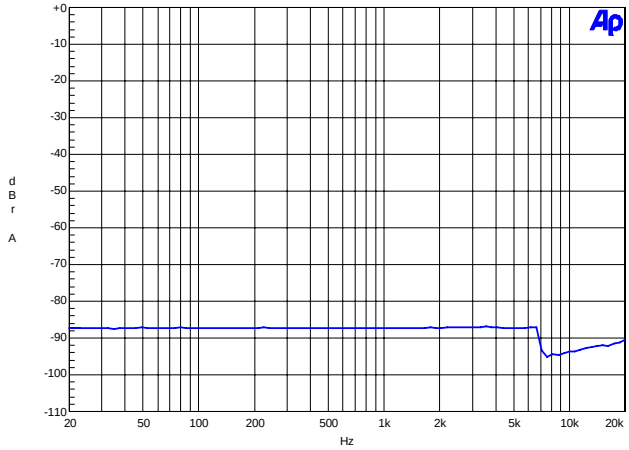


Figure 49. 96 kHz, THD+N vs. Input Freq

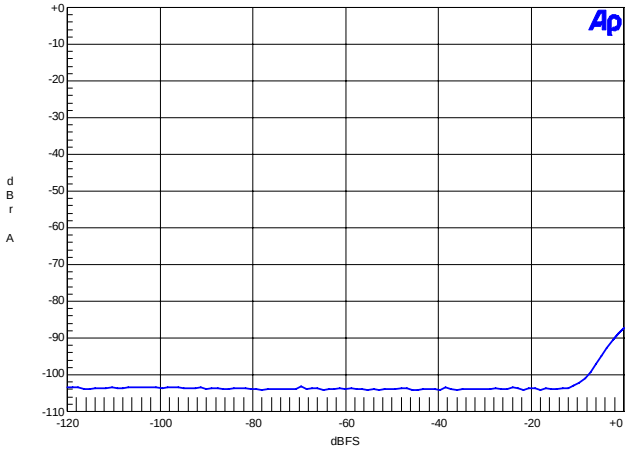


Figure 50. 96 kHz, THD+N vs. Level

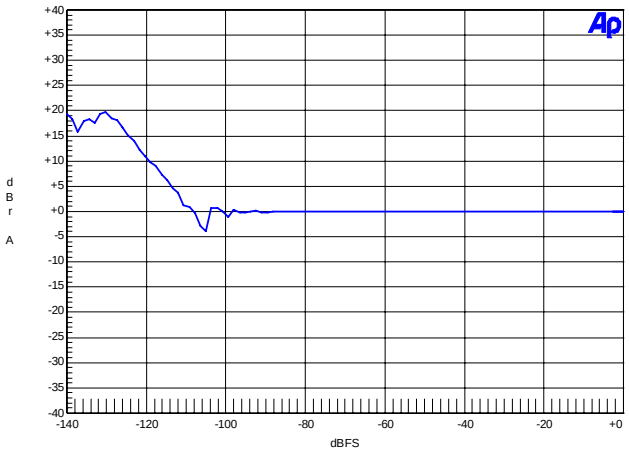


Figure 51. 96 kHz, Fade-to-Noise Linearity

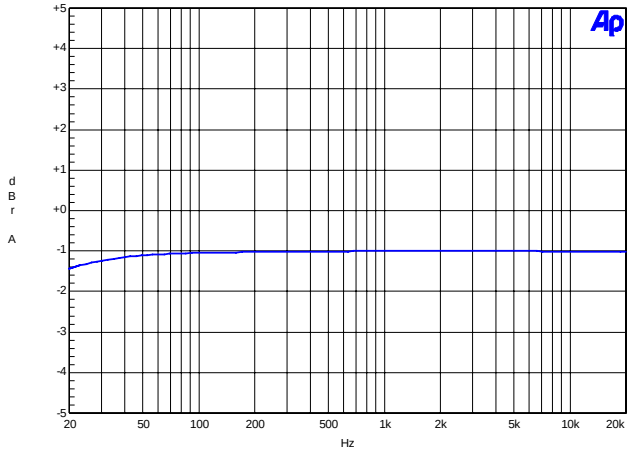


Figure 52. 96 kHz, Frequency Response

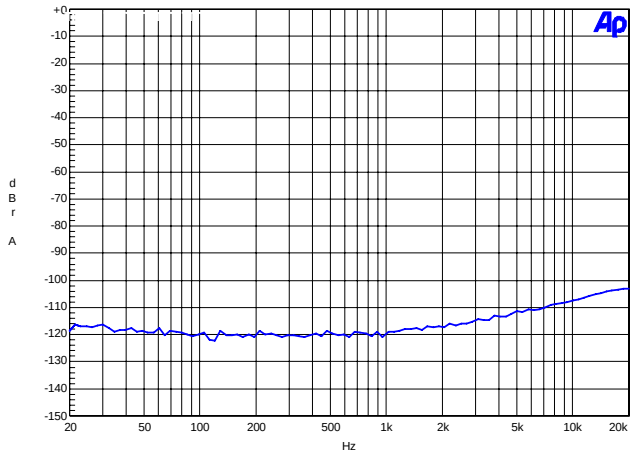


Figure 53. 96 kHz, Crosstalk

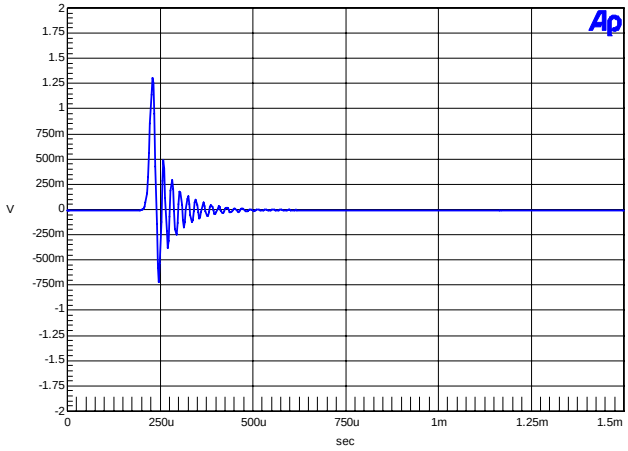


Figure 54. 96 kHz, Impulse Response

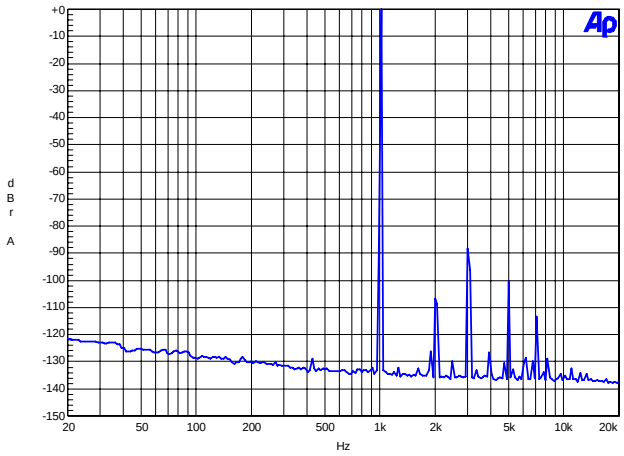


Figure 55. FFT (192 kHz, 0 dB)

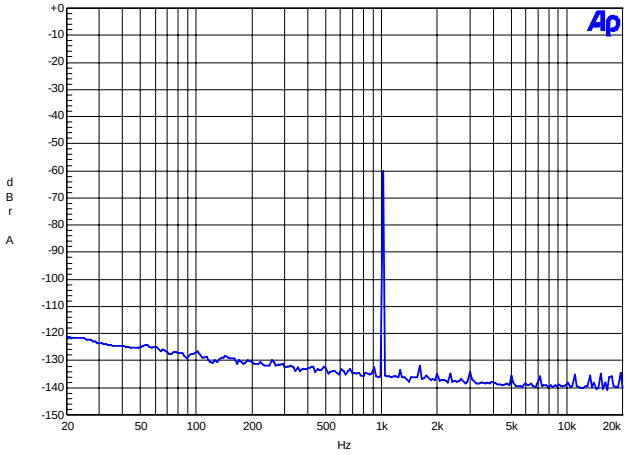


Figure 56. FFT (192 kHz, -60 dB)

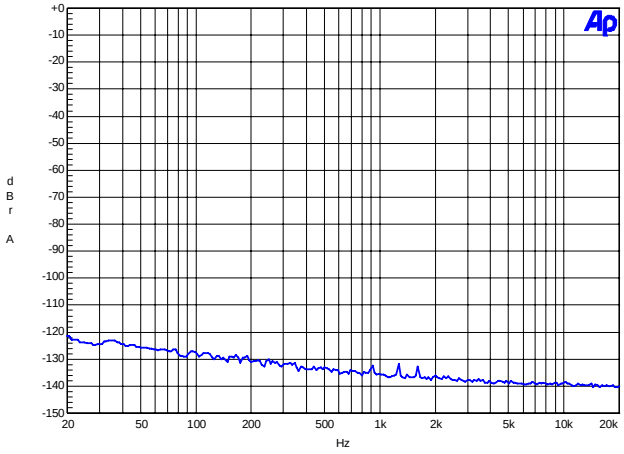


Figure 57. FFT (192 kHz, No Input)

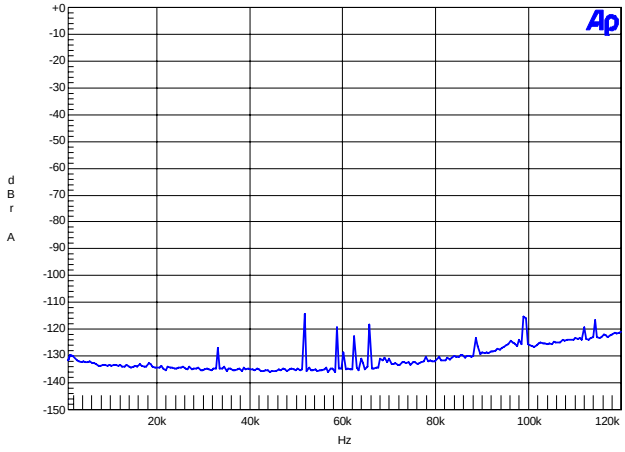


Figure 58. FFT (192 kHz Out-of-Band, No Input)

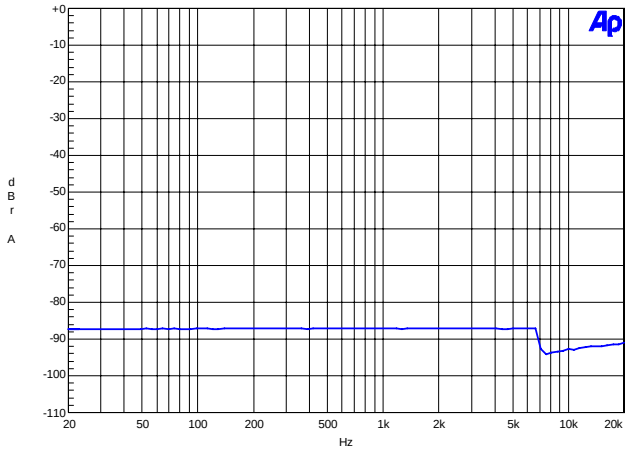


Figure 59. 192 kHz, THD+N vs. Input Freq

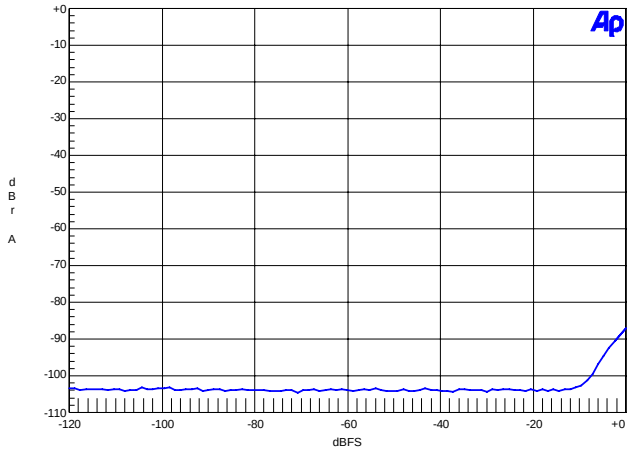


Figure 60. 192 kHz, THD+N vs. Level

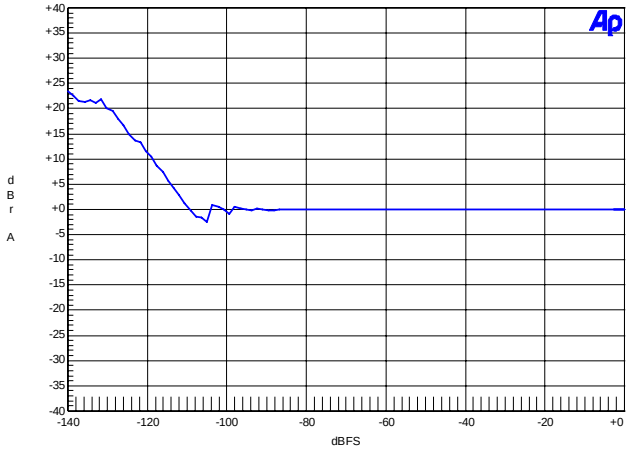


Figure 61. 192 kHz, Fade-to-Noise Linearity

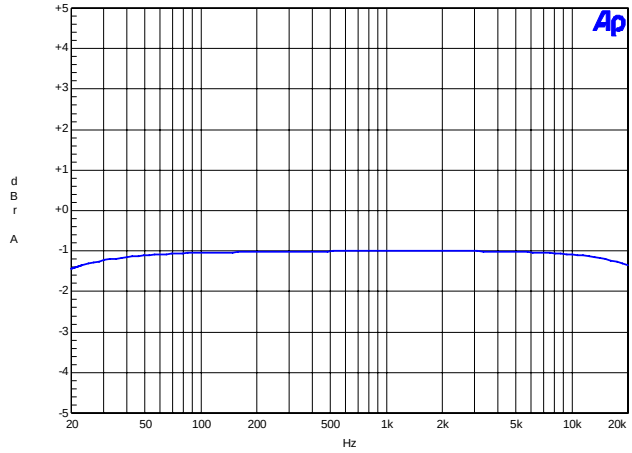


Figure 62. 192 kHz, Frequency Response

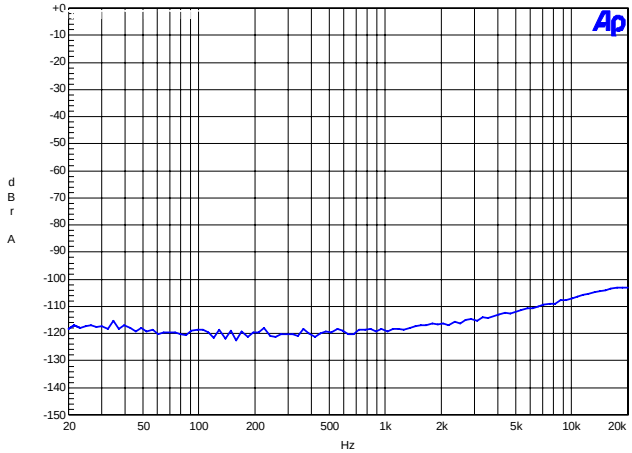


Figure 63. 192 kHz, Crosstalk

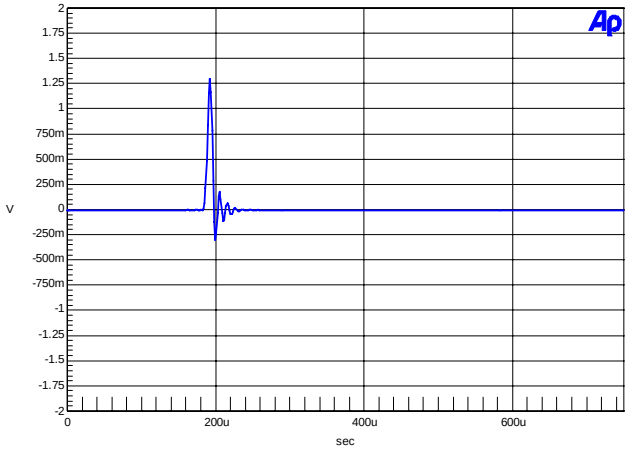


Figure 64. 192 kHz, Impulse Response

10. CDB BLOCK DIAGRAM

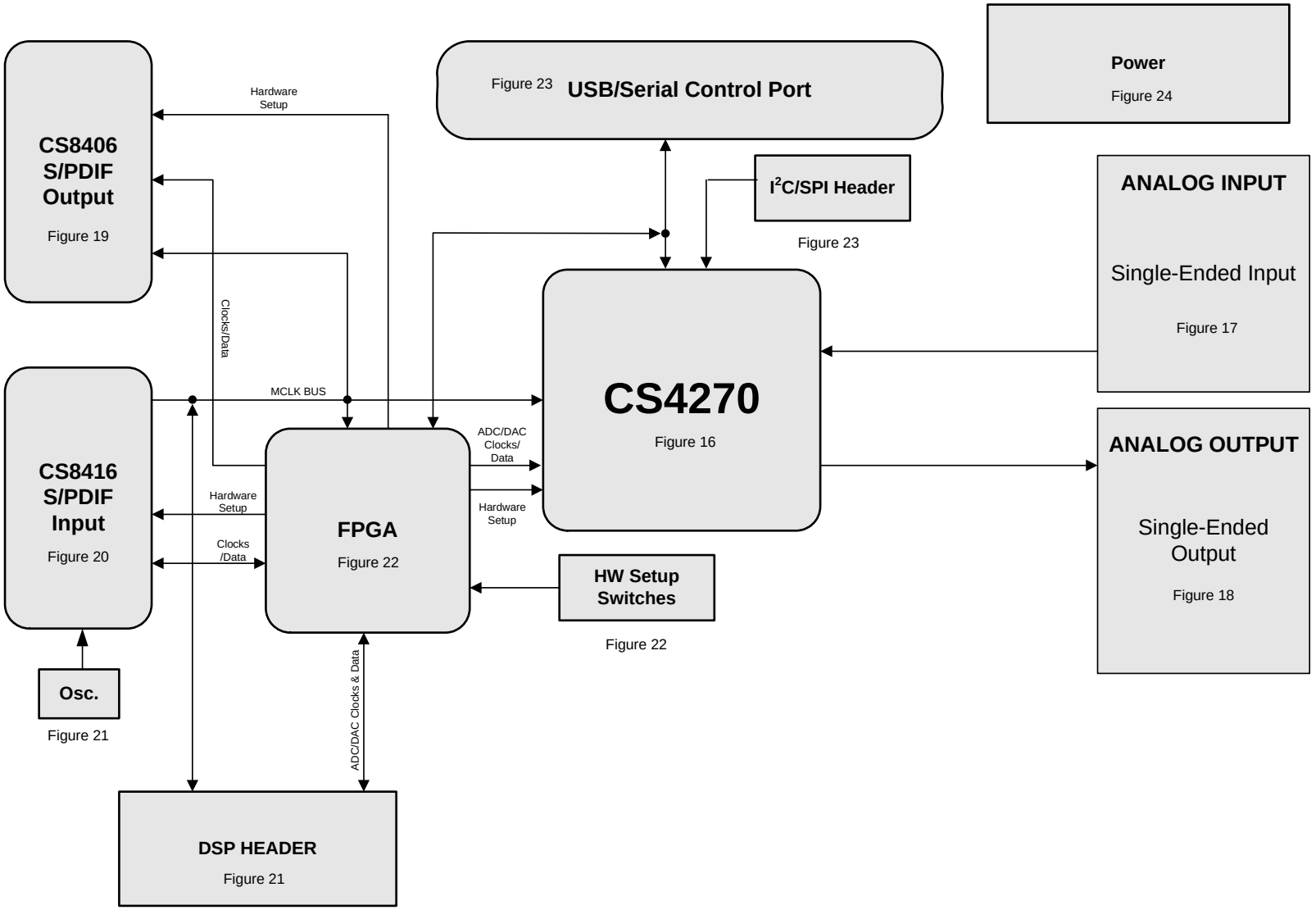
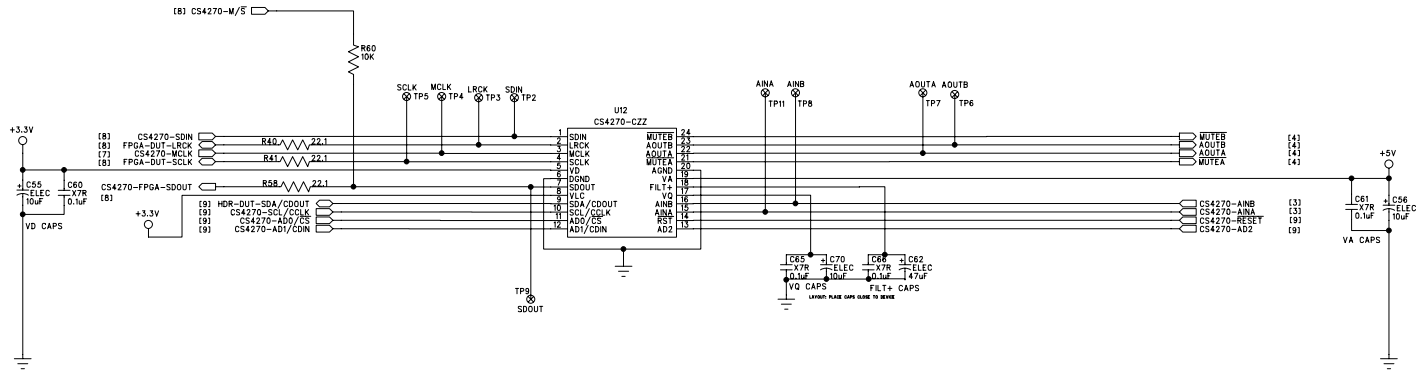


Figure 65. Block Diagram

11. CDB SCHEMATICS



NOTES: UNLESS OTHERWISE SPECIFIED;

1. ALL RESISTORS VALUES ARE IN OHMS.

Figure 66. CS4270

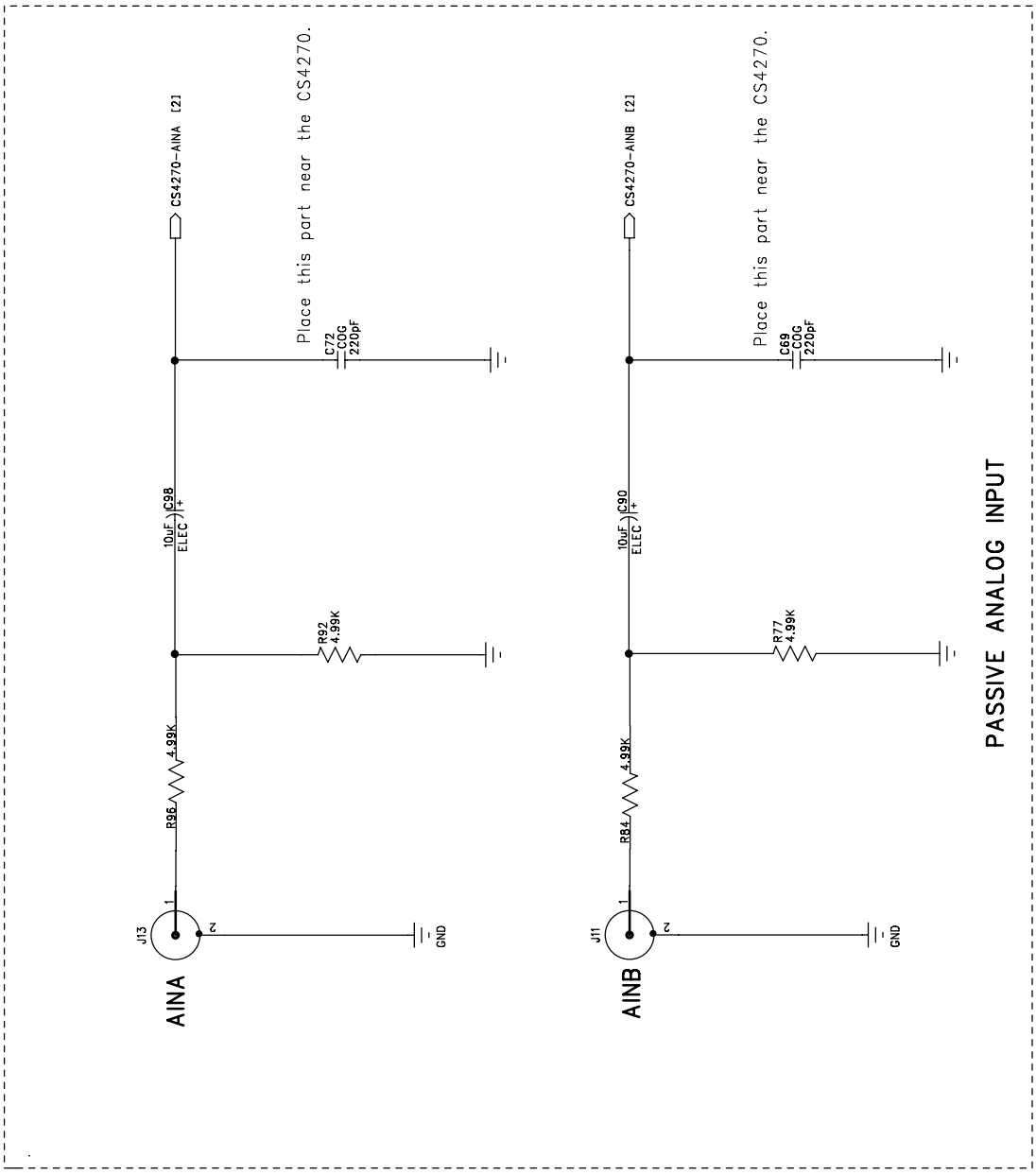


Figure 67. Analog Input

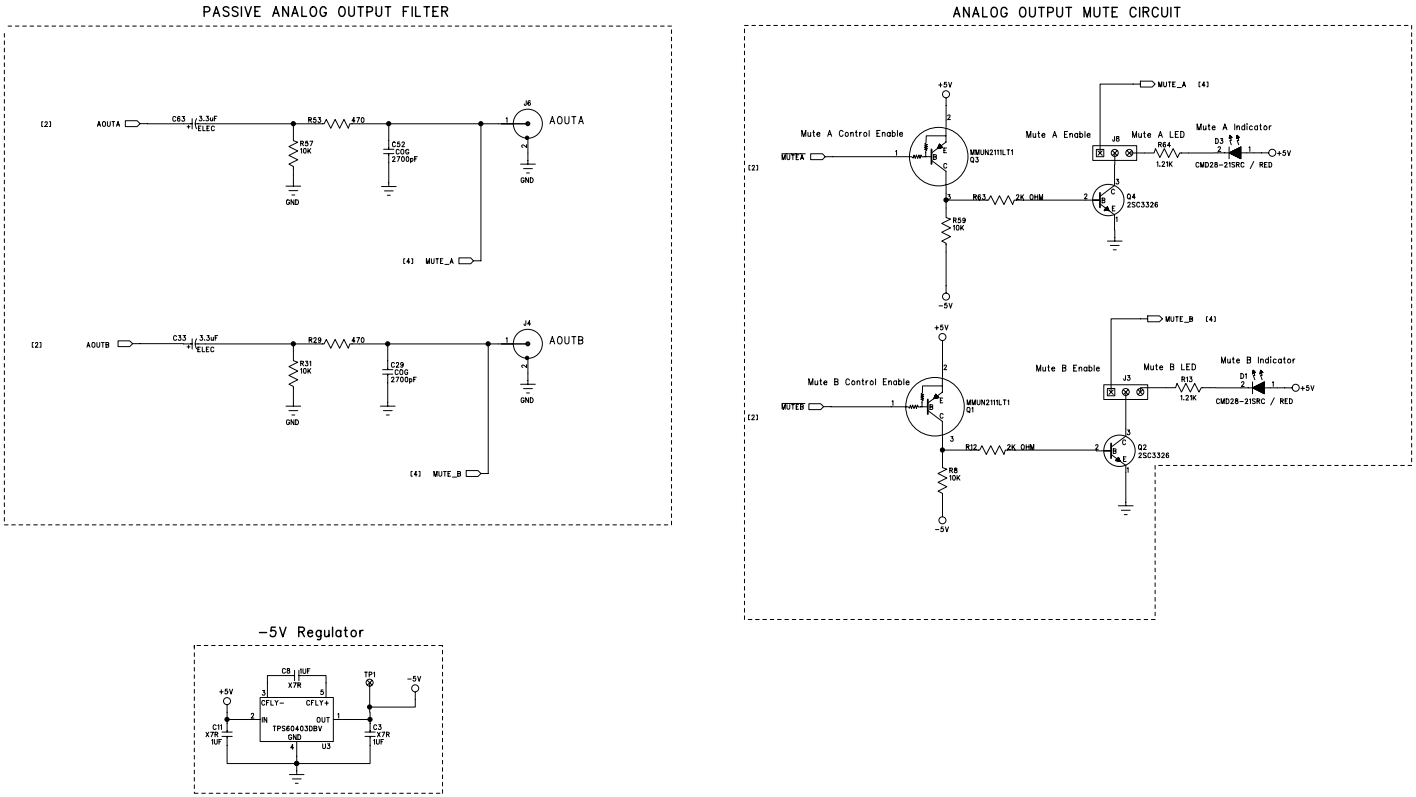


Figure 68. Analog Output

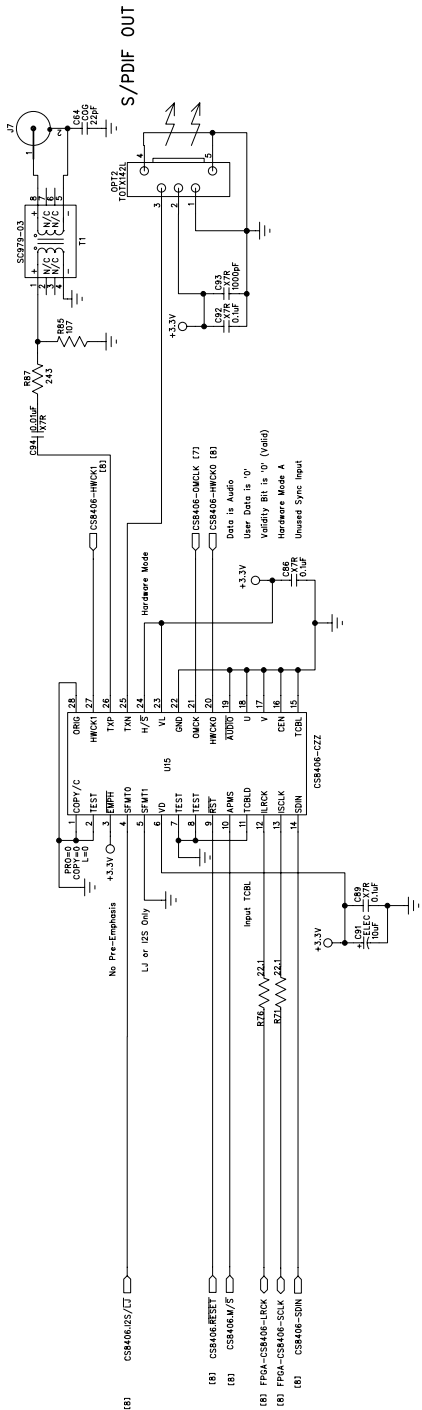


Figure 69. CS8406 S/PDIF Transmitter

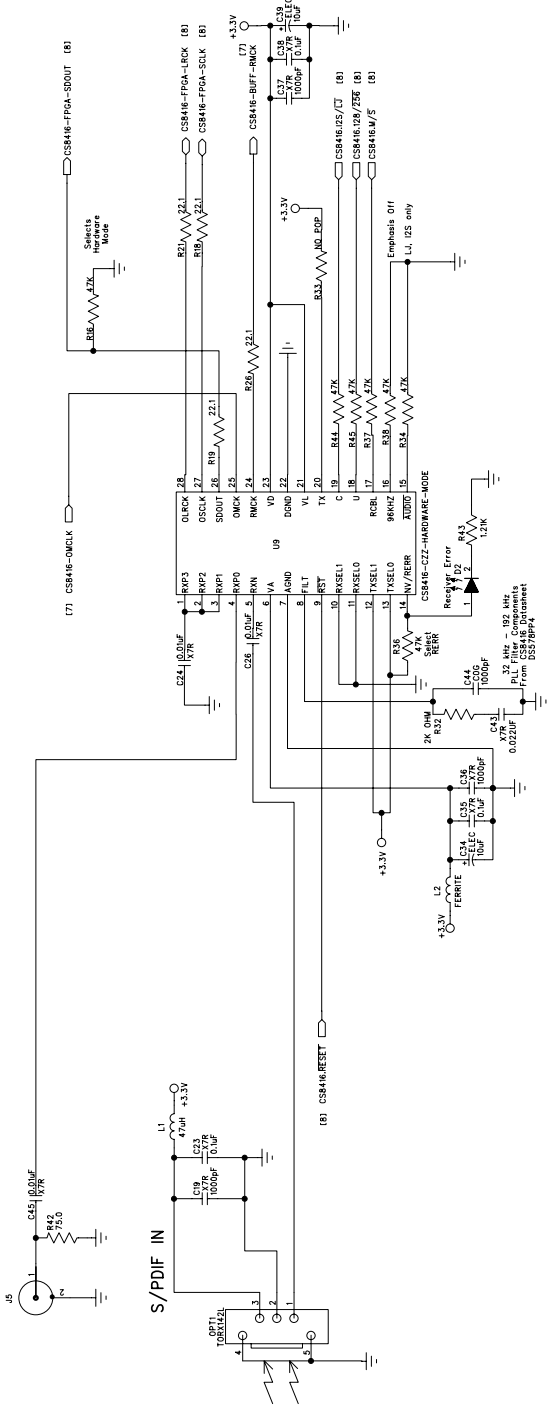


Figure 70. CS8416 S/PDIF Receiver

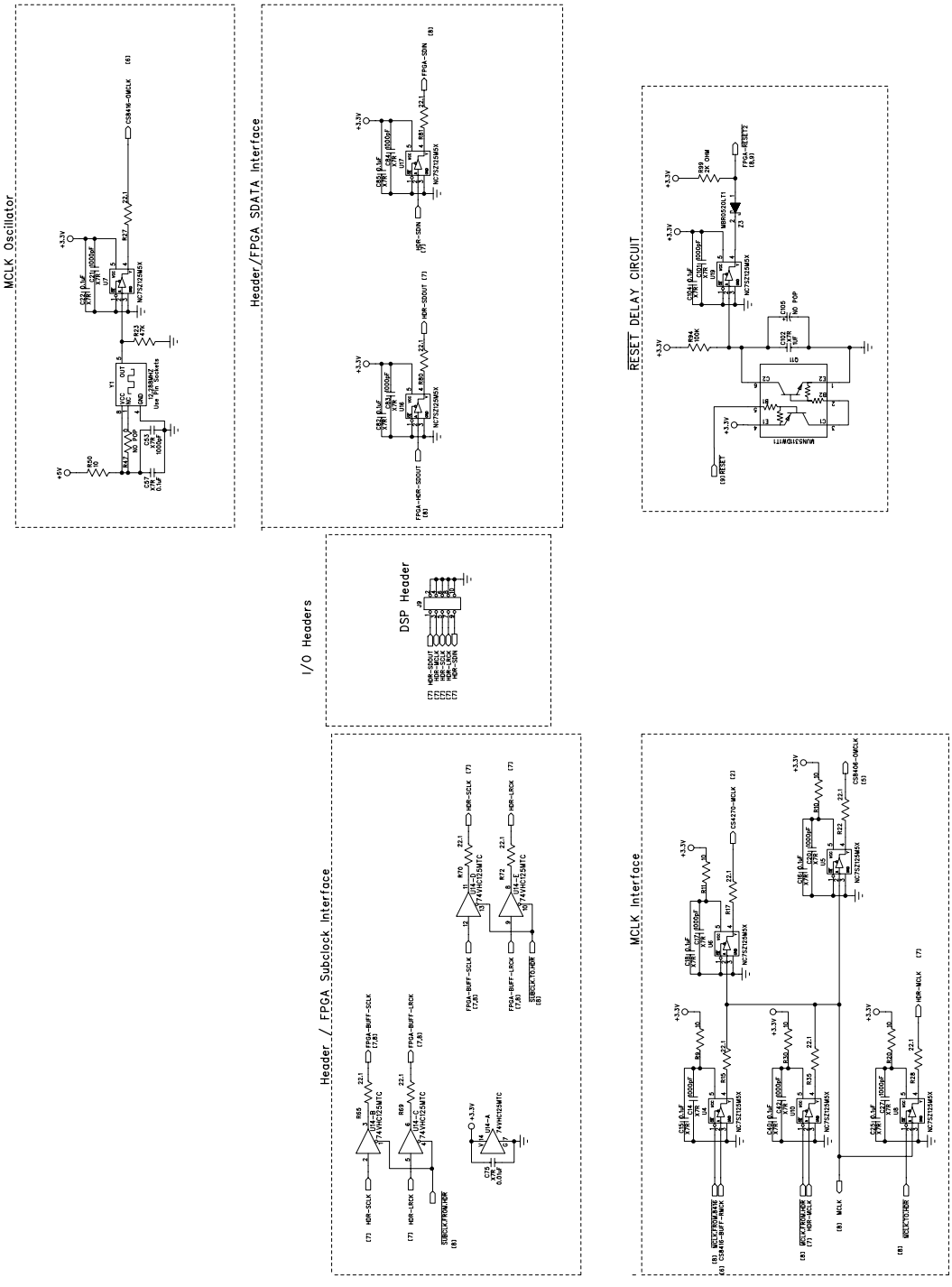


Figure 71. Buffers - Clock/Data Routing

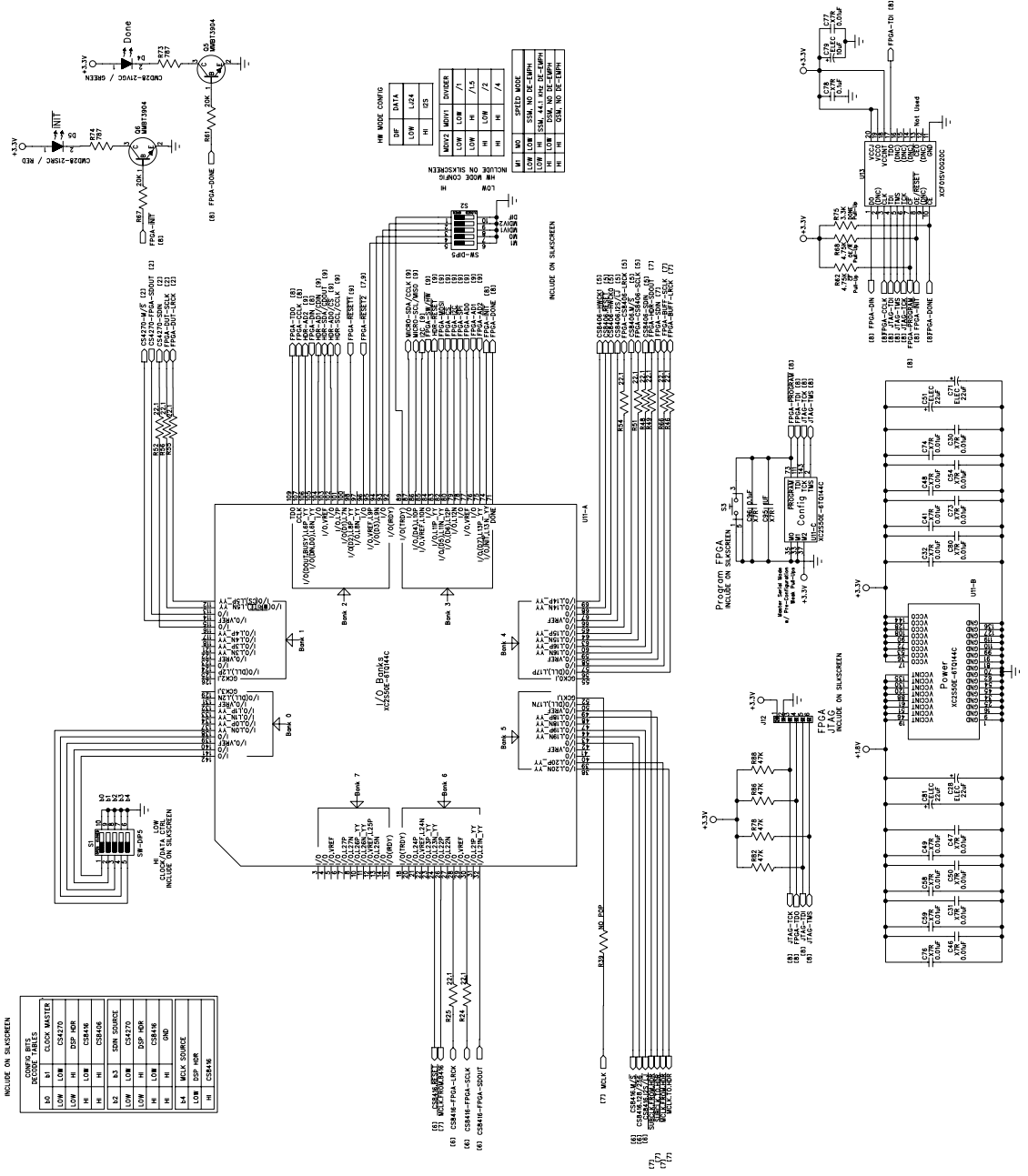


Figure 72. FPGA

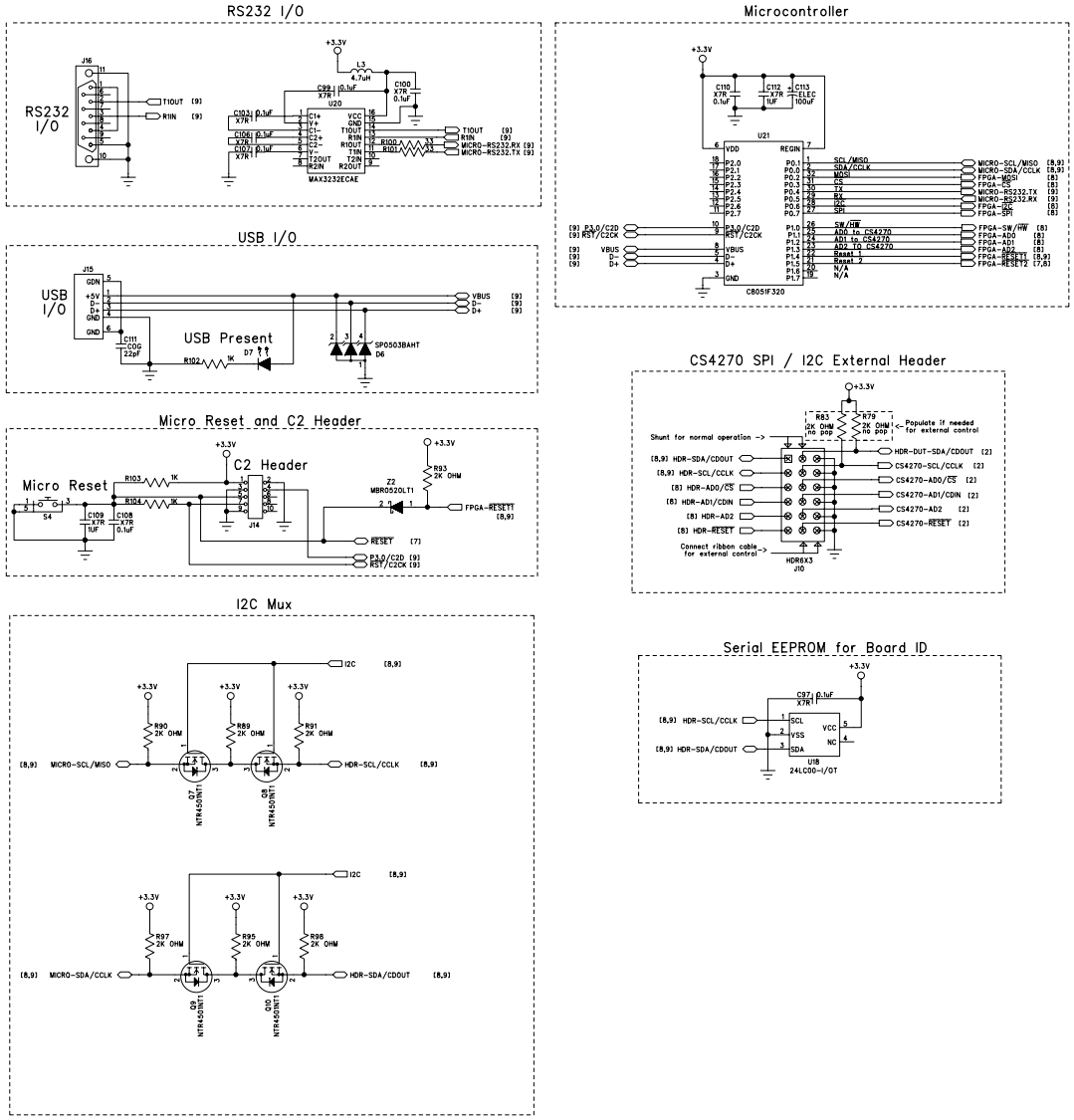


Figure 73. USB/RS232 Microprocessor

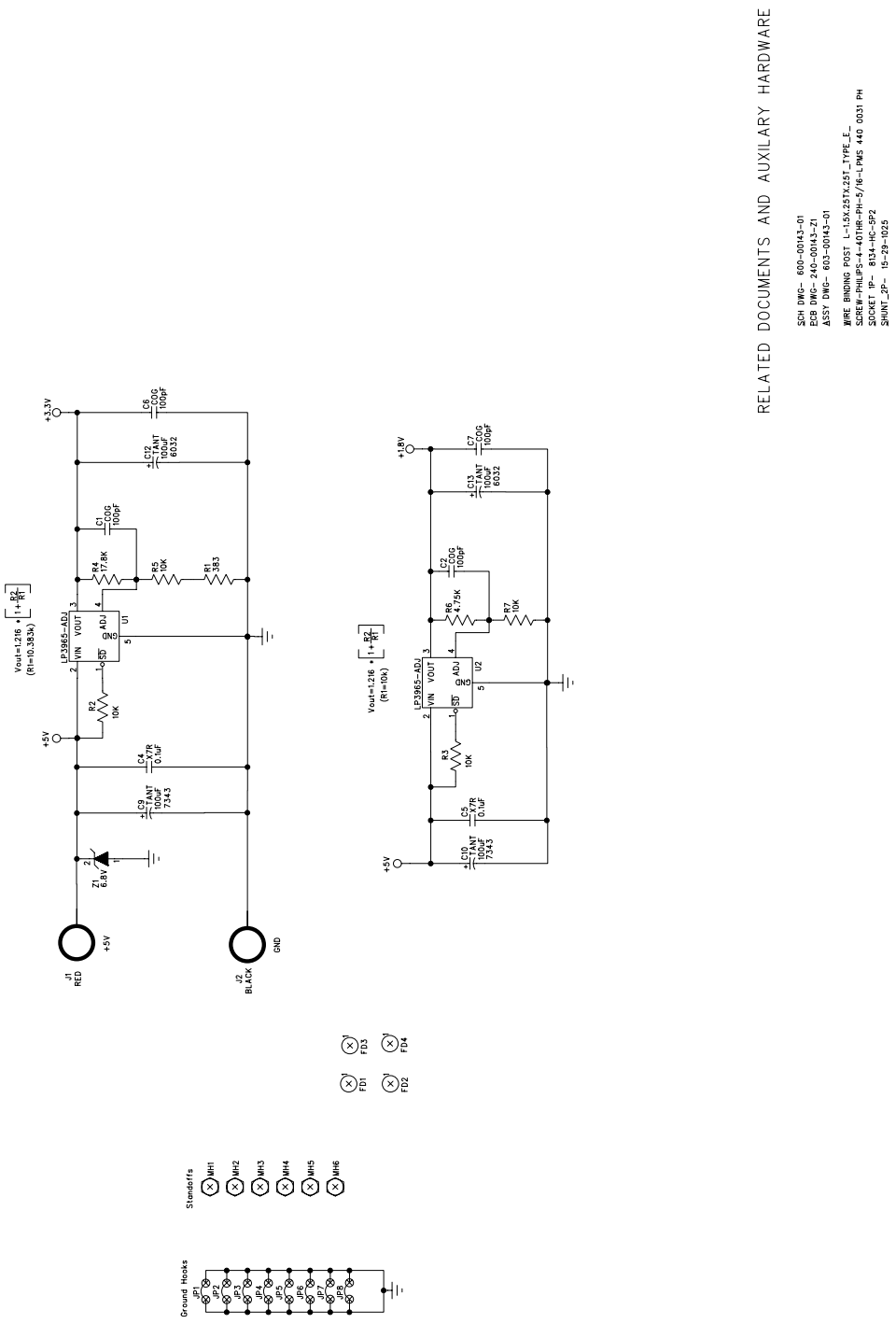


Figure 74. Power

12. CDB LAYOUT

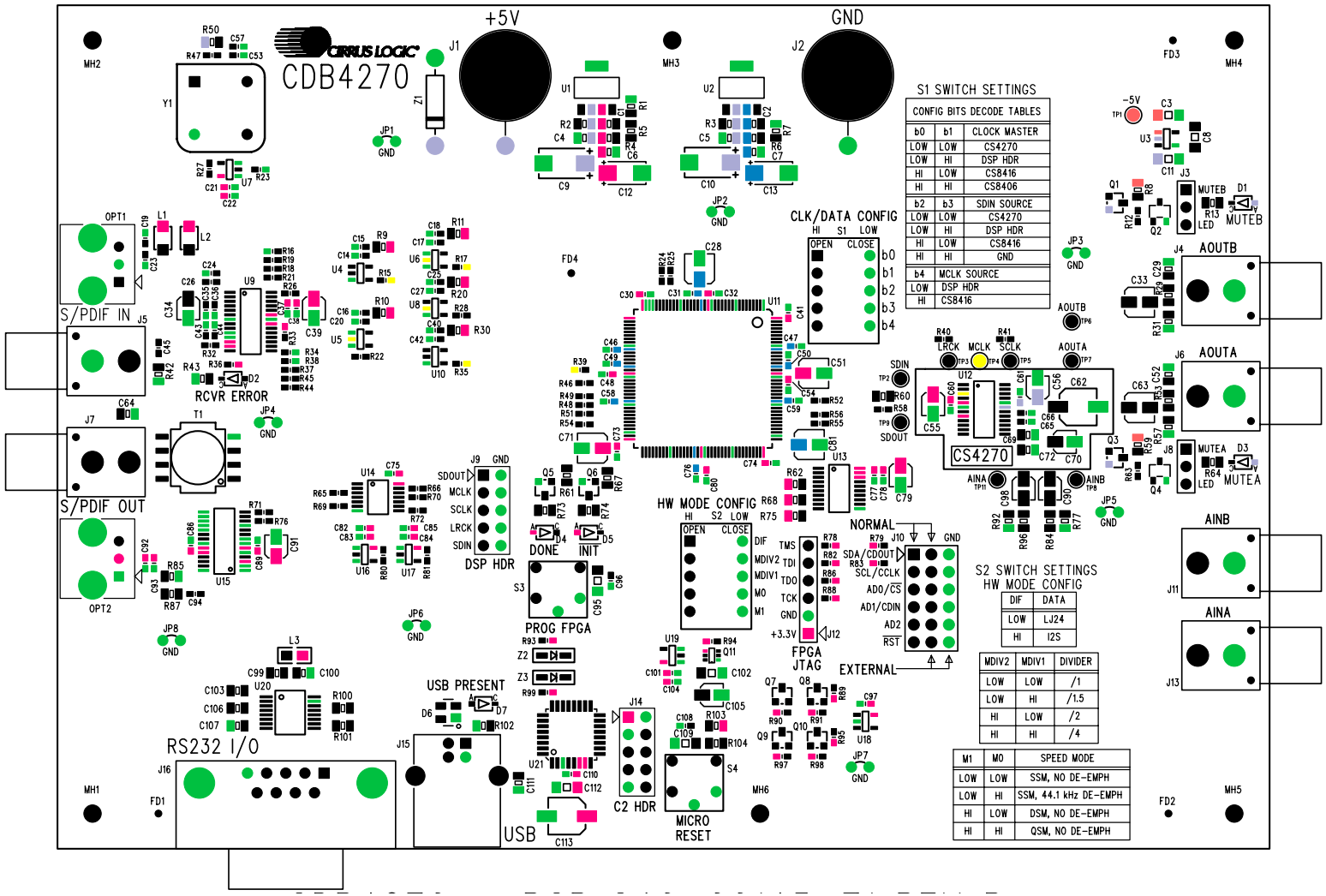


Figure 75. Silk Screen

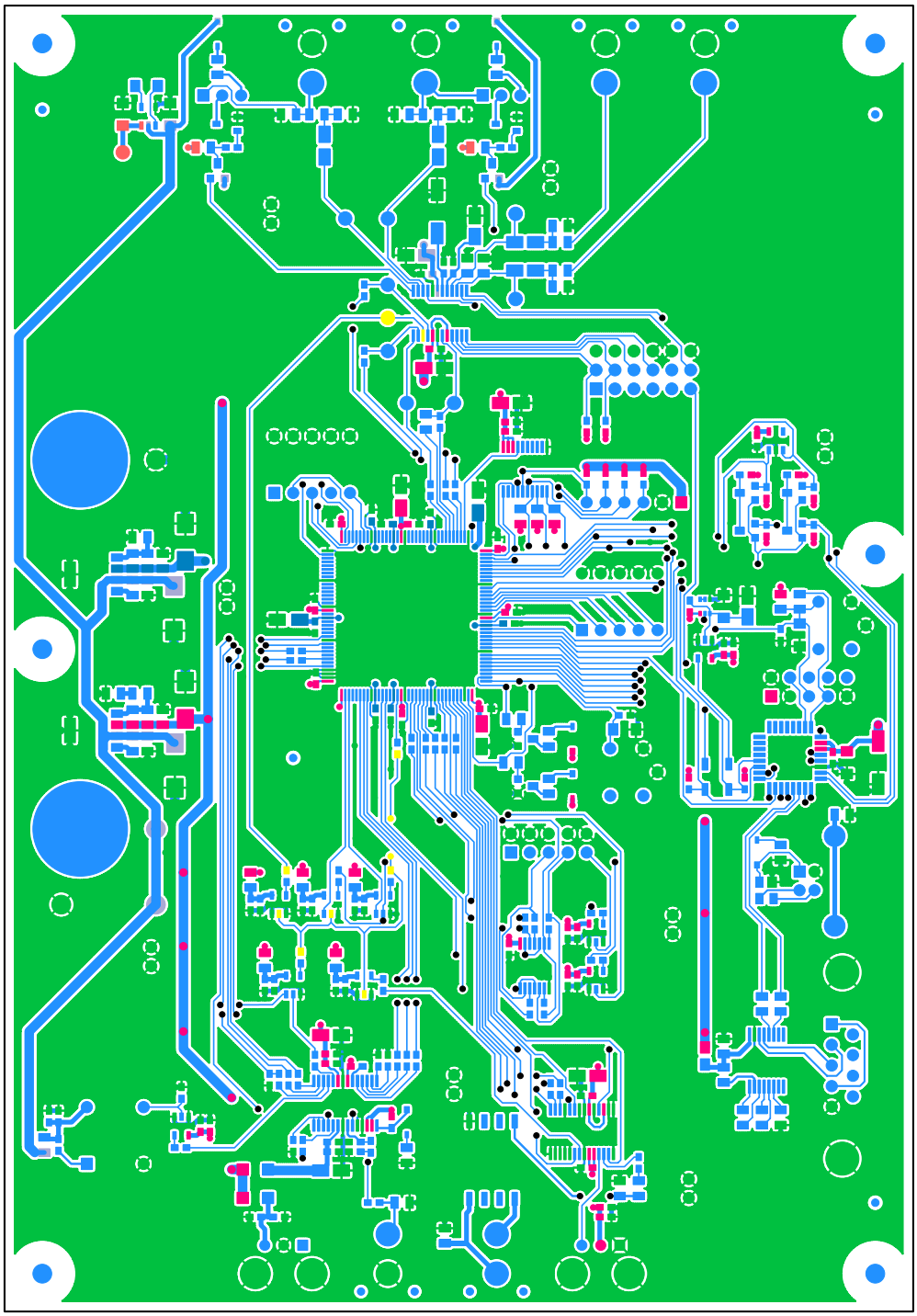


Figure 76. Top-Side Layer

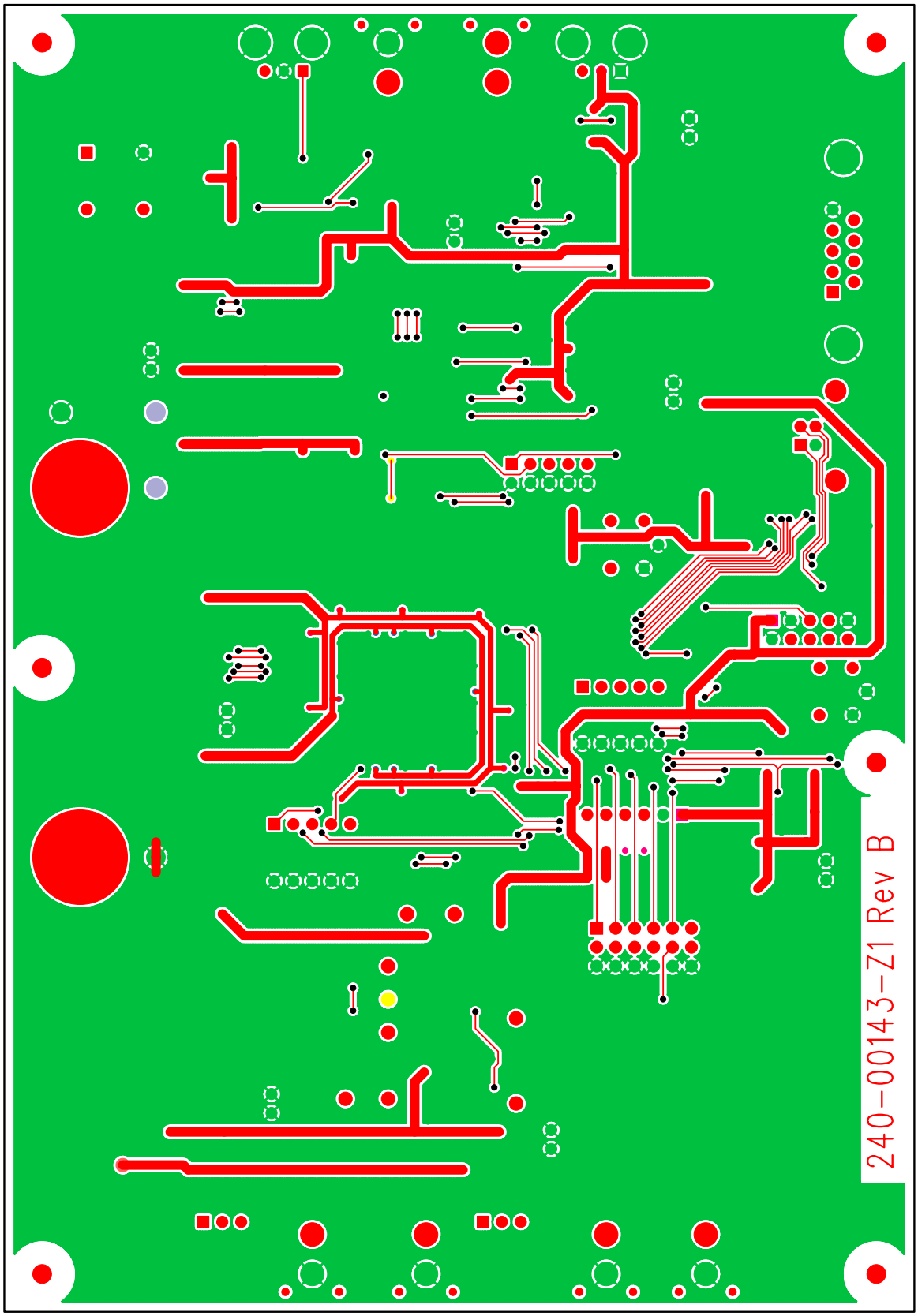


Figure 77. Bottom-Side Layer

13. CHANGES MADE TO REV. B BOARD

13.1 Modifications (Done by Cirrus Logic)

Note: There is no rework necessary when CS4270 C0 parts are installed on the Rev. B board. See CDB Data Sheet DS686DB2 when B0 parts are installed on the Rev. B board or DS686DB1 when A0 parts are installed on the Rev. A board. Also reference the Rev. A0, B0, and C0 chip Errata at http://www.cirrus.com/en/support. Select **Errata** from the product information categories shown.

14. REVISION HISTORY

Revision	Changes
DB1	Initial Release: Applies to A Assy. (A2 PL).
DB2	This Revision is for the B Assy. (B2 PL). Updates for USB port use, new GUI graphics, new schematics, new rework information, new layout graphics and added performance plots. Removed Rev. A/A1 (PL) references, schematics, layout graphics and rework.
DB3	Added Performance Plots Replaced Figure 67 on page 38 Deleted Figure 28, Board Modifications

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.