19-3206; Rev 0; 1/08

EVALUATION KIT AVAILABLE

315MHz/390MHz Dual-Frequency ASK Transmitter

General Description

The MAX7058 UHF transmitter alternately transmits ASK/OOK data at 315MHz or 390MHz using a single crystal. The MAX7058 has internal tuning capacitors at the output of the power amplifier that can be programmed for matching to the antenna or load. The MAX7058 can transmit at a data rate up to 100kbps NRZ (50kbps Manchester coded). Typical transmitted power into a 50Ω load is +10dBm. The MAX7058 operates from +2.1V to +3.6V and draws under 8.0mA of current. The standby current is less than 1µA at room temperature. A 15MHz crystal is used as the reference for 315MHz and 390MHz operation by selecting synthesizer-divide ratios of 21 and 26, respectively.

The MAX7058 is available in a 4mm x 4mm, 24-pin thin QFN package and is specified to operate in the -40°C to +125°C automotive temperature range.

Features

- **Switched 315MHz/390MHz Carrier Frequency Using One Crystal**
- **+2.1V to +3.6V Single-Supply Operation**
- **ASK/OOK Modulation**
- **Internal Switched Capacitors for Optimum Dual-Frequency Operation**
- **8.0mA DC Current Drain (50% Duty Cycle OOK)**
- **0.8µA Standby Current**
- **Small 4mm x 4mm, 24-Pin Thin QFN Package**

Applications

Garage Door Openers
RF Remote Controls
Home Automation
Wireless Sensors
Security Systems
Automotive

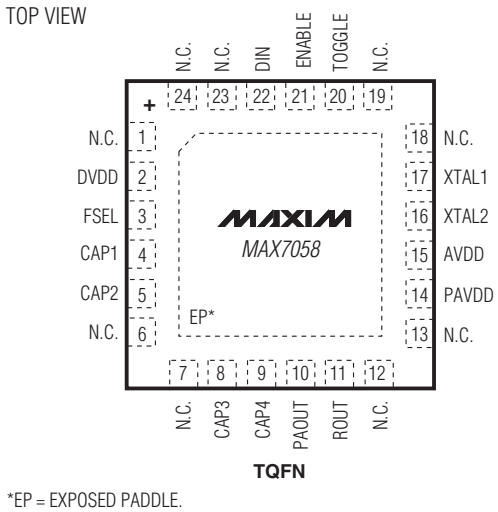
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX7058ATG+	-40°C to +125°C	24 Thin QFN-EP* (4mm x 4mm)	T2444+3

+Denotes a lead-free package.

**EP = Exposed paddle.*

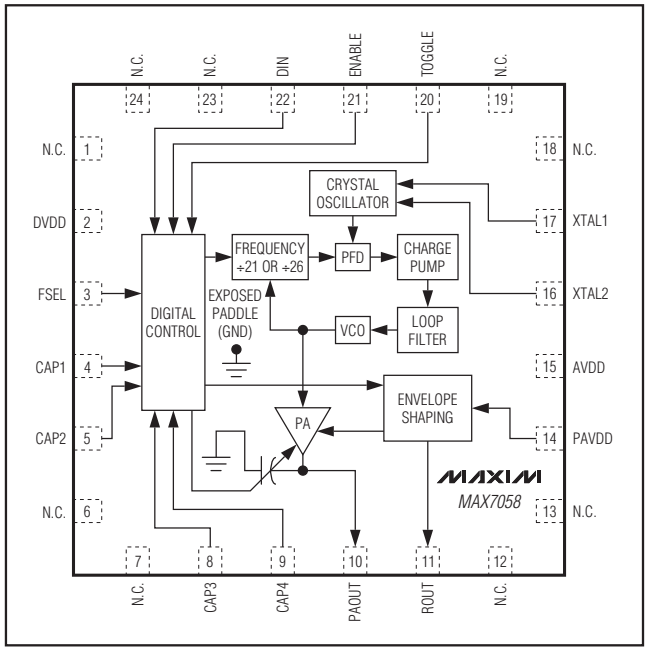
Pin Configuration



TQFN

*EP = EXPOSED PADDLE.

Functional Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

315MHz/390MHz Dual-Frequency ASK Transmitter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, AVDD, DVDD, PAVDD to GND (Exposed Paddle) .....-0.3V to +4V
All Other Pins .....Exposed Paddle - 0.3V to (VDD + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 20.8mW/°C above +70°C) 1666.7mW

Operating Temperature.....-40°C to +125°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Operating Circuit*, 50Ω system impedance, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 315MHz or 390MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C, and guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	PAVDD, AVDD, and DVDD connected to power supply, V_{DD}		2.1	2.7	3.6	V
Supply Current	I_{DD}	PA off, V_{DIN} at 0% duty cycle	f_{RF} = 315MHz		3.4	5.4	mA
			f_{RF} = 390MHz		3.8	6.3	
		V_{DIN} at 50%, duty cycle (Notes 1, 2, 3)	f_{RF} = 315MHz		8.0	13.7	
			f_{RF} = 390MHz		8.3	14.2	
		V_{DIN} at 100%, duty cycle (Note 1)	f_{RF} = 315MHz		12.6	21.9	
			f_{RF} = 390MHz		12.9	22.1	
Standby Current	I_{STDBY}	$V_{ENABLE} < V_{IL}$	T_A = +25°C		0.8		µA
		(Note 3)	T_A < +85°C		1.0	4.0	
			T_A < +125°C		6.2	16.1	
DIGITAL I/O							
Input High Threshold	V_{IH}			0.9 x DV_{DD}			V
Input Low Threshold	V_{IL}					0.1 x DV_{DD}	V
Pulldown Sink Current					13		µA

AC ELECTRICAL CHARACTERISTICS

(*Typical Operating Circuit*, 50Ω system impedance, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 315MHz or 390MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C, and guaranteed by design and characterization over temperature, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Frequency Range				300	315/390	450	MHz
Power-On Time	t_{ON}	ENABLE transition low-to-high, frequency settled to within 50kHz of the desired carrier			110		µs
		ENABLE transition low-to-high, frequency settled to within 5kHz of the desired carrier			250		
Maximum Data Rate		Manchester encoded			50		kbps
		Nonreturn to zero (NRZ)			100		
Frequency Switching Time		Time from low-to-high or high-to-low transition of FSEL to frequency settled to within 5kHz of the desired carrier			30		µs
PHASE-LOCKED LOOP (PLL)							
VCO Gain	K_{VCO}				320		MHz/V
PLL Phase Noise		f_{RF} = 315MHz	10kHz offset		-87		dBc/Hz
			1MHz offset		-98		
		f_{RF} = 390MHz	10kHz offset		-84		
			1MHz offset		-98		
Loop Bandwidth					600		kHz
Reference Frequency Input Level					500		mV_{P-P}
Frequency-Divider Range				21		26	
CRYSTAL OSCILLATOR							
Crystal Frequency	f_{XTAL}				15		MHz
Frequency Pulling by V_{DD}					4		ppm/V
Crystal Load Capacitance		(Note 4)			10		pF

315MHz/390MHz Dual-Frequency ASK Transmitter

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, 50Ω system impedance, AVDD = DVDD = PAVDD = +2.1V to +3.6V, f_{RF} = 315MHz or 390MHz, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at AVDD = DVDD = PAVDD = +2.7V, T_A = +25°C, unless otherwise noted. All min and max values are 100% tested at T_A = +125°C, and guaranteed by design and characterization over temperature, unless otherwise noted.)

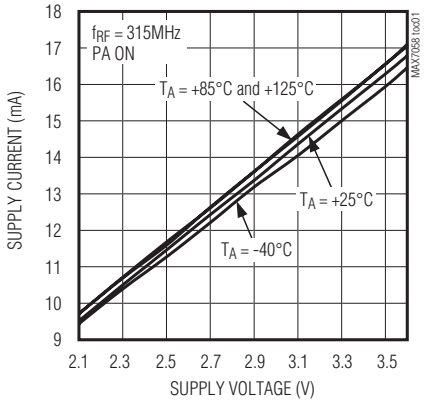
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER AMPLIFIER							
Output Power (Note 1)	P_{OUT}	T_A = +25°C (Note 3)		4.2	10	15.5	dBm
		T_A = +125°C, PAVDD = AVDD = DVDD = +2.1V		3.0	5.9		
		T_A = -40°C, PAVDD = AVDD = DVDD = +3.6V (Note 3)			13.3	16.4	
Modulation Depth					80		dB
Maximum Carrier Harmonics		With output matching network	f_{RF} = 315MHz		-28		dBc
			f_{RF} = 390MHz		-32		
Reference Spur					-48		dBc

Note 1: Supply current and output power are greatly dependent on board layout and PAOUT match.
Note 2: 50% duty cycle at 10kHz ASK data (Manchester coded).
Note 3: Guaranteed by design and characterization, not production tested.
Note 4: Dependent on PCB trace capacitance.

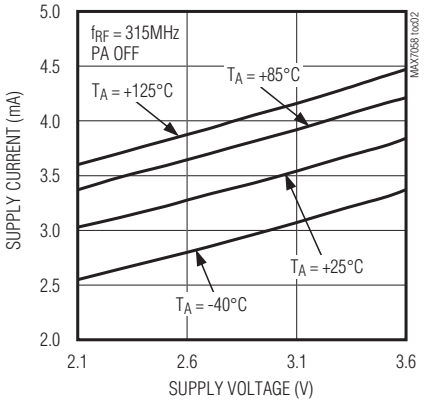
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

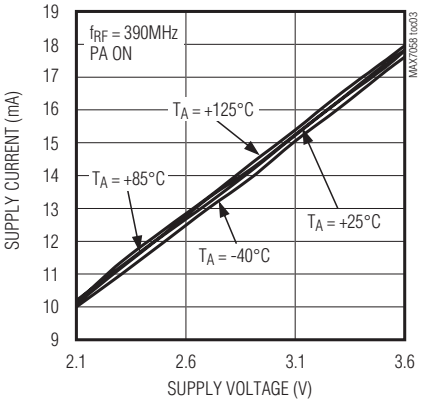
SUPPLY CURRENT vs. SUPPLY VOLTAGE



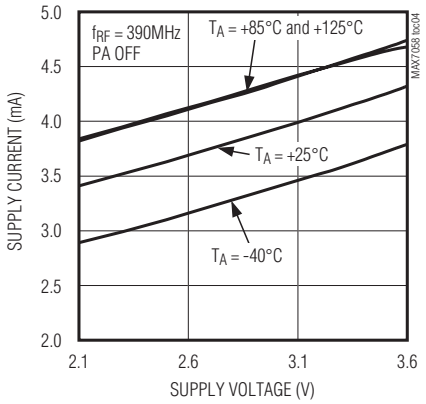
SUPPLY CURRENT vs. SUPPLY VOLTAGE



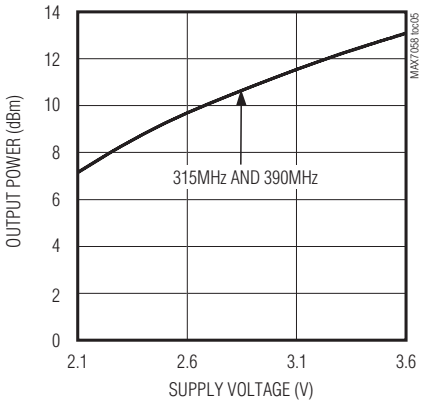
SUPPLY CURRENT vs. SUPPLY VOLTAGE



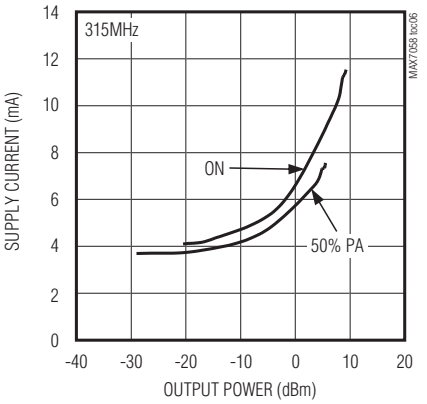
SUPPLY CURRENT vs. SUPPLY VOLTAGE



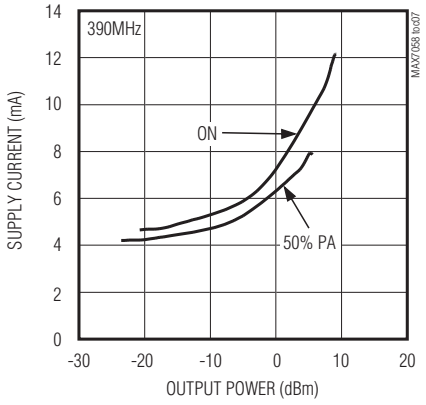
OUTPUT POWER vs. SUPPLY VOLTAGE



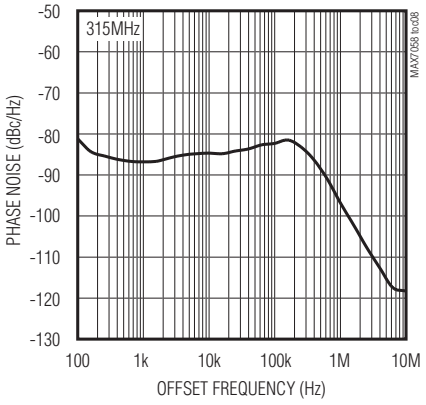
SUPPLY CURRENT vs. OUTPUT POWER



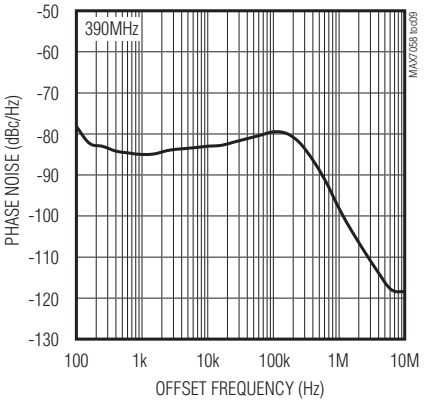
SUPPLY CURRENT vs. OUTPUT POWER



PHASE NOISE vs. OFFSET FREQUENCY



PHASE NOISE vs. OFFSET FREQUENCY

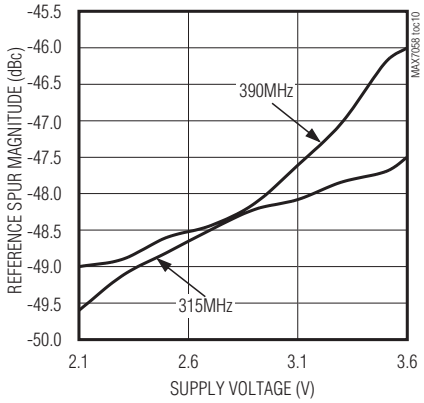


315MHz/390MHz Dual-Frequency ASK Transmitter

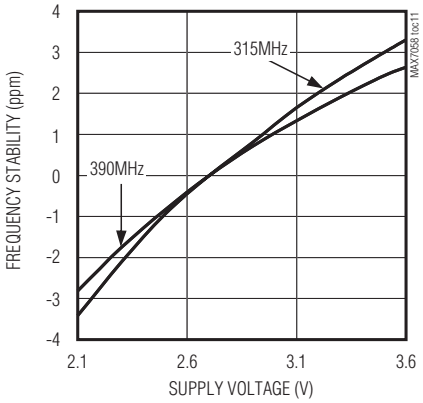
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

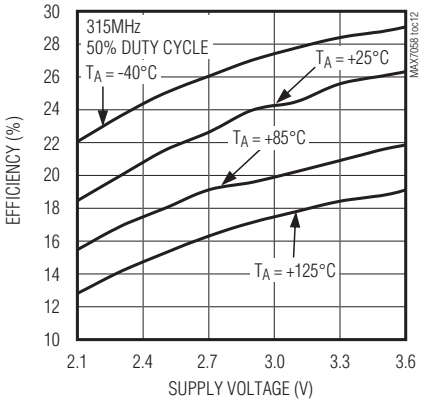
REFERENCE SPUR MAGNITUDE vs. SUPPLY VOLTAGE



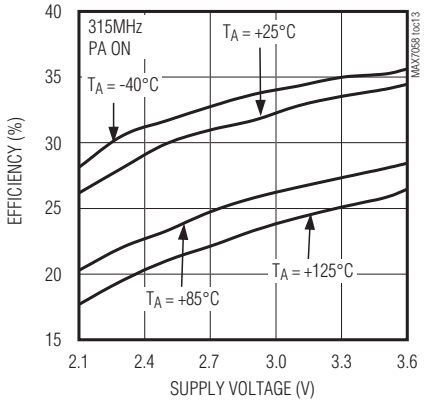
FREQUENCY STABILITY vs. SUPPLY VOLTAGE



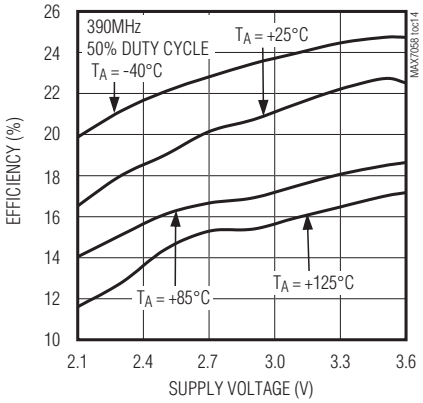
EFFICIENCY vs. SUPPLY VOLTAGE



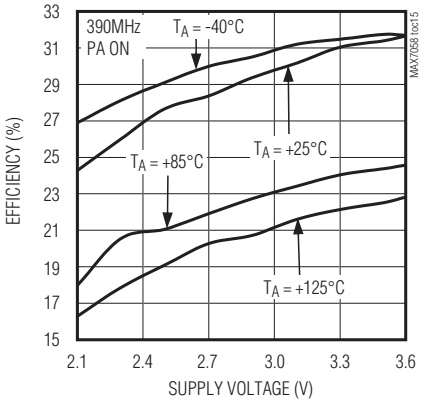
EFFICIENCY vs. SUPPLY VOLTAGE



EFFICIENCY vs. SUPPLY VOLTAGE



EFFICIENCY vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 6, 7, 12, 13, 18, 19, 24	N.C.	No Connection. Internally not connected.
2	DVDD	Digital Positive Supply Voltage. Bypass to GND with 0.1µF and 0.01µF capacitors placed as close to the pin as possible.
3	FSEL	Frequency Select. Internally pulled down to GND when the part is not in standby mode. Set FSEL = 0/TOGGLE = 0 to select continuous 390MHz, and FSEL = 1/TOGGLE = 0 to select continuous 315MHz. See Table 1 for detailed mode description.
4	CAP1	Output Capacitance Adjustment 1. Logic pin to control the capacitance on PAOUT (see Table 2). Set CAP1 = 1 to add 0.5pF shunt capacitance at PAOUT when at 315MHz. Internally pulled down to GND when the part is not in standby mode.
5	CAP2	Output Capacitance Adjustment 2. Logic pin to control the capacitance on PAOUT (see Table 2). Set CAP2 = 1 to add 1pF shunt capacitance at PAOUT when at 315MHz. Internally pulled down to GND when the part is not in standby mode.
8	CAP3	Output Capacitance Adjustment 3. Logic pin to control the capacitance on PAOUT (see Table 2). Set CAP3 = 1 to add 2pF shunt capacitance at PAOUT when at 315MHz. Internally pulled down to GND when the part is not in standby mode.
9	CAP4	Output Capacitance Adjustment 4. Logic pin to control the capacitance on PAOUT (see Table 2). Set CAP4 = 1 to add 4pF shunt capacitance at PAOUT when at 315MHz. Internally pulled down to GND when the part is not in standby mode.
10	PAOUT	Power Amplifier Output. Requires a pullup inductor to the supply voltage or ROUT. The pullup inductor can be part of the output-matching network.
11	ROUT	Envelope-Shaping Output. ROUT controls the power amplifier envelope's rise and fall times. Connect ROUT to PA pullup inductor or optional power-adjust resistor. Bypass the inductor to GND as close to the inductor as possible with 680pF and 220pF capacitors.
14	PAVDD	Power Amplifier Supply Voltage. Bypass to GND with 0.01µF and 220pF capacitors placed as close to the pin as possible.
15	AVDD	Analog Positive Supply Voltage. Bypass AVDD to GND with 0.1µF and 0.01µF capacitors placed as close to the pin as possible.
16	XTAL2	Crystal Input 2. XTAL2 can be driven from an AC-coupled external reference.
17	XTAL1	Crystal Input 1. Bypass to GND if XTAL2 is driven from an AC-coupled external reference.
20	TOGGLE	Toggle Pin. Set TOGGLE = 1 to enable toggle operation (see the *Detailed Description* section and Table 1 for operating mode). Internally pulled down to GND when the part is not in standby mode.
21	ENABLE	Enable Pin. Drive high for normal operation, and drive low or leave unconnected to put the device in standby mode. Internally pulled down to GND.
22	DIN	ASK Data Input. Internally pulled down to GND. Auto power-up occurs upon activity (see the *Detailed Description* section.)
23	N.C.	No connection. Must remain unconnected.
—	EP (GND)	Exposed Paddle. Internally connected to ground (the only ground for the MAX7058.) Requires low-inductance path (e.g., one or more vias) to solid ground plane. Solder evenly to the board's ground plane for proper operation.

315MHz/390MHz Dual-Frequency ASK Transmitter

Detailed Description

The MAX7058 alternately transmits OOK/ASK data at 315MHz or 390MHz using a single crystal. The device has integrated tuning capacitors at the output of the power amplifier to ensure high efficiency at each frequency.

The crystal-based architecture of the MAX7058 eliminates many of the common problems with surface acoustic wave (SAW) transmitters, by providing greater modulation depth, faster frequency settling, tighter transmit frequency tolerance, and reduced temperature dependence. In particular, the tighter transmit frequency tolerance means that a super-heterodyne receiver with a narrower IF bandwidth (therefore lower noise bandwidth) can be used. The payoff is improved overall receiver performance when using a super-heterodyne receiver such as the MAX1471, MAX1473, MAX7033, MAX7034, or MAX7042.

Dual Frequency

The MAX7058 is a crystal-referenced PLL VHF/UHF transmitter that transmits OOK/ASK data at 315MHz or 390MHz. Two fixed synthesizer-divide ratios of 21 and 26 can be selected, and a 15MHz crystal is used as the reference for 315MHz/390MHz operation. The FSEL pin is used to select the divide ratio. The MAX7058 can operate over a 300MHz to 450MHz range by using different crystal frequencies. The two operating frequencies are always related by a 26:21 ratio.

An internal variable shunt capacitor is connected at the PA output. This capacitor is controlled by four external logic bits (CAP1–CAP4) to maintain highly efficient transmission at either 315MHz or 390MHz. This means that it is possible to change the frequency and retune the antenna to the new frequency in a very short time. The combination of rapid-antenna tuning ability with rapid-synthesizer tuning makes the MAX7058 a true frequency-agile transmitter. The tuning capacitor has a resolution of 0.5pF. When the MAX7058 operates at 315MHz, the capacitance added at PAOUT corresponds to the setting at CAP1–CAP4, as seen in Table 2. When the MAX7058 operates at 390MHz, the MAX7058 does not add any internal shunt capacitance at PAOUT.

The MAX7058 supports ASK data rates up to 100kbps NRZ and features adjustable output power through an external resistor to more than +10dBm into a 50Ω load.

Power-Up and Standby Modes

The MAX7058 can be placed in either an enabled state (all circuit blocks necessary for transmission powered up) or a disabled state (low-current standby). The state selection can be controlled either by ENABLE (ENABLE method) or by activity on DIN (auto-power-up method). In either method, the MAX7058 can begin transmission within 250µs after being enabled. Either method can be used with any TOGGLE/FSEL operating mode.

In the ENABLE method, setting ENABLE to a logic-high state enables the MAX7058 and setting it to a logic-low state disables the MAX7058. To avoid conflict with the auto-power-up method, DIN must be set to a logic-low state before ENABLE is set to a logic-low state, and remains low until after ENABLE is set to a logic-high state.

In the auto-power-up method, ENABLE can be hardwired to a logic-low state and a rising edge on DIN will enable the MAX7058. The MAX7058 will remain enabled until DIN is placed in a steady logic-low state for 2^{22} cycles of the reference clock (279.62ms with a 15MHz crystal), at which time the MAX7058 will be disabled.

When the MAX7058 is enabled, the active pulldowns at CAP1–CAP4, FSEL, and TOGGLE will be turned on. When the MAX7058 is disabled, these active pulldowns will be turned off. The active pulldowns at ENABLE and DIN are always turned on.

Operating Mode

TOGGLE and FSEL are two pins available for controlling the state of the toggle mode and the operating frequency. The following truth table defines the pin logic for the four possible operating states.

Table 1. Toggle Pin Operation for MAX7058

TOGGLE PIN	FSEL PIN	OPERATING STATE
0	0	Continuous fixed-frequency operation at 390MHz
0	1	Continuous fixed-frequency operation at 315MHz
1	0	Five packets toggle operation between 315MHz and 390MHz
1	1	100 packets toggle operation between 315MHz and 390MHz

The internal variable shunt capacitor control pins (CAP1–CAP4) are used whenever the frequency setting is 315MHz, in either continuous (TOGGLE = 0, FSEL = 1) or toggle (TOGGLE = 1) mode.

Toggle Definition

With TOGGLE/FSEL set to state 10, the MAX7058 is in 5-packet toggle mode; with TOGGLE/FSEL set to state 11, the MAX7058 is in 100-packet toggle mode. Upon power-up, the MAX7058 begins transmission at 315MHz within 250µs. Packet termination is defined as the time duration of greater than 2^{18} crystal oscillator reference clock cycles (17.49ms) with DIN continuously at logic 0. The frequency of operation toggles every five or 100 packets based on the logic level of FSEL.

Power Amplifier (PA)

The power amplifier (PA) of the MAX7058 is a high-efficiency, open-drain, switching-mode amplifier. In a switching-mode amplifier, the gate of the final-stage FET is driven with a very sharp 25% duty-cycle square wave at the transmit frequency. This square wave is derived from the synthesizer circuit. When the matching network is tuned correctly, the output FET resonates the attached tank circuit with a minimum amount of power dissipated in the FET. With a proper output-matching network, the PA can drive a wide range of antenna impedances, which include a small-loop PCB trace and a 50Ω antenna. The output-matching network suppresses the carrier harmonics and transforms the antenna impedance to optimal impedance at PAOUT, which is from 125Ω to 250Ω.

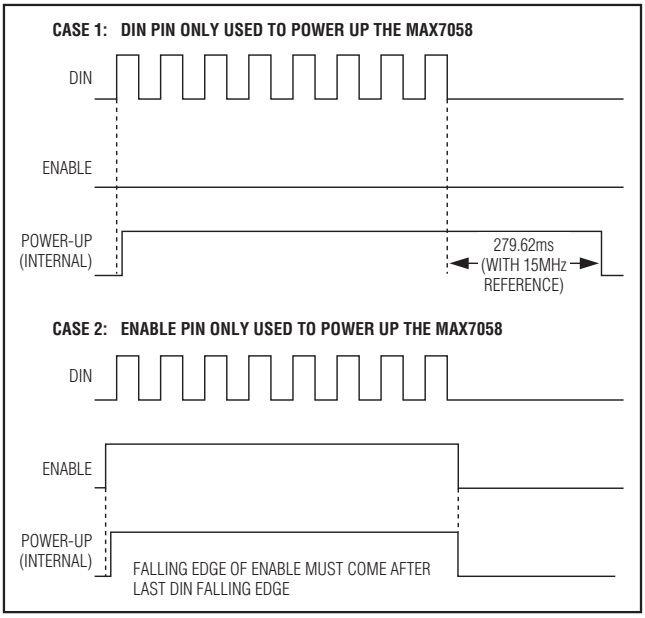


Figure 1. Power-Up Waveform with DIN/ENABLE for MAX7058

When the output-matching network is properly tuned, the PA transmits +10dBm (typ), with a high overall efficiency. The efficiency of the PA itself is more than 40%. The output power can be adjusted by changing the impedance seen by the PA or by adjusting the value of an external resistor at PAOUT.

Envelope Shaping

The MAX7058 features an internal envelope-shaping resistor, which connects between PAVDD and ROUT. When connected to the PA pullup inductor, the envelope-shaping resistor slows the turn-on/turn-off time of the PA and results in a smaller spectral width of the modulated PA output signal.

Variable Capacitor

The MAX7058 has a set of selectable internal shunt capacitors that can be switched in and out to present different capacitor values at the PA output. The capacitors are connected from the PA output to ground. This allows changing the tuning network, along with the synthesizer-divide ratio each time the transmitted frequency changes, making it possible to maintain maximum transmitter power while moving rapidly from one frequency to another.

315MHz/390MHz Dual-Frequency ASK Transmitter

When the particular capacitance control input pin is high, then the corresponding amount of capacitance is added at PAOUT; this capacitance tuning works only at 315MHz. The 16 capacitor values are selected by setting CAP1–CAP4; the capacitance resolution is 0.5pF. The total capacitance varies from 0 to 7.5pF. For example, if CAP1 and CAP3 are high and CAP4 and CAP2 are low when operating at 315MHz, then this circuit will add 2.5pF at PAOUT.

Table 2. Variable Capacitor Values and Control Input Pins

CAPACITOR CONTROL PIN STATE (CAP4–CAP1)	ADDED SHUNT CAPACITANCE IN pF	
	315MHz (÷21)	390MHz (÷26)
0000	0	0
0001	0.5	
0010	1.0	
0011	1.5	
0100	2.0	
0101	2.5	
0110	3.0	
0111	3.5	
1000	4.0	
1001	4.5	
1010	5.0	
1011	5.5	
1100	6.0	
1101	6.5	
1110	7.0	
1111	7.5	

Phase-Locked Loop

The MAX7058 utilizes a fully integrated, programmable PLL for its frequency synthesizer. All PLL components including the loop filter are included on-chip. The divide ratio is set at one of two fixed values: 21 (FSEL is set to high) or 26 (FSEL is set to low).

Crystal (XTAL) Oscillator

The crystal (XTAL) oscillator in the MAX7058 is designed to present a capacitance of approximately 6pF between XTAL1 and XTAL2. In most cases, this corresponds to an 8pF load capacitance applied to the external crystal when typical PCB parasitics are added. The MAX7058 is designed to operate with a typical 10pF load capacitance crystal. **It is very important to use a crystal with a load capacitance equal to the capacitance of the MAX7058 crystal oscillator plus PCB parasitics.** If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. A crystal designed to operate at a higher load capacitance than the value specified for the oscillator will always be pulled higher in frequency. Adding capacitance to increase the load capacitance on the crystal will increase the startup time and may prevent oscillation altogether.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance.

Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_p = \frac{C_m}{2}\left(\frac{1}{C_{case}+C_{load}} - \frac{1}{C_{case}+C_{spec}}\right)\times 10^6$$

where:

f_p is the amount the crystal frequency is pulled in ppm

C_m is the motional capacitance of the crystal

C_{case} is the case capacitance

C_{load} is the actual load capacitance

C_{spec} is the specified load capacitance

When the crystal is loaded as specified (i.e., $C_{load} = C_{spec}$), the frequency pulling equals zero.

Applications Information

Output Matching to 50Ω

When matched to a 50Ω system, the MAX7058's PA is capable of delivering +10dBm of output power at V_{DD} = +2.7V. The output of the PA is an open-drain transistor, which has internal selectable shunt tuning capacitors for impedance matching (see the *Variable Capacitor* section). It is connected to V_{DD} through a pullup inductor for proper biasing. The internal selectable shunt capacitors make it easy for tuning when changing the output frequency. The pullup inductance from the PAOUT to V_{DD} or ROUT serves three main purposes: resonating the capacitive PA output, providing biasing for the PA, and acting as a high-frequency choke to prevent RF energy from coupling into V_{DD}. The pi network between the PA output and the antenna also forms a lowpass filter that provides attenuation for the higher-order harmonics.

Output Matching to PCB Loop Antenna

In many applications, the MAX7058 must be impedance-matched to a small loop antenna. The antenna is usually fabricated out of a copper trace on a PCB in a rectangular, circular, or square pattern. The antenna has impedance that consists of a lossy component and a radiative component. To achieve high radiating efficiency, the radiative component should be as high as possible, while minimizing the lossy component. In addition, the loop antenna has an inherent loop inductance associated with it (assuming the antenna is terminated to ground). In a typical application, the inductance of the loop antenna is approximately 50nH to 100nH. The radiative and lossy impedances may be anywhere from a few tenths of an ohm to 5Ω or 10Ω.

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. At high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are on the order of λ/10 or longer act as antennas, where λ is the wavelength.

Keeping the traces short also reduces parasitic inductance. Generally, one inch of PCB trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance of a passive component. For example, a 0.5in trace connecting to a 100nH inductor adds an extra 10nH of inductance, or 10%.

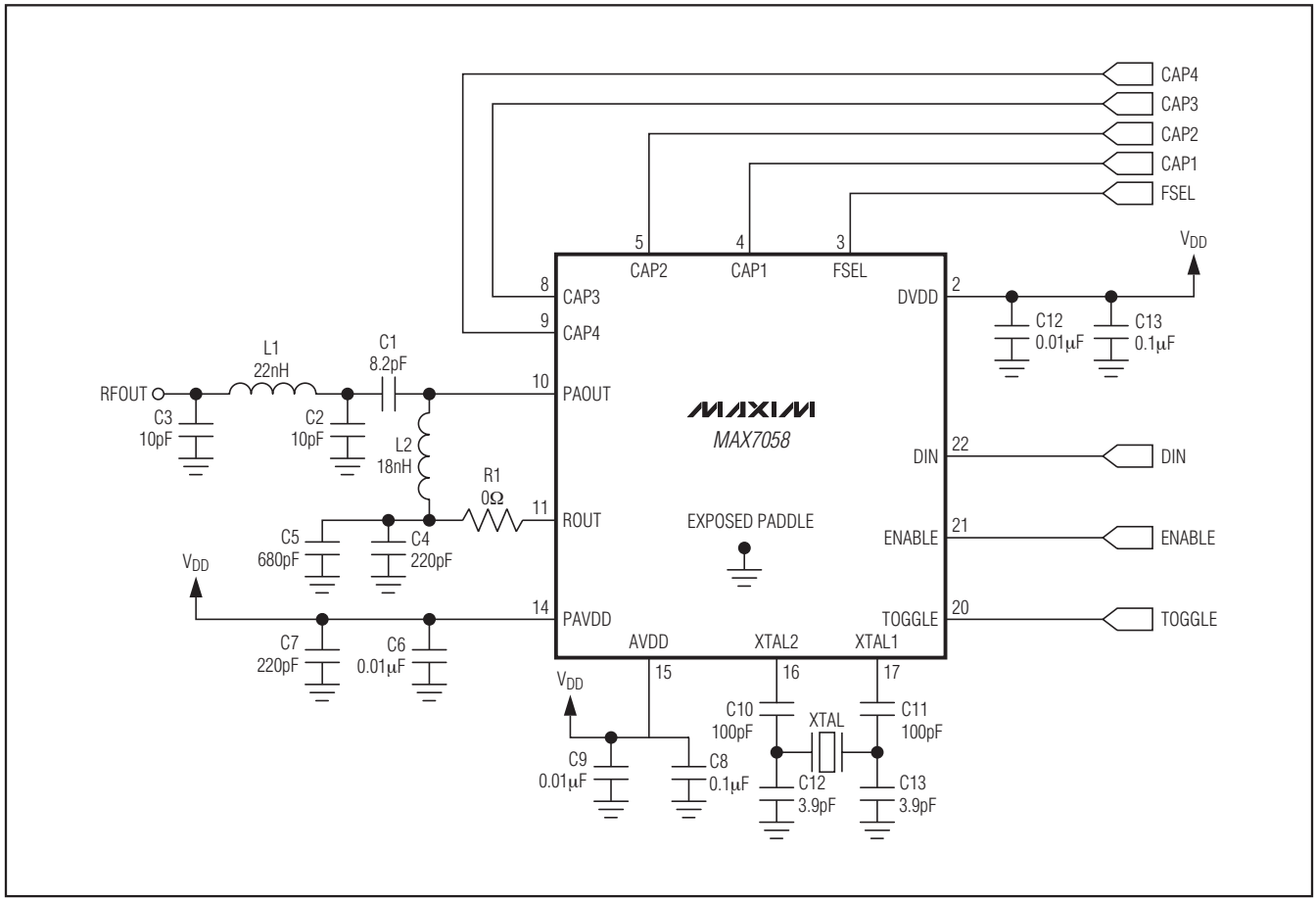
To reduce parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Using a solid ground plane can reduce the parasitic inductance from approximately 20nH/in to 7nH/in. Also, use low-inductance connections to the ground plane and place decoupling capacitors as close as possible to all VDD pins.

Chip Information

PROCESS: CMOS

315MHz/390MHz Dual-Frequency ASK Transmitter

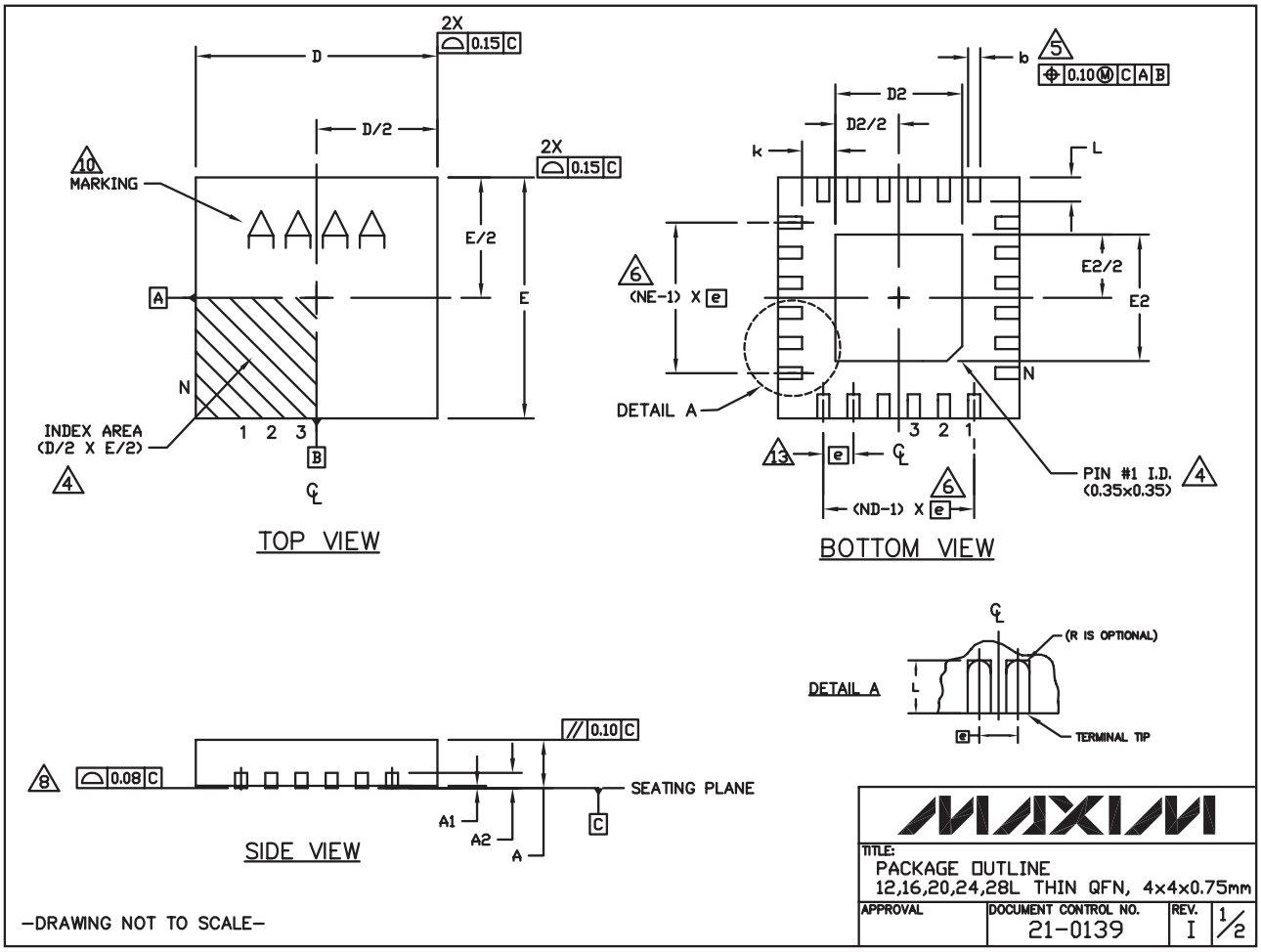
Typical Operating Circuit



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



315MHz/390MHz Dual-Frequency ASK Transmitter

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	12			16			20			24			28			
ND	3			4			5			6			7			
NE	3			4			5			6			7			
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE 12,16,20,24,28L THIN QFN, 4x4x0.75mm

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