Serial 12-Bit, 2.2Msps Sampling ADC with Shutdown

FEATURES

- **Sample Rate: 2.2Msps**
- **72dB S/(N + D) and –89dB THD at Nyquist**
- **Power Dissipation: 90mW (Typ)**
- **80MHz Full Power Bandwidth Sampling**
- No Missing Codes over Temperature
- Available in 16-Pin Narrow SSOP Package
- Single Supply 5V or ±5V Operation
- Nap Mode with Instant Wake-Up: 15mW
- Sleep Mode: 10µW
- True Differential Inputs Reject Common Mode Noise
- Input Range (1mV/LSB): 0V to 4.096V or ±2.048V
- Internal Reference Can Be Overdriven Externally
- 3-Wire Interface to DSPs and Processors (SPI and MICROWIRE™ Compatible)

APPLICATIONS

- Telecommunications
- High Speed Data and Signal Acquisition
- Digitally Multiplexed Data Acquisition Systems
- Digital Radio Receivers
- Spectrum Analysis
- Low Power and Battery-Operated Systems
- Handheld or Portable Instruments
- Imaging Systems

DESCRIPTION

The LTC®1402 is a 12-bit, 2.2Msps sampling A/D converter. This high performance device includes a high dynamic range sample-and-hold and a precision reference. It operates from a single 5V supply or dual ±5V supplies and draws only 90mW from 5V.

The versatile differential input offers a unipolar range of 4.096V and a bipolar range of ±2.048V for dual supply systems where high performance op amps perform best, eliminating the need for special translation circuitry.

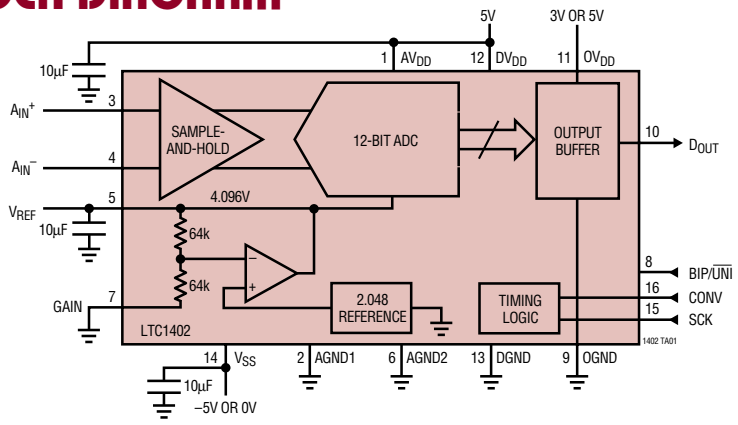
The high common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

Outstanding AC performance includes 72dB S/(N + D) and –93dB SFDR at the Nyquist input frequency of 1.1MHz with dual ±5V supplies and –84dB SFDR with a single 5V supply.

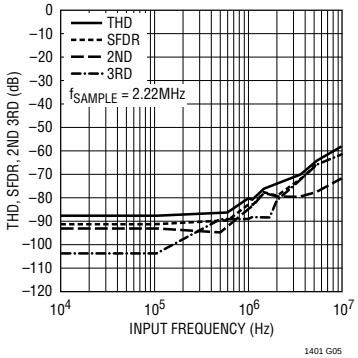
The LTC1402 has two power saving modes: Nap and Sleep. Nap mode consumes only 15mW of power and can wake up and convert immediately. In Sleep mode, it typically consumes 10µW of power. Upon power-up from Sleep mode, a reference ready (REFRDY) signal is available in the serial data word to indicate that the reference has settled and the chip is ready to convert.

The 3-wire serial port allows compact and efficient data transfer to a wide range of microprocessors, microcontrollers and DSPs. A digital output driver power supply pin allows direct connection to 3V or lower logic.

BLOCK DIAGRAM



5 Harmonic THD, 2nd, 3rd and SFDR vs Input Frequency (Unipolar)

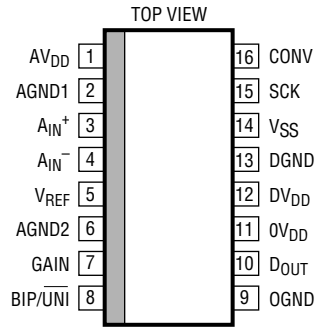


ABSOLUTE MAXIMUM RATINGS

$AV_{DD} = DV_{DD} = OV_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage
(Note 4) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Output Voltage ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 250mW
Operation Temperature Range
LTC1402C ..... 0°C to 70°C
LTC1402I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1402CGN LTC1402IGN
GN PART MARKING
1402 1402I

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With internal reference (Note 5).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 6)	●		±0.35	±1	LSB
Differential Linearity	(Note 6)	●		±0.25	±1	LSB
Offset Error	(Note 6)	●		±2	±10	LSB
Full-Scale Error	(Note 6)	●		±10	±15	LSB
Full-Scale Tempco	Internal Reference (Note 6) External Reference			±15 ±1		ppm/°C ppm/°C

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Differential Input Range (Notes 3, 11)	Bipolar Mode with BIP/$\overline{UNI}$ High 4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V	●		±2.048		V
		Unipolar Mode with BIP/$\overline{UNI}$ Low 4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ 0V	●		0 to 4.096		V
V_{CM}	Analog Common Mode + Differential Input Range (Note 12)	Dual ±5V Supply Single 5V Supply			–2.5 to 5 0 to 5		V V
I_{IN}	Analog Input Leakage Current		●			1	µA
C_{IN}	Analog Input Capacitance				10		pF
t_{ACQ}	Sample-and-Hold Acquisition Time	(Note 9)	●			57	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				2.6		ns
t_{JITTER}	Sample-and-Hold Aperture Delay Time Jitter				1		ps
CMRR	Analog Input Common Mode Rejection Ratio	f_{IN} = 1MHz, V_{IN} = 2V to –2V f_{IN} = 100MHz, V_{IN} = 2V to –2V			–62 –24		dB dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Bipolar mode with ± 5V supplies and unipolar mode with 5V supply. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal 1.1MHz Input Signal	 ●	 69	72.5 72.0		dB dB
THD	Total Harmonic Distortion	100kHz First 5 Harmonics, Bipolar Mode 1.1MHz First 5 Harmonics, Bipolar Mode 100kHz First 5 Harmonics, Unipolar Mode 1.1MHz First 5 Harmonics, Unipolar Mode	 ● 	 	–89 –89 –87 –82	 –74.5 	dB dB dB dB
SFDR	Spurious Free Dynamic Range	100kHz Input Signal, Bipolar Mode 1.1MHz Input Signal, Bipolar Mode 100kHz Input Signal, Unipolar Mode 1.1MHz Input Signal, Unipolar Mode	 	 	–93 –93 –93 –84	 	dB dB dB dB
IMD	Intermodulation Distortion	±1V 1.25MHz into A_{IN}^+, 1.2MHz into A_{IN}^- Bipolar Mode 1.5V to 3.5V 1.25MHz into A_{IN}^+, 1.2MHz into A_{IN}^- Unipolar Mode	 	 	–84 –84	 	dB dB
	Code-to-Code Transition Noise	V_{REF} = 4.096V, 1LSB = 1mV			0.18		LSB_{RMS}
	Full Power Bandwidth	$V_{IN} = 4V_{P-P}$, $D_{OUT} = 2828LSB_{P-P}$ (Note 18)			82		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 68dB Bipolar Mode Unipolar Mode	 	 	5.0 3.5	 	MHz MHz

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0			4.096		V
V_{REF} Output Tempco				15		ppm/°C
V_{REF} Line Regulation	AV_{DD} = 4.75V to 5.25V, V_{REF} = 4.096V			1		LSB/V
V_{REF} Output Resistance	Load Current = 0.5mA			2		Ω
V_{REF} Settling Time				2		ms

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	OV_{DD} = 4.75V, I_{OUT} = –10µA OV_{DD} = 4.75V, I_{OUT} = –200µA OV_{DD} = 3V, I_{OUT} = –200µA	 ● ●	 4 2.5	4.7 2.9	 	V V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_{OUT} = 160µA V_{DD} = 4.75V, I_{OUT} = 1.6mA	 ●	 	0.05 0.10	 0.4	V V
I_{OZ}	Hi-Z Output Leakage D_{OUT}	V_{OUT} = 0V to V_{DD}	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D_{OUT}				15		pF
I_{SOURCE}	Output Short-Circuit Source Current	V_{OUT} = 0V, OV_{DD} = 5V V_{OUT} = 0V, OV_{DD} = 3V	 	 	–40 –15	 	mA mA
I_{SINK}	Output Short-Circuit Sink Current	V_{OUT} = OV_{DD} = 5V			40		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage			4.75		5.25	V
V_{SS}	Negative Supply Voltage			–5.25		0	V
I_{DD}	Positive Supply Current	Active Mode	●		18	30	mA
		Nap Mode	●		3	5	mA
		Sleep Mode			2	10	µA
I_{SS}	Negative Supply Current	Active, Sleep or Nap Modes with SCK Off	●			2	µA
PD	Power Dissipation	Active Mode with SCK in Fixed State (Hi or Lo)			90	150	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency (Conversion Rate)		●	2.2			MHz
$t_{THROUGHPUT}$	Minimum Sampling Period (Conversion + Acquisiton Period)		●			455	ns
t_{SCK}	Minimum Clock Period		●	28		10000	ns
t_{CONV}	Conversion Time	(Note 9)			14		SCK cycles
t_0	14th SCLK↑ to CONV↑ Interval	(Notes 9, 10, 16)	●	57			ns
t_1	Minimum Positive or Negative SCK Pulse Width	(Note 9)	●		3.8	6	ns
t_2	CONV to SCK Setup Time	(Notes 9, 13)	●		7.3	12	ns
t_3	SCK After CONV	(Note 9)	●	0			ns
t_4	Minimum Positive or Negative CONV Pulse Width	(Note 9)	●		3.5	5	ns
t_5	SCK to Sample Mode	(Note 9)	●		9	14	ns
t_6	CONV to Hold Mode	(Notes 9, 14)	●		3.4	5	ns
t_7	Minimum Delay Between Conversions	(Note 9)	●	48			ns
t_8	Minimum Delay from SCK to Valid Bits 0 Through 11	(Notes 9, 15)	●		9	12	ns
t_{8a}	Minimum Delay from SCK to Valid REFREADY	(Notes 9, 15)	●		15	20	ns
t_9	SCK to Hi-Z at D_{OUT}	(Notes 9, 15)	●		11.4	16	ns
t_{10}	Previous D_{OUT} Bit Remains Valid After SCK	(Notes 9, 15)	●	4	7		ns
t_{11}	REFREADY Bit Delay After Sleep-to-Wake Transition	(Notes 9, 17)	●		10		ms
t_{12}	V_{REF} Settling Time After Sleep-to-Wake Transition	(Notes 9, 17)	●		2		ms

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND1 and AGND2 wired together.

Note 3: When these pins are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or greater than V_{DD} without latchup.

Note 4: When these pins are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or greater than V_{DD}. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 2.2MHz, V_{SS} = 0V for unipolar mode specifications and V_{SS} = –5V for bipolar specifications.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended A_{IN}^+ input with A_{IN}^- grounded and using the internal reference in bipolar mode with ±5V supplies.

Note 7: Integral linearity is defined as the deviation of a code from the straight line passing through the actual endpoints of a transfer curve. The deviation is measured from the center of quantization band.

Note 8: Bipolar offset is the offset measured from –0.5LSB when the input flickers between 1000 0000 0000 and 0111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: The analog input range is defined as the voltage difference between A_{IN}^+ and A_{IN}^-. The bipolar ±2.048V input range could be used with a single 5V supply if the absolute voltages of the inputs remain within the single 5V supply voltage.

ELECTRICAL CHARACTERISTICS

Note 12: The absolute voltage at A_{IN}^+ and A_{IN}^- must be within this range.

Note 13: If less than 7.3ns is allowed, the output data will appear one clock cycle later. It is best for CONV to rise half a clock before SCK, when running the clock at rated speed.

Note 14: Not the same as aperture delay. Aperture delay is smaller (2.6ns) because the 0.8ns delay through the sample-and-hold is subtracted from the CONV to Hold mode delay.

Note 15: The rising edge of SCK is guaranteed to catch the data coming out into a storage latch.

Note 16: The time period for acquiring the input signal is started by the 14th rising clock and it is ended by the rising edge of convert.

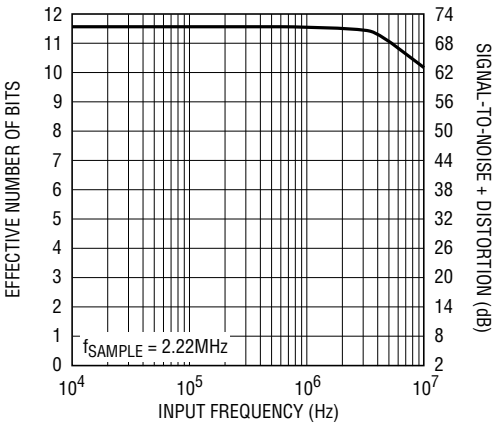
Note 17: The internal reference settles in 2ms after it wakes up from Sleep mode with one or more cycles at SCK and a 10µF capacitive load. The Sleep mode resets the REFREADY bit in the D_{OUT} sequence. The REFREADY bit goes high again 10ms after the V_{REF} has stopped slewing in wake up. This ensures valid REFREADY bit operation even with higher load capacitances at V_{REF}.

Note 18: The full power bandwidth is the frequency where the output code swing drops to 2828LSBs with a $4V_{P-P}$ input sine wave.

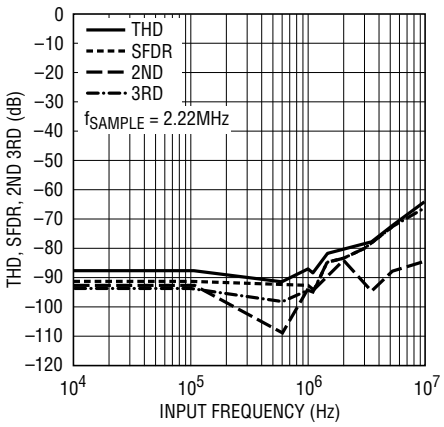
TYPICAL PERFORMANCE CHARACTERISTICS

(Bipolar Mode Plots Run with Dual ±5V Supplies. Unipolar Mode Plots Run with a Single 5V Supply. V_{DD} = 5V, V_{SS} = –5V for Bipolar, V_{DD} = 5V, V_{SS} = 0V for Unipolar), T_A = 25°C.

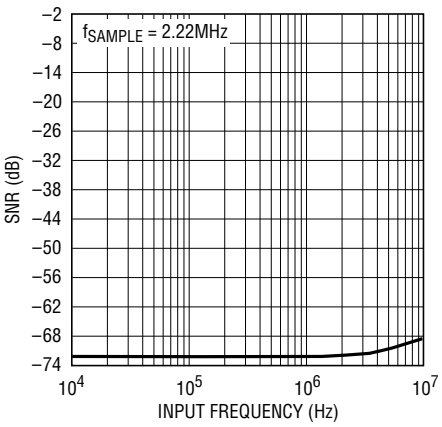
ENOBs and SINAD vs Input Frequency (Bipolar)



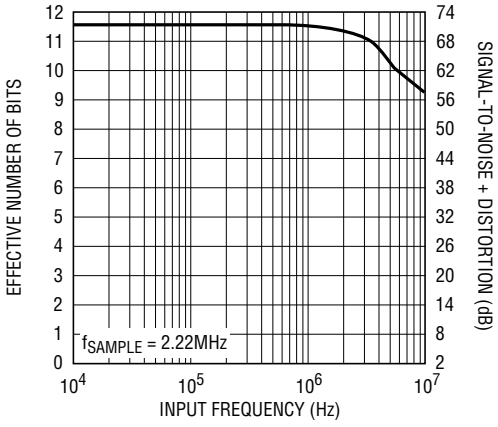
5 Harmonic THD, 2nd, 3rd and SFDR vs Input Frequency (Bipolar)



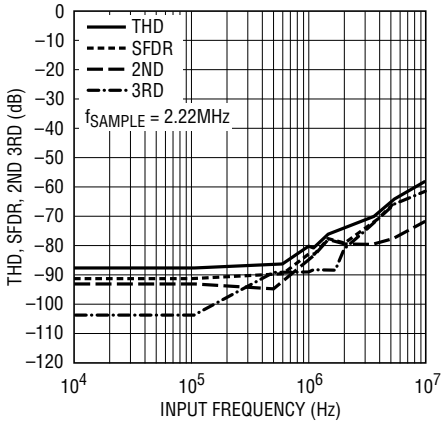
SNR vs Input Frequency (Bipolar)



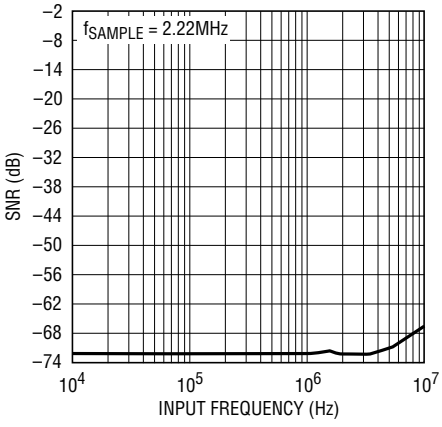
ENOBs and SINAD vs Input Frequency (Unipolar)



5 Harmonic THD, 2nd, 3rd and SFDR vs Input Frequency (Unipolar)



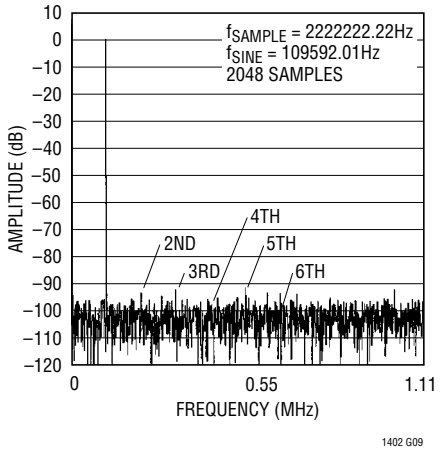
SNR vs Input Frequency (Unipolar)



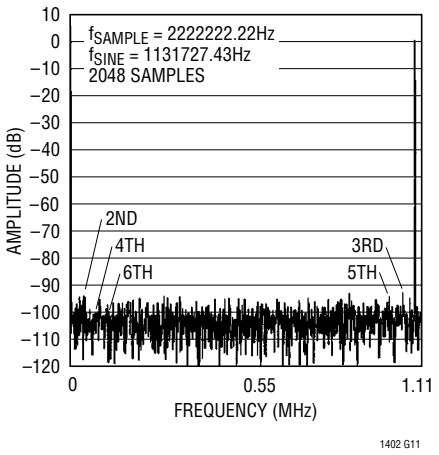
TYPICAL PERFORMANCE CHARACTERISTICS

(Bipolar Mode Plots Run with Dual ±5V Supplies. Unipolar Mode Plots Run with a Single 5V Supply. V_{DD} = 5V, V_{SS} = –5V for Bipolar, V_{DD} = 5V, V_{SS} = 0V for Unipolar), T_A = 25°C.

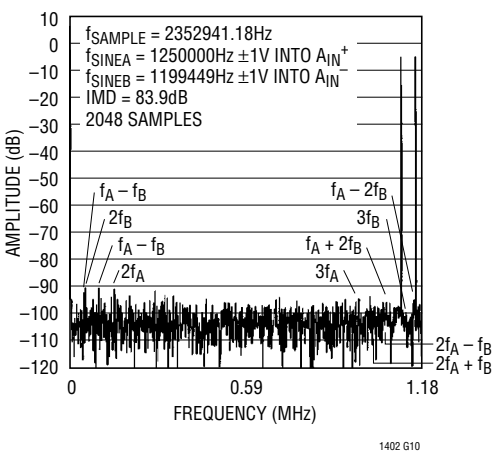
Sine Wave Spectrum Plot (Bipolar) ±5V Supply



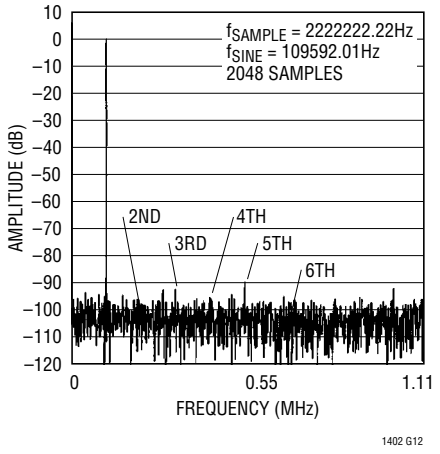
Sine Wave Spectrum Plot (Bipolar) Dual ±5V Supply



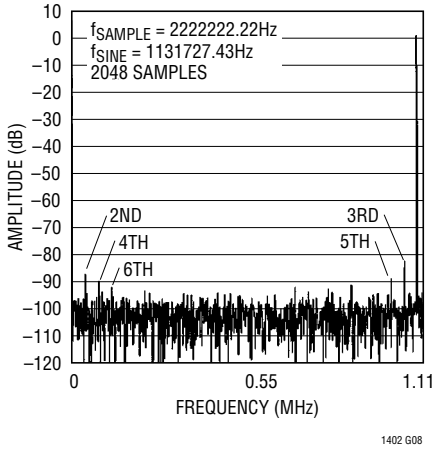
IMD Spectrum Plot (Bipolar)



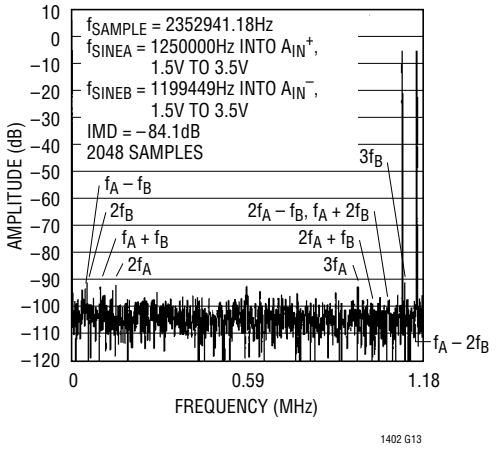
Sine Wave Spectrum Plot (Unipolar) 5V Supply



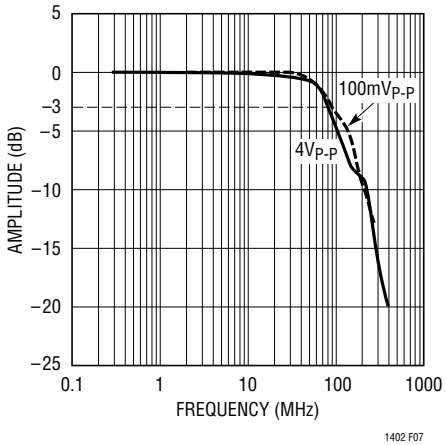
Sine Wave Spectrum Plot (Unipolar) 5V Supply



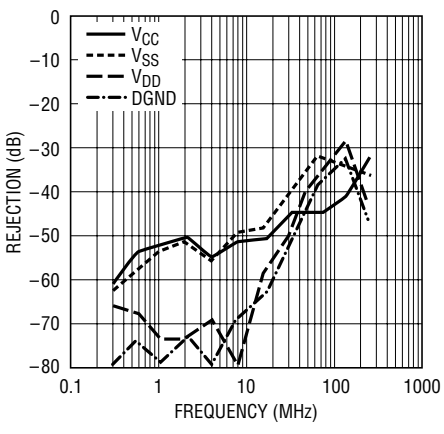
IMD Spectrum Plot (Unipolar)



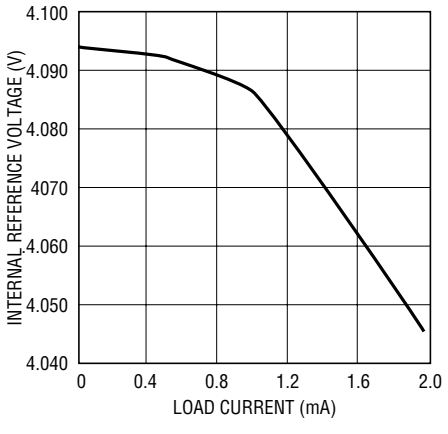
4V_{P-P} Power Bandwidth and 100mV_{P-P} Small-Signal Bandwidth



PSRR vs Frequency



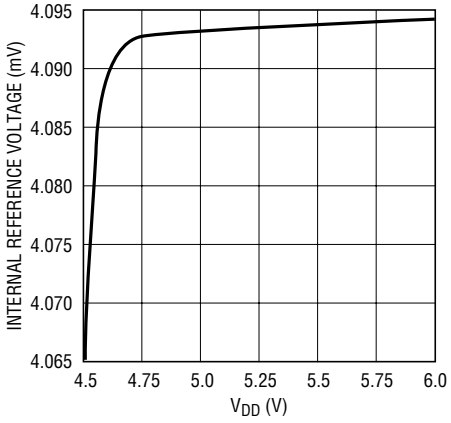
Load Regulation for V_{REF}



TYPICAL PERFORMANCE CHARACTERISTICS

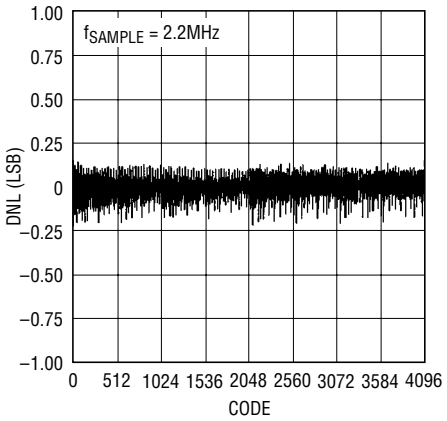
(Bipolar Mode Plots Run with Dual ±5V Supplies. Unipolar Mode Plots Run with a Single 5V Supply. V_{DD} = 5V, V_{SS} = –5V for Bipolar, V_{DD} = 5V, V_{SS} = 0V for Unipolar), T_A = 25°C.

Positive Power Supply Rejection for V_{REF}



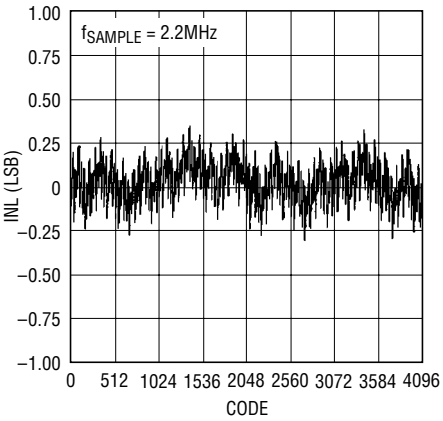
1402 G21

Differential Nonlinearity vs Output Code (Bipolar)



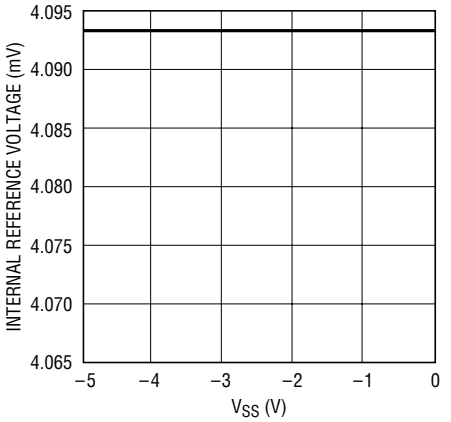
1402 G15

Integral Nonlinearity vs Output Code (Bipolar)



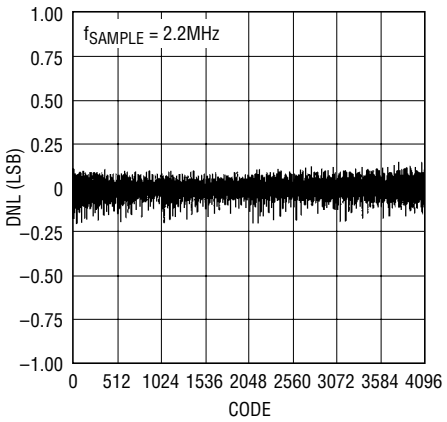
1402 G14

Negative Power Supply Rejection for V_{REF}



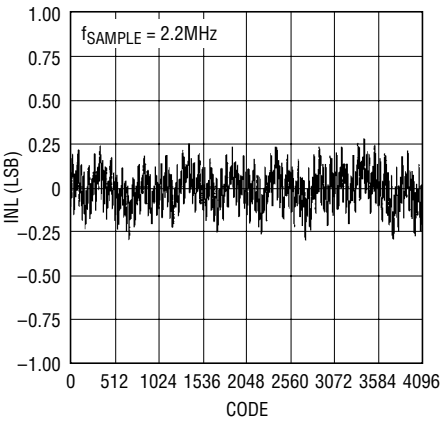
1402 G19

Differential Nonlinearity vs Output Code (Unipolar)



1402 G17

Integral Nonlinearity vs Output Code (Unipolar)



1402 G16

PIN FUNCTIONS

AV_{DD} (Pin 1): 5V Analog Power Supply. Bypass to AGND1 and solid analog ground plane with 10µF ceramic (or 10µF tantalum in parallel with 0.1µF ceramic).

AGND1 (Pin 2): Analog Ground. Tie to solid analog ground plane. The analog ground plane should be solid and have no cuts near the LTC1402.

A_{IN}^+ (Pin 3): Positive Analog Signal Input. 0V to 4.096V in unipolar mode and ±2.048V in bipolar mode when A_{IN}^- is grounded. Both of these ranges operate fully differentially with respect to A_{IN}^-. (Note 3)

A_{IN}^- (Pin 4): Negative Analog Signal Input. Can be grounded or driven differentially with A_{IN}^+. Identical to A_{IN}^+, except that it inverts the input signal. (Note 3)

V_{REF} (Pin 5): 4.096V Reference Voltage Output. Bypass to AGND1 and solid analog ground plane with 10µF ceramic (or 10µF tantalum in parallel with 0.1µF ceramic).

AGND2 (Pin 6): Analog Ground Return for the Reference and Internal CDAC. AGND2 could be overdriven externally above ground. Tie to solid analog ground plane.

PIN FUNCTIONS

GAIN (Pin 7): Tie to AGND2 to set the reference voltage to 4.096V or tie to V_{REF} to set the reference voltage to 2.048V. (Note 4)

BIP/$\overline{UNI}$ (Pin 8): Tie to logic low to set the input range to unipolar mode or tie to logic high to set the input range to bipolar mode. (Note 4)

OGND (Pin 9): Output Ground for the Output Driver. This pin can be tied to the digital ground of the system. All other ground pins should be tied to the analog ground plane.

D_{OUT} (Pin 10): Three-State Data Output. (Note 3) Each output data word represents the analog input at the start of the previous conversion.

OV_{DD} (Pin 11): Output Data Driver Power. Tie to V_{DD} when driving 5V logic. Tie to 3V when driving 3V logic.

DV_{DD} (Pin 12): Digital Power for Internal Logic. Bypass to DGND with 10µF ceramic (or 10µF tantalum in parallel with 0.1µF ceramic).

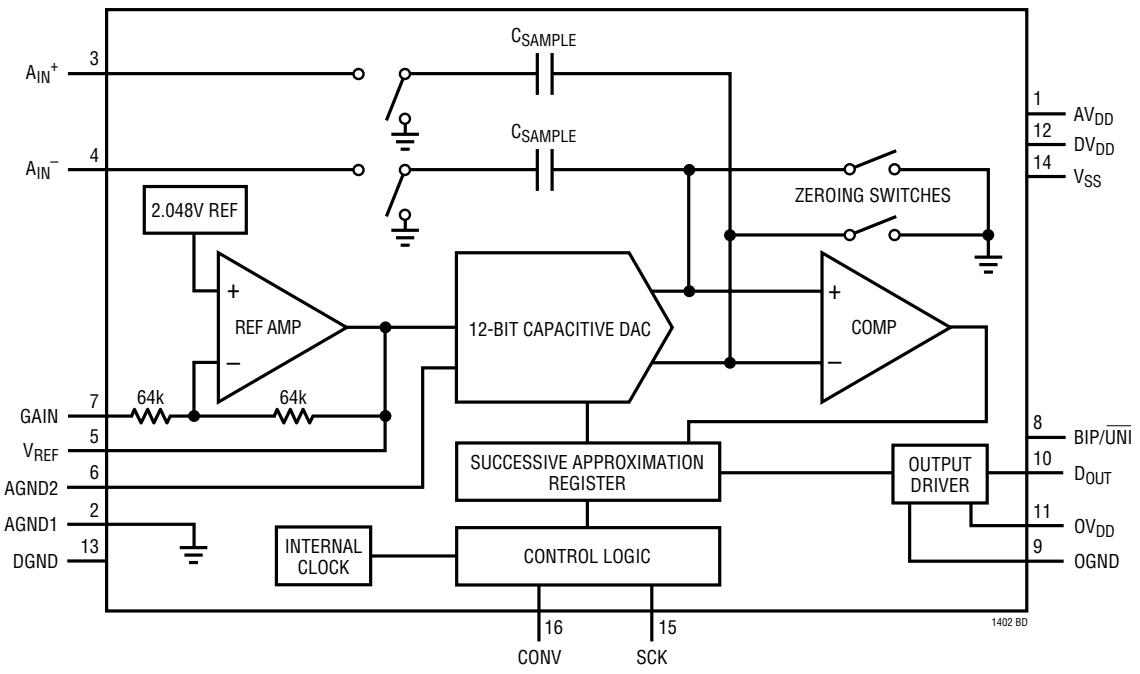
DGND (Pin 13): Digital Ground for Internal Logic. Tie to solid analog ground plane.

V_{SS} (Pin 14): Negative Supply Voltage. Bypass to solid analog ground plane with 10µF ceramic (or 10µF tantalum in parallel with 0.1µF ceramic) or tie directly to the solid analog ground plane for single supply use. Must be set more negative than either A_{IN}^+ or A_{IN}^-. Set to 0V or –5V.

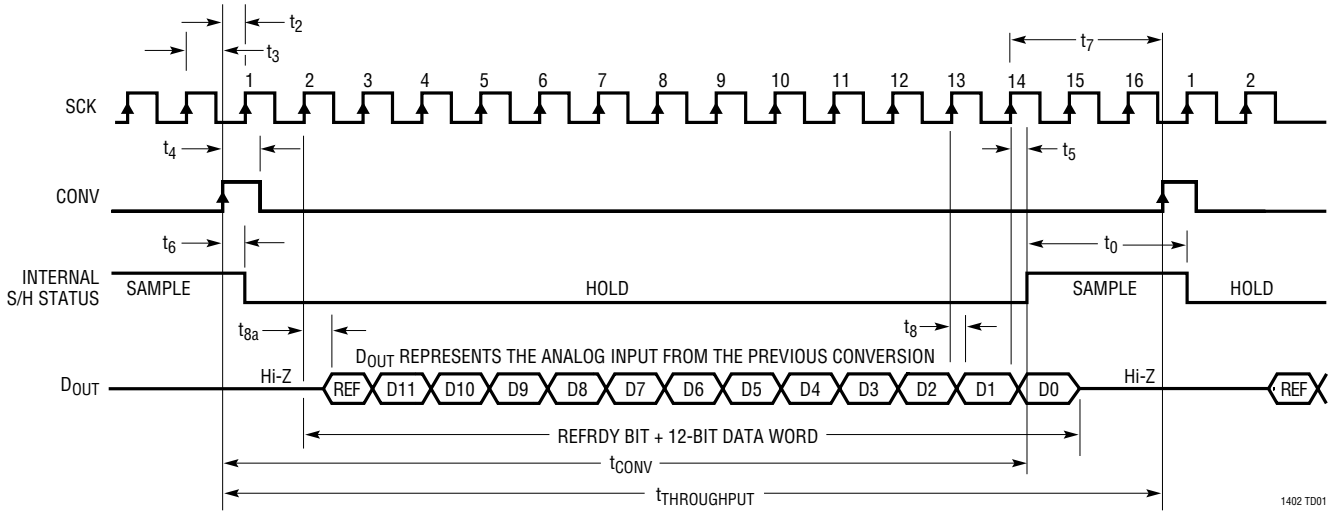
SCK (Pin 15): External Clock. Advances the conversion process and sequences the output data at D_{OUT} on the rising edge. Responds to 5V or 3V CMOS and to TTL levels. (Note 4). One or more pulses wake from Nap or Sleep.

CONV (Pin 16): Holds the input analog signal and starts the conversion on the rising edge. Responds to 5V or 3V CMOS and to TTL levels. (Note 4). Two pulses with SCK in fixed high or fixed low state start Nap Mode. Four pulses with SCK in fixed high or fixed low state start Sleep mode.

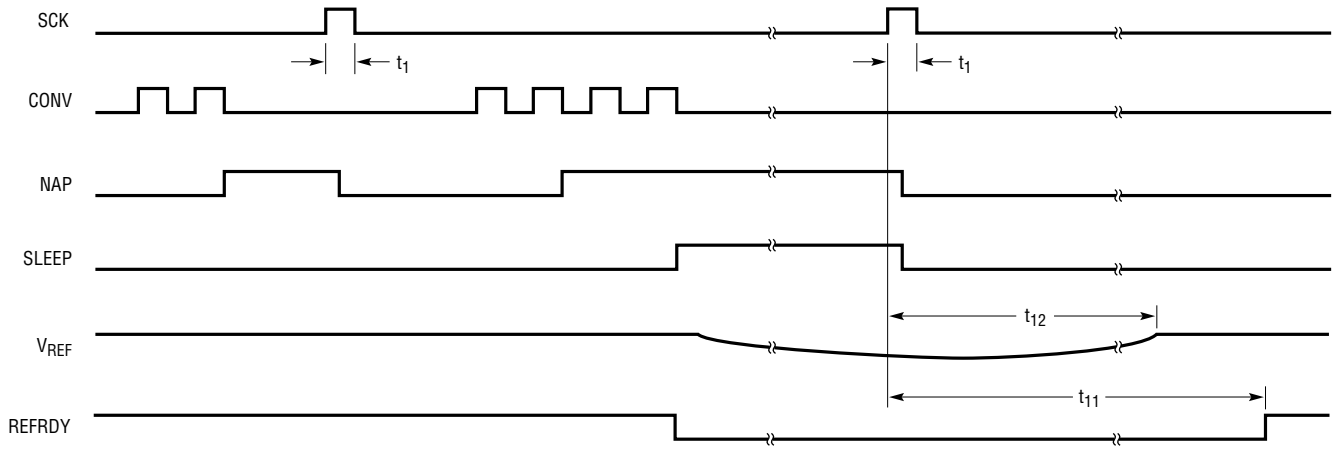
BLOCK DIAGRAM



TIMING DIAGRAMS



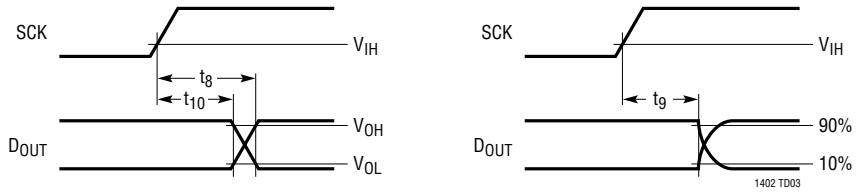
Nap Mode and Sleep Mode Waveforms



NOTE: NAP AND SLEEP ARE INTERNAL SIGNALS. REFRDY APPEARS AS A BIT IN THE D_{OUT} WORD.

1402 TD02

SCK to D_{OUT} Delay



APPLICATIONS INFORMATION

DRIVING THE ANALOG INPUT

The differential analog inputs of the LTC1402 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is grounded). The A_{IN}^+ and A_{IN}^- inputs are sampled at the same instant. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1402 inputs can be driven directly. As source impedance increases, so will acquisition time (see Figure 1). For minimum acquisition time with high source impedance, a buffer amplifier must be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 50ns for full throughput rate).

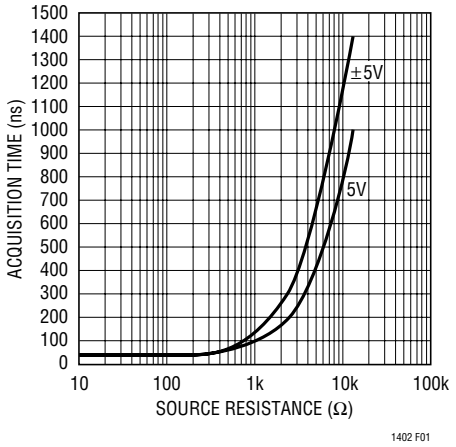


Figure 1. Acquisition Time vs Source Resistance in Bipolar and Unipolar Modes

CHOOSING AN INPUT AMPLIFIER

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 40MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more time for settling can be provided by increasing the time between conversions. The best choice for an op amp to drive the LTC1402 will depend on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most critical, and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1402. More detailed information is available in the Linear Technology Databooks and on the LinearView™ CD-ROM.

LT®1206: 60MHz Current Feedback Amplifier with Shutdown Pin (Amplifier Draws 200μA While in Shutdown). ±5V to ±15V supplies. Distortion is –80dB to 1MHz ($2V_{P-P}$ into 30Ω). Good for AC applications. Dual available with shutdown as LT1207. Output swings to within $2V_{BE}$ of the supply rails.

LT1223: 100MHz Video Current Feedback Amplifier. 6mA supply current. ±5V to ±15V supplies. Low distortion at frequencies above 400kHz. Low noise. Good for AC applications.

LT1227: 140MHz Video Current Feedback Amplifier. 10mA supply current; has shutdown pin (draws 120μA while in shutdown). ±5V to ±15V supplies. Lowest distortion (–92dB) at frequencies above 400kHz. Low noise. Best for AC applications.

LT1229/LT1230: Dual and Quad 100MHz Current Feedback Amplifiers. ±2V to ±15V supplies. Low noise. Good AC specifications, 6mA supply current each amplifier.

LT1360: 50MHz Voltage Feedback Amplifier. 3.8mA supply current. ±5V to ±15V supplies. Good AC and DC specifications. 70ns settling to 0.5LSB.

LT1363: 70MHz, 1000V/μs Op Amps. 6.3mA supply current. Good AC and DC specifications. 60ns settling to 0.5LSB.

LT1364/LT1365: Dual and Quad 70MHz, 1000V/μs Op Amps. 6.3mA supply current per amplifier. 60ns settling to 0.5LSB.

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APPLICATIONS INFORMATION

LT1630: Dual 30MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 500µV offset and 520ns settling to 0.5LSB for a 4V swing. THD and noise are –93dB to 40kHz and below 1LSB to 320kHz (A_V = 1, $2V_{P-P}$ into 1kΩ, V_S = 5V), making the part excellent for AC applications (to 1/3 Nyquist) where rail-to-rail performance is desired. Quad version is available as LT1631.

LT1632: Dual 45MHz Rail-to-Rail Voltage FB Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 1.5mV offset and 400ns settling to 0.5LSB for a 4V swing. It is suitable for applications with a single 5V supply. THD and noise are –93dB to 40kHz and below 1LSB to 800kHz (A_V = 1, $2V_{P-P}$ into 1kΩ, V_S = 5V), making the part excellent for AC applications where rail-to-rail performance is desired. Quad version is available as LT1633.

LT1813: Dual 100MHz 750V/µs 3mA Voltage Feedback Amplifier. 5V to ±5V supplies. Distortion is –86dB to 100kHz and –77dB to 1MHz with ±5V supplies ($2V_{P-P}$ into 500Ω). Excellent part for fast AC applications with ±5V supplies.

INPUT FILTERING AND SOURCE IMPEDANCE

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1402 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 80MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 2 shows a 68pF capacitor from A_{IN}^+ to ground and a 51Ω source resistor to limit the input bandwidth to 47MHz. The 68pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch-sensitive circuitry.

High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity.

Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems. When high amplitude unwanted signals are close in frequency to the desired signal frequency, a multiple pole filter is required. Figure 3 shows a simple implementation using an LTC1560-1, a fifth order elliptic continuous-time 1MHz filter.

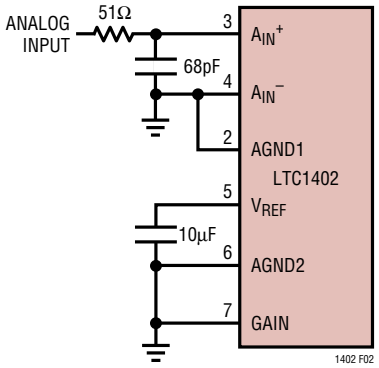

Figure 2. RC Input Filter

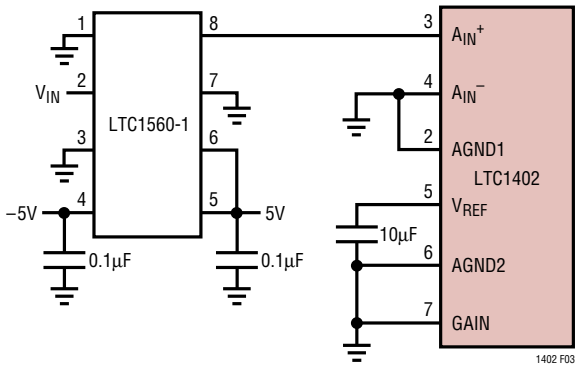

Figure 3. 1MHz Fifth Order Elliptic Lowpass Filter

BIPOLAR AND UNIPOLAR INPUT RANGES

The ±2V bipolar input range of the LTC1402 is optimized for low noise and low distortion. Most op amps also perform best over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry. The inputs of the LTC1402 may also be driven fully differential in bipolar mode with a single supply. Each input should not swing more than $2V_{P-P}$ individually to get the best performance from single supply amplifiers.

The 0V to 4V range is ideal for single ended input use with single supply applications.

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INTERNAL REFERENCE

The LTC1402 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.048V. It is connected internally to a reference amplifier, see Figure 4. The reference amplifier amplifies the voltage at the V_{REF} pin by 2 to create the required internal reference voltage of 4.096V. This provides buffering for the high speed capacitive DAC. The reference amplifier output V_{REF}, (Pin 5) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF ceramic or a 10µF tantalum in parallel with a 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with an external reference as shown in Figure 5a. The GAIN pin (Pin 7) is tied to the positive supply to disable the internal reference buffer.

A DAC may also be used to drive V_{REF} as shown in Figure 6. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal LTC1402 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 5ms should be allowed after a reference adjustment.

DIFFERENTIAL INPUTS

The LTC1402 has a unique differential sample-and-hold circuit that allows inputs from –2.5V to 5V. The ADC will always convert the difference of $A_{IN}^+ - A_{IN}^-$ independent of the common mode voltage. The common mode rejection holds up at extremely high frequencies, see Figure 7.

The only requirement is that both inputs not exceed –2.5V or 5V. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage. However, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage. Figure 5b shows the use of bipolar mode with single 5V supply.

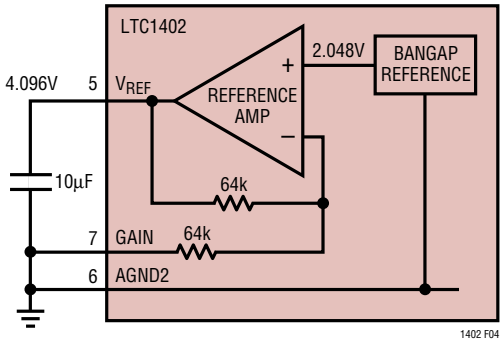

Figure 4. LTC1402 Reference Circuit

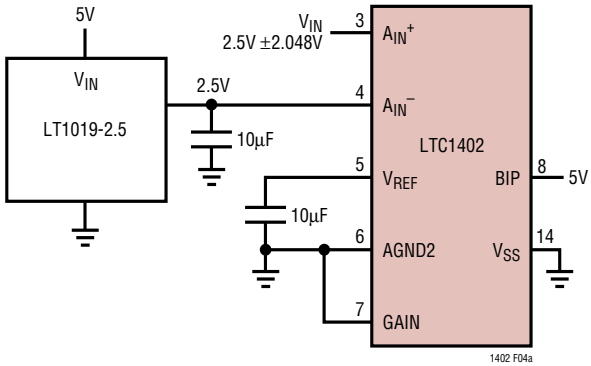

Figure 5b. Bipolar Mode with Single Supply

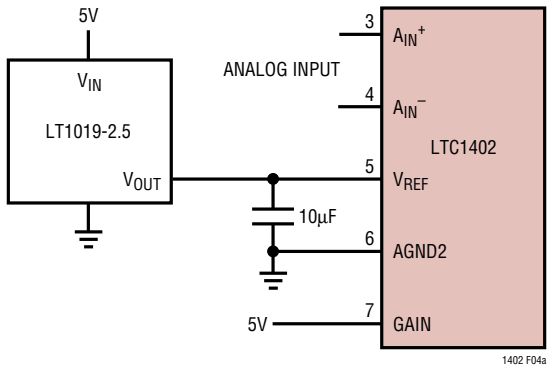

Figure 5a. Using the LT1019-2.5 as an External Reference

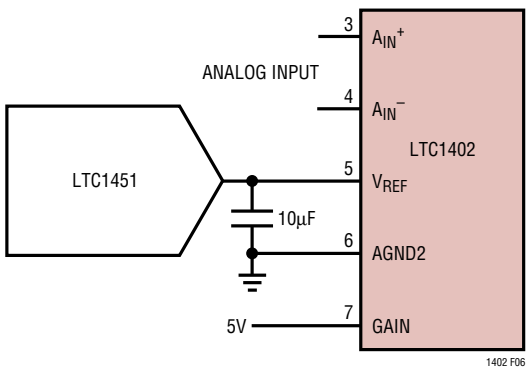

Figure 6. Driving V_{REF} with a 12 Bit, V_{OUT} DAC

APPLICATIONS INFORMATION

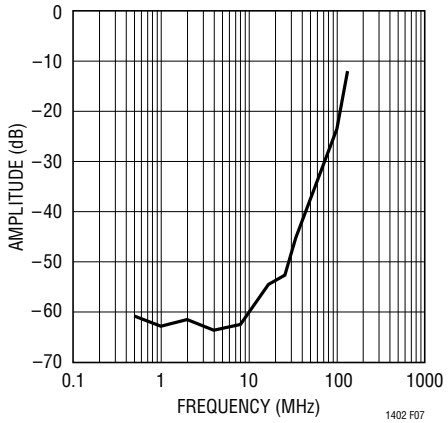

Figure 7. CMRR vs Input Frequency

INPUT SPAN VERSUS REFERENCE VOLTAGE

The differential input range has a voltage span that equals the difference between the voltage at the reference buffer output V_{REF} at Pin 5, and the voltage at the reference ground AGND2 at Pin 6. The external reference voltage may have any value between 2V and 5V. The internal ADC is referenced to these two points. If you use an external reference, tie the GAIN (Pin 7) to AV_{DD} (Pin 1) to disable the internal reference, and connect the external reference between V_{REF} (Pin 5) and AGND2 (Pin 6).

If you cut the reference voltage in half by halving the gain of the reference buffer with the GAIN (Pin 7) tied to V_{REF} (Pin 5), the input span also cuts in half. In bipolar mode, the differential input range changes from ±2.048V to ±1.024V, when the reference is cut in half. In unipolar mode, the differential input range changes from 0V-4.096V to 0V-2.048V, for the same reference cut in half. Note that in both unipolar and bipolar modes, the input range pivots around 0V with changing reference voltage. AGND2 (Pin 6) has no direct effect on the ADC offset voltage, it only affects input voltage span. Any external offsetting voltages must be applied through the A_{IN}^+ and A_{IN}^- inputs, as shown in Figure 10b.

SEVERAL LTC1402 ADCs MAY SHARE ONE EXTERNAL REFERENCE

Figure 8 shows how several ADCs can share a single common external reference. The V_{REF} (Pin 5) and AGND2 (Pin 6) of several LTC1402 ADCs can be tied together to share the same external reference in a data acquisition system. Tie GAIN (Pin 7) to AV_{DD} at each ADC to disable all the internal references. When AGND2 (Pin 6) is tied to the external ground plane, it sources 2.7mA ±30% typically; approximately 2mA are sourced through an internal equivalent 2k resistance tied to the V_{REF} (Pin 5) at 4.096V and the remaining 0.7mA supply the internal reference ground. The V_{REF} (Pin 5) equivalent input resistance is the same 2k tied to AGND2 (Pin 6). When you bus a common reference voltage to several LTC1402 ADCs, you need to keep PC board track resistance low to avoid reference voltage attenuation at each ADC. For example, 0.5Ω of track resistance to Pins 5 or 6 causes 0.025% of reference voltage and input range reduction. Figure 8 shows optional buffer amplifiers at each ADC to eliminate resistive voltage drops from the common external reference to each ADC. Figure 8 shows 10µF bypass capacitors tied to the common analog ground plane, at V_{REF} (Pin 5) and AGND2 (Pin 6), wired closely to each ADC to eliminate crosstalk of internal ADC glitch currents from one ADC to another. The 10µF bypass capacitors are recommended whether you drive Pins 5 and 6 with amplifiers, or with copper traces

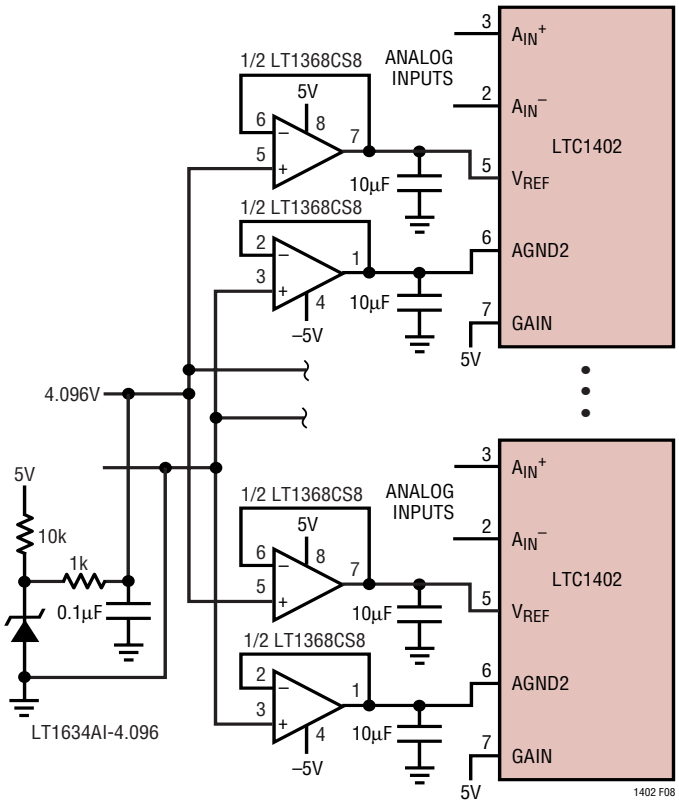

Figure 8. Several LTC1402 ADCs Can Share a Single External Reference

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more than 0.25 inch long to the common reference. You may also choose to tie AGND2 (Pin 6) directly to a solid analog ground plane and eliminate all the 10µF capacitors at this pin. The external reference source needs to have enough output drive current for the 2kΩ load at each ADC.

FULL-SCALE AND OFFSET ADJUSTMENT

Figure 9 shows the ideal input/output characteristics for the LTC1402 in bipolar mode and unipolar mode. Figure 10a shows the components required for full-scale error adjustment. Figure 10b includes the components for offset and full-scale adjustment.

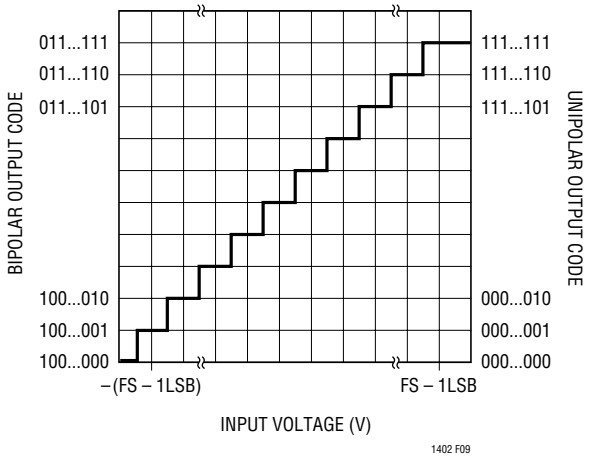

Figure 9. LTC1402 Transfer Characteristic

Adjustment in Bipolar Mode with Pin 8 Held High

The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB,...FS – 2.5LSB, FS – 1.5LSB). The output at D_{OUT} is two's complement binary with 1LSB = FS – (–FS)/4096 = 4.096V/4096 = 1.0mV. In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. In Figure 10b, zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error, apply –0.5mV (i.e., –0.5LSB) to A_{IN}^+ and adjust the offset at the A_{IN}^- input using R8 until the output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment in Figures 10a and 10b, apply an input voltage of 2.0465V (FS – 1.5LSB) to A_{IN}^+ and adjust R5 until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

Adjustment in Unipolar Mode with Pin 8 Held Low

The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB,...FS – 2.5LSB, FS – 1.5LSB). The output at D_{OUT} is binary with 1LSB = FS/4096 = 4.096V/4096 = 1.0mV. In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. In Figure 10b, zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error apply –0.5mV (i.e., –0.5LSB) to A_{IN}^+ and adjust the offset at the A_{IN}^- input using R8 until the output code flickers between

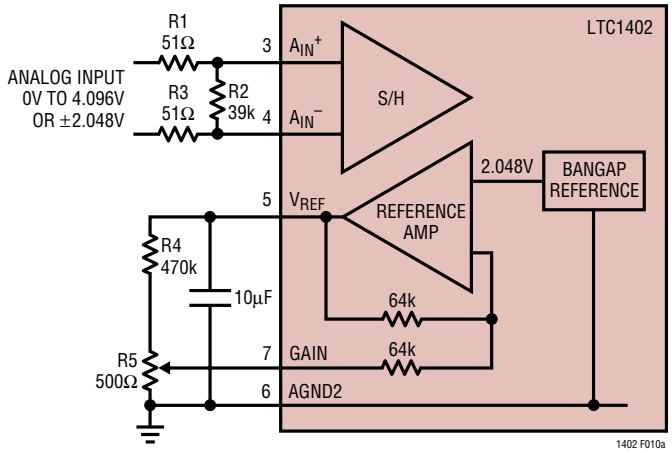

Figure 10a. Full-Scale Adjustment Circuit with ±10LSB Range

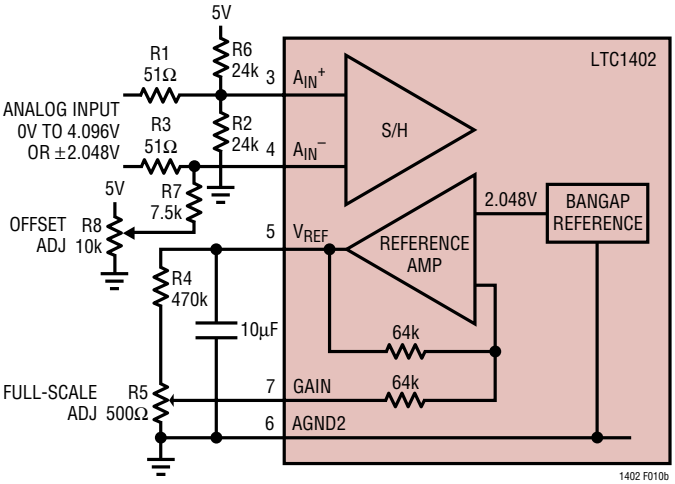

Figure 10b. Offset and Full-Scale Adjustment Circuits with ±10LSB Range

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0000 0000 0000 and 0000 0000 0001. For full-scale adjustment in Figures 10a and 10b, apply an input voltage of 2.0465V (FS – 1.5LSBs) to A_{IN}^+ and adjust R5 until the output code flickers between 1111 1111 1110 and 1111 1111 1111.

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution and/or high speed A/D converters. To obtain the best performance from the LTC1402, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 2 (AGND1), Pin 6 (AGND2), Pin 13 (DGND) and all other analog grounds should be connected directly to an analog ground plane. Pin 9 (OGND) should be connected near Pin13 (DGND), where the analog ground plane ties to the logic system ground. The V_{REF} bypass capacitor and the DV_{DD} bypass capacitor should also be connected to this analog ground plane, see Figure 11. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1402 has differential inputs to minimize noise coupling. Common mode noise on the A_{IN}^+ and A_{IN}^- leads will be rejected by the input CMRR. The A_{IN}^- input can be used as a ground sense for the A_{IN}^+ input; the LTC1402 will hold and convert the difference voltage between A_{IN}^+ and A_{IN}^-. The leads to A_{IN}^+ (Pin 3) and A_{IN}^- (Pin 4) should be kept as short as possible. In applications where this is not possible, the A_{IN}^+ and A_{IN}^- traces should be run side-by-side to cancel noise coupling.

SUPPLY BYPASSING

High quality, low series resistance 10µF ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively, 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

POWER-DOWN MODES

Upon power-up, the LTC1402 is initialized to the active state and is ready for conversion. The Nap and Sleep Mode waveforms show the power-down modes for the LTC1402. The SCK and CONV inputs control the power-down modes (see Timing Diagrams). Two rising edges at CONV, without any intervening rising edges at SCK, put the LTC1402 in Nap mode and the power drain drops from 90mW to

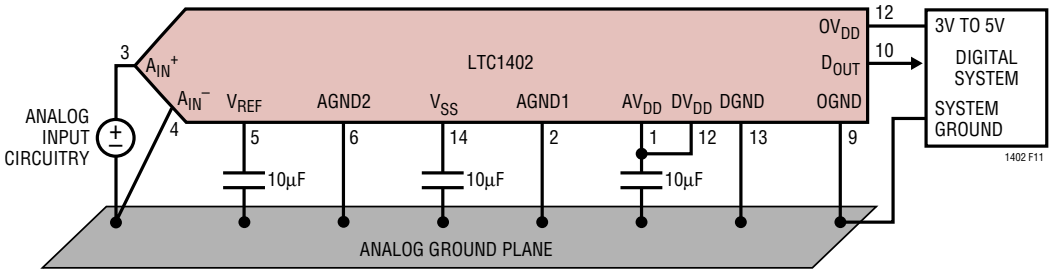

Figure 11. Power Supply Grounding Practice

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15mW. The internal reference remains powered in Nap mode. One or more rising edges at SCK wake up the LTC1402 for service very quickly, and CONV can start an accurate conversion within a clock cycle. Four rising edges at CONV, without any intervening rising edges at SCK, put the LTC1402 in Sleep mode and the power drain drops from 90mW to 10µW. One or more rising edges at SCK wake up the LTC1402 for operation. The internal reference (V_{REF}) takes 2ms to slew and settle with a 10µF load, and the REFREADY bit in the D_{OUT} stream takes an additional 10ms to go high after the reference output Pin 5 (V_{REF}) has finished slewing. Note that, using sleep mode more frequently than every 2ms, compromises the settled accuracy of the internal reference. Figure 12 shows the power consumption versus the conversion rate. Note that, for slower conversion rates, the Nap and Sleep modes can be used for substantial reductions in power consumption.

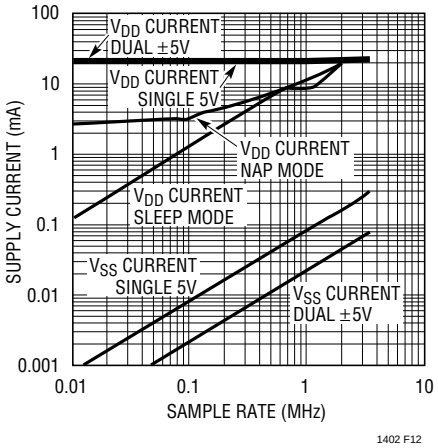

Figure 12. Power Consumption vs Sample Rate in Normal Mode, Nap Mode and Sleep Mode

DIGITAL INTERFACE

The LTC1402 has a 3-wire SPI (Serial Protocol Interface) interface. The SCK and CONV inputs and D_{OUT} output implement this interface. The SCK and CONV inputs are TTL compatible and also accept swings from 3V or 5V logic. The amplitude of D_{OUT} can easily produce 5V logic or 3V logic swings by tying the independent output supply OV_{DD} (Pin 11) to the same supply as system logic. A detailed description of the three serial port signals follows.

CONV at Pin 16

The rising edge of CONV starts a conversion but subsequent rising edges at CONV, during the following 14 SCK cycles of conversion, are ignored by the LTC1402. The duty cycle of CONV can be arbitrarily chosen to be used as a frame sync signal for the processor serial port. A simple approach to generate CONV is to create a pulse that is one SCK wide to drive the LTC1402 and then buffer this signal with the appropriate number of inverters to drive the frame sync input of the processor serial port. It is good practice to drive the LTC1402 CONV input first to avoid digital noise interference during the sample-to-hold transition triggered by CONV at the start of conversion. Another point to consider is the level of jitter in the CONV signal if the input signals have fast transients or sinewaves. Some processors can be programmed to generate a convenient frame sync pulse at their serial port, but often this signal is derived from a jittery processor phase locked loop clock multiplier. This is true even if a low jitter crystal clock is the reference for the processor clock multiplier.

SCK at Pin 15

The rising edge of SCK advances the conversion process and also udpates each bit in the D_{OUT} data stream. After CONV rises, the second rising edge of SCK sends out the REFREADY bit. Subsequent edges send out the 12 data bits, with the MSB sent first. A simple approach is to generate SCK to drive the LTC1402 and then buffer this signal with the appropriate number of inverters to drive the serial clock input of the processor serial port. The rising edge of SCK is guaranteed to coincide with stable data at D_{OUT}. It is good practice to drive the LTC1402 SCK input first to avoid digital noise interference during the internal bit comparison decision by the internal high speed comparator. Unlike the CONV input, the SCK input is not sensitive to jitter because the input signal is already sampled and held constant.

D_{OUT} at Pin 10

Upon power-up, the D_{OUT} output is automatically reset to the high impedance state. The D_{OUT} output remains in high impedance until a new conversion is started. D_{OUT} sends out 13 bits in the output data stream after the second rising edge of SCK after the start of conversion with the rising

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edge of CONV. Please note the delay specification from SCK to a valid D_{OUT}. D_{OUT} is always guaranteed to be valid by the next rising edge of SCK.

DIGITAL JITTER AT CONV (PIN 16)

In high speed applications, where high amplitude sinewaves above 100kHz are sampled, the CONV signal must have as little jitter as possible (10ps or less). The square wave output of a common crystal clock module usually meets this requirement easily. The challenge is to generate a CONV signal from this crystal clock without jitter corruption from other digital circuits in the system. A clock divider and any gates in the signal path from the crystal clock to the CONV input should not share the same integrated circuit with other parts of the system. As shown in the interface circuit examples, the LTC1402's SCK and CONV inputs should be driven first with digital buffers used to drive the serial port interface. Also note that the master clock in the DSP may already be corrupted with jitter, even if it comes directly from the DSP crystal. Another problem with high speed processor clocks is that they often use a low cost, low speed crystal (i.e., 10MHz) to generated a fast, but jittery, phase locked loop system clock (i.e., 40MHz). The jitter, in these PLL-generated high speed clocks, can be several nanoseconds. Note that if you choose to use the frame sync signal generated by the DSP port, this signal will have the same jitter of the DSP's master clock.

SERIAL TO PARALLEL CONVERSION

You can take advantage of the serial interface of the LTC1402 in a parallel data system to minimize bus wiring congestion in the PC board layout. Figure 13 shows an example of this interface. It is best to send the SCK and CONV signals to the LTC1402, and then bus them together across the board to avoid excessive time skew among the three signals. It is usually not necessary to buffer D_{OUT}, if the PC track is not too long. Buffering SCK and CONV prevents jitter from corrupting these signals. The relative phase between SCK and CONV affects the position of the parallel word at the output of the 74HC595. The position of the output word in Figure 13 assumes 16 clocks between each CONV rising edge, and the CONV pulse is one clock wide.

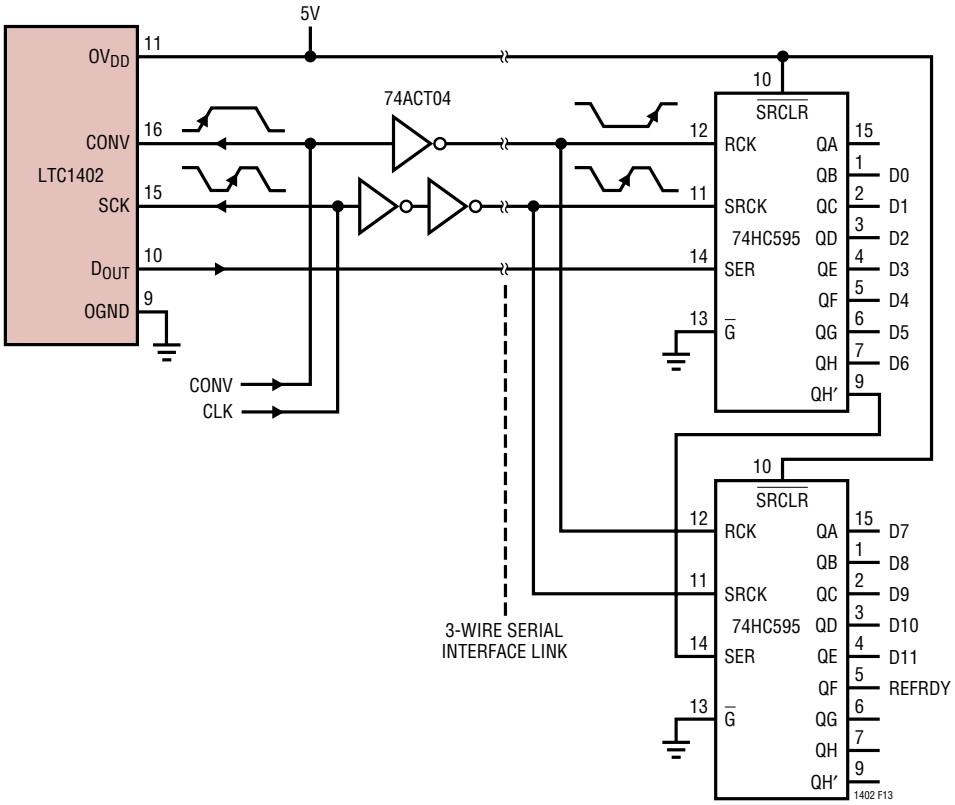

Figure 13. Serial to Parallel Interface

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HARDWARE INTERFACE TO TMS320C54x

The LTC1402 is a serial output ADC whose interface has been designed for high speed buffered serial ports in fast digital signal processors (DSPs). Figure 14 shows an example of this interface using a TMS320C54X.

The buffered serial port in the TMS320C54x has direct access to a 2kB segment of memory. The ADC's serial data can be collected in two alternating 1kB segments, in real time, at the full 2.2Msps conversion rate of the LTC1402. The DSP assembly code sets frame sync mode at the BFSR pin to accept an external positive going pulse, and the serial clock at the BCLKR pin to accept an external positive edge clock. Buffers near the LTC1402 may be added to drive long tracks to the DSP to prevent corruption of the signal to LTC1402. This configuration is adequate to traverse a typical system board, but source resistors at the buffer outputs, and termination resistors at the DSP may be needed to match the characteristic impedance of very long transmission lines. If you need to terminate the D_{OUT} transmission line, buffer it first with one or two 74ACxx gates. The TTL threshold inputs of the DSP port respond properly to the 2.5V swing of the terminated transmission lines. The OV_{DD} supply output driver supply voltage can be driven directly from the DSP.

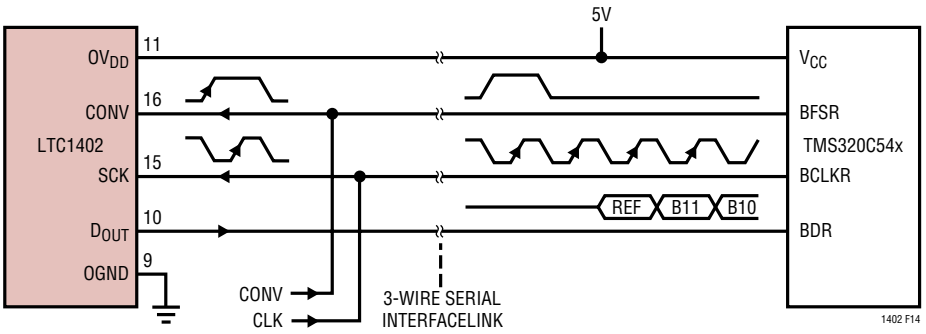

Figure 14. DSP Serial Interface to TMS320C54x

APPLICATIONS INFORMATION

```
; ***************************************************************************
; Files: BSP2KB.ASM ->
; 2kbyte collection into DSKPlus TMS320C542 with Serial Port interface to LTC1402
; first element at 1024, last element at 1023, two middle elements at 2047 and 0000
; bipolar mode
; ***************************************************************************
        .width    160
        .length   110
        .title “sineb0 BSP in auto buffer mode”
        .mmregs
        .setsect  “.text”,     0x500,0     ;Set address of executable
        .setsect  “vectors”, 0x180,0       ;Set address of incoming 1402 data
        .setsect  “buffer”,   0x800,0      ;Set address of BSP buffer for clearing
        .setsect  “result”,   0x1800,0     ;Set address of result for clearing
       .text                               ;.text marks start of code
start:              ;Make sure /PWRDWN is low at J1-9 to turn off AC01 adc
       tim=#0fh
       prd=#0fh
       tcr = #10h          ; stop timer
       tspc = #0h          ; stop TDM serial port to AC01
       pmst = #01a0h       ; set up iptr. Processor Mode STatus register
       sp = #0700h         ; init stack pointer.
       dp = #0             ; data page
       ar2 = #1800h        ; pointer to computed receive buffer.
       ar3 = #0800h        ; pointer to Buffered Serial Port receive buffer
       ar4 = #0h           ; reset record counter
       call sineinit         ; Double clutch the initialization to insure a proper
sinepeek:                    ; insert debugger break here to view results
       call sineinit         ; reset. The external frame sync must occur 2.5 clocks
                             ; or more after the port comes out of reset.
wait   goto   wait
;     ————————————Buffered Receive Interrupt Routine ————————————
breceive:
       ifr = #10h                        ; clear interrupt flags
       TC = bitf(@BSPCE,#4000h)          ; check which half (bspce(bit14)) of buffer
       if (NTC) goto bufull              ; if this still the first half get next half
       bspce = #(2023h + 08000h)         ; turn on halt for second half (bspce(bit15))
       return_enable
;      ————————————mask and shift input data after 2k buffer is full——-
bufull:
       b = *ar3+ << -2                   ; load acc b with BSP buffer and shift right 2
       b = #00FFFh & b                   ; mask out the REF bit and the 3 other tristate bits
       b = #00800h ^ b                   ; invert BIPOLAR MSB. Comment this line in UNIPOLAR mode
       *ar2+ = data(#0bh)                ; store B to out buffer and advance AR2 pointer
       TC = (@ar2 == #02000h)            ; output buffer is 2k starting at 1800h
       if (TC) goto start                ; restart if out buffer is at 1fffh
       goto bufull
;      ————————————dummy bsend return————————————————
bsend   return_enable                    ;this is a dummy return to define bsend
                                         ;in vector table below
;     ———————————— end ISR ————————————————
       ;initialize buffered serial port
*************************************************************************
*      BSP initialization code for the ‘C54x DSKplus                    *
*      for use with 1402 in standard mode                               *
*      BSPC and SPC are the same in the ‘C542                           *
*************************************************************************
ON          .set 1
OFF         .set !ON
YES         .set 1
NO          .set !YES
BIT_8       .set 2
BIT_10      .set 1
BIT_12      .set 3
BIT_16      .set 0
GO          .set 0x80
*************************************************************************
```

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```
* This is an example of how to initialize the Buffered Serial Port (BSP).
* The BSP is initialized to require an external CLK and FSX for
* operation. The data format is 16-bits, burst mode, with autobuffering
* enabled.
*
*
*****************************************************************************************************
*Timing at BSP pins in DSKPLUS TMS320c542 board with inverters at BCLKR and BFSR.                     *
*BFSR  Pin JP1-20 ~\___/~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~\___/~~~~~~~~~~~*
*BCLKR Pin JP1-14 _/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/~\_/  *
*BDR   Pin JP1-26 -_—_—<REF-B11-B10-B09-B08-B07-B06-B05-B04-B03-B02-B01-B00>—_—_—<REF-B11-              *
*CLKIN Pin JP5-09 ~~~~~\_______/~~~~~~~~\_______/~~~~~~~~\_______/~~~~~~~~\_______/~~~~~~~~\_______/~~~~  *
*                                                                                                    *
*A 2 place right shift is needed to right justify the input data.                                     *
*The REF bit is also be masked in this example                                                        *
*****************************************************************************************************
*
Loopback        .set   NO          ;(digital looback mode?)                DLB bit
Format          .set   BIT_16      ;(Data format? 16,12,10,8)              FO bit
IntSync         .set   NO          ;(internal Frame syncs generated?)      TXM bit
IntCLK          .set   NO          ;(internal clks generated?)             MCM bit
BurstMode       .set   YES         ;(if BurstMode=NO, then Continuous)     FSM bit
CLKDIV          .set   3           ;(3=default value, 1/4 CLOCKOUT)
PCM_Mode        .set   NO          ;(Turn on PCM mode?)
FS_polarity     .set   NO          ;(change polarity)YES=^^^\_/^^^, NO=___/^\___
CLK_polarity    .set   YES         ;(change polarity)for BCLKR YES=_/^, NO=~\_
Frame_ignore    .set   !YES         ;(inverted  !YES -ignores frame)
XMTautobuf      .set   NO          ;(transmit autobuffering)
RCVautobuf      .set   YES         ;(receive autobuffering)
XMThalt         .set   NO          ;(transmit buff halt if XMT buff is full)
RCVhalt         .set   NO          ;(receive buff halt if RCV buff is full)
XMTbufAddr      .set   0x800       ;(address of transmit buffer)
XMTbufSize      .set   0x000       ;(length of transmit buffer)
RCVbufAddr      .set   0x800       ;(address of receive buffer)
RCVbufSize      .set   0x800       ;(length of receive buffer)works up to 800
*
*
*
*************************************************************************
      .eval ((Loopback >> 1)|((Format & 2)<<1)|(BurstMode <<3)|(IntCLK <<4)|(IntSync <<5)) ,SPCval
      .eval ((CLKDIV)|(FS_polarity <<5)|(CLK_polarity<<6)|((Format & 1)<<7)|(Frame_ignore<<8)|(PCM_Mode<<9)), SPCEval
      .eval (SPCEval|(XMTautobuf<<10)|(XMThalt<<12)|(RCVautobuf<<13)|(RCVhalt<<15)), SPCEval
sineinit:
      bspc = #SPCval             ; places buffered serial port in reset
      ifr = #10h                 ; clear interrupt flags
      imr = #210h                ; Enable HPINT,enable BRINT0
      intm = 0                   ; all unmasked interrupts are enabled.
      bspce = #SPCEval           ; programs BSPCE and ABU
      axr = #XMTbufAddr          ; initializes transmit buffer start address
      bkx = #XMTbufSize          ; initializes transmit buffer size
      arr = #RCVbufAddr          ; initializes receive buffer start address
      bkr = #RCVbufSize          ; initializes receive buffer size
      bspc = #(SPCval | GO)      ; bring buffered serial port out of reset
      return                     ;for transmit and receive because GO=0xC0
      .space 16*32               ;clear a chunk at the end to mark the end
;=========================================================================
;
;  VECTORS
;
;=========================================================================
      .sect “vectors”                  ;The vectors start here
      ;get BSP vectors
; ************************************************************************
;                     Vector Table for the ‘C54x DSKplus
;                     BSP vectors and Debugger vectors
;                     TDM vectors just return
; ************************************************************************
```

APPLICATIONS INFORMATION

```
; The vectors in this table can be configured for processing external and
; internal software interrupts. The DSKplus debugger uses four interrupt
; vectors. These are RESET, TRAP2, INT2, and HPIINT.
;   *  DO NOT MODIFY THESE FOUR VECTORS IF YOU PLAN TO USE THE DEBUGGER  *
;
; All other vector locations are free to use. When programming always be sure
; the HPIINT bit is unmasked (IMR=200h) to allow the communications kernel and
; host PC interact. INT2 should normally be masked (IMR(bit 2) = 0) so that the
; DSP will not interrupt itself during a HINT. HINT is tied to INT2 externally.
;
;
;
        .mmregs
reset   goto #80h           ;00; RESET  * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
nmi     return_enable       ;04; non-maskable external interrupt
        nop
        nop
        nop
trap2   goto #88h           ;08; trap2  * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
        .space 52*16        ;0C-3F: vectors for software interrupts 18-30
int0    return_enable       ;40; external interrupt int0
        nop
        nop
        nop
int1    return_enable       ;44; external interrupt int1
        nop
        nop
        nop
int2    return_enable       ;48; external interrupt int2
        nop
        nop
        nop
tint    return_enable       ;4C; internal timer interrupt
        nop
        nop
        nop
brint   goto breceive       ;50; BSP receive interrupt
        nop
        nop
        nop
bxint   goto bsend          ;54; BSP transmit interrupt
        nop
        nop
        nop
trint   return_enable       ;58; TDM receive interrupt
        nop
        nop
        nop
txint   return_enable       ;5C; TDM transmit interrupt
        nop
        nop
int3    return_enable       ;60; external interrupt int3
        nop
        nop
        nop
hpiint  dgoto #0e4h         ;64; HPIint  * DO NOT MODIFY IF USING DEBUGGER *
        nop
        nop
        .space  24*16       ;68-7F; reserved area
        .sect “buffer”              ;Set address of BSP buffer for clearing
        .space 16*0x800
        .sect “result”              ;Set address of result for clearing
        .space 16*0x800
        .end
```

TYPICAL APPLICATION

Using Quad Cable Drivers/Receivers in Remote LTC1402 Applications

In some applications, the host controller or main processor may be located some distance from the sensor, the signal conditioning circuitry, and the ADC. In these applications, maintaining serial data integrity over long cable distances can be a challenge. The circuit in Figure 15 shows one way to convey the LTC1402's high-speed serial data over a long distance. The circuit uses the LTC1688 quad cable driver and an LTC1520 quad cable receiver to transmit/receive the LTC1402's high-speed 35.2Mbps serial data to the DSPs serial port over category-5 unshielded cable. Using these devices, the LTC1402's serial data can be transmitted up to 100 feet without data corruption. Because the SCK, CONV and D_{OUT} signals originate at the LTC1402, they arrive at the serial port with similar delays and remain synchronized. When the data is received at the serial port of the DSP or other controller, the port must be programmed to respond to the appropriate SCK and CONV edges. It is also necessary to check where the 12-bit output DATA resides in the 16-bit data frame. The TMS320C54x serial port READ instructions can shift the 12-bit data to the preferred position within the 16-bit data frame.

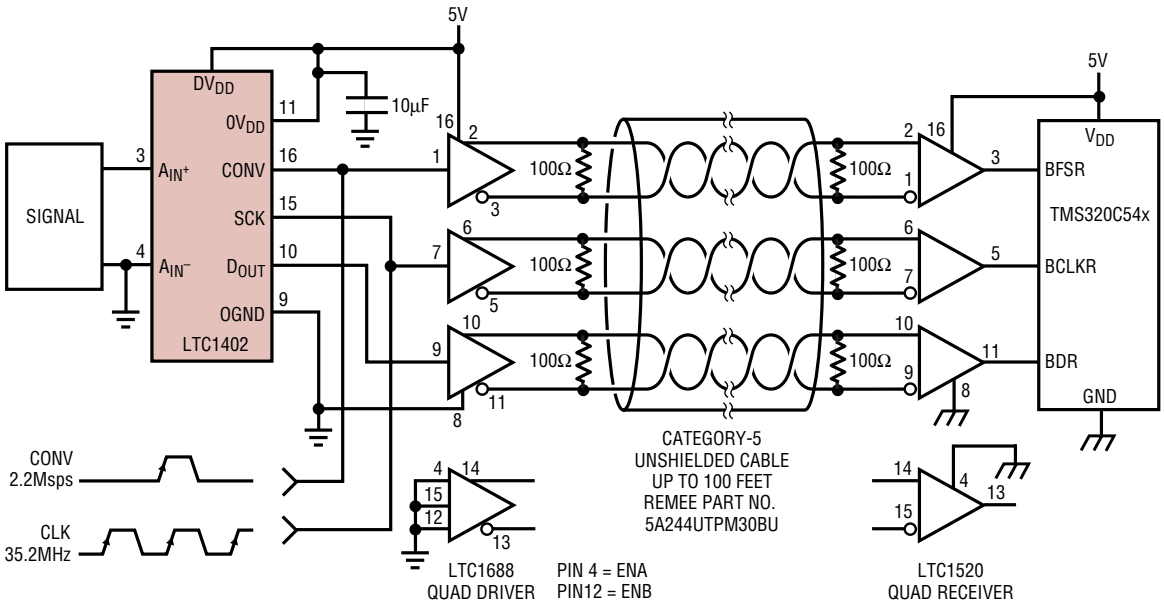
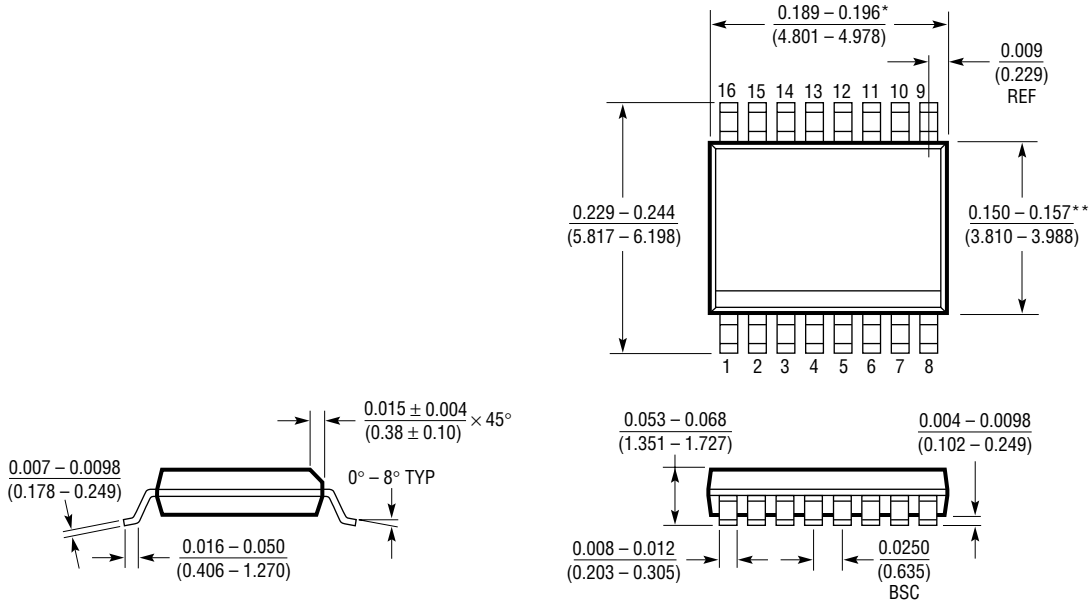


Figure 15. The LTC1402 3-Wire Serial Port Sends Data Over 100 Feet of Category-5 Twisted Pair with the LTC1688/LTC1520 Quad Driver/Receiver Pairs

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

RELATED PARTS

PART NUMBER	RESOLUTION	SPEED	COMMENTS
16-Bit			
LTC1604	16	333ksps	±2.5V Input Range, ±5V Supply
LTC1605	16	100ksps	±10V Input Range, Single 5V Supply
LTC1606	16	250ksps	±10V Input Range, Pin-Compatible with LTC1605
LTC1608	16	500ksps	±2.5V Input Range, Pin-Compatible with LTC1604
14-Bit			
LTC1414	14	2.2Msps	175mW, 80dB SINAD and 95dB SFDR
LTC1419	14	800ksps	150mW, 81.5dB SINAD and 95dB SFDR
LTC1416	14	400ksps	75mW, Low Power with Excellent AC Specs
LTC1418	14	200ksps	15mW, Single 5V, Serial/Parallel I/O
12-Bit			
LTC1412	12	3Msps	150mW, 72dB SINAD and 82dB SFDR
LTC1410	12	1.25Msps	150mW, 71.5dB SINAD and 84dB THD
LTC1415	12	1.25Msps	55mW, Single 5V Supply
LTC1409	12	800ksps	80mW, 71.5dB SINAD and 84dB THD
LTC1404	12	600ksps	High Speed Serial I/O in SO-8 Package
LTC1400	12	400ksps	High Speed Serial I/O in SO-8 Package
PART NUMBER	**DESCRIPTION**		**COMMENTS**
References			
LT1019-2.5	Precision Band Gap Voltage Reference		3ppm/°C Drift, 0.5% Max Initial Accuracy
LT1460-2.5	Micropower Series Voltage Reference		0.075% Initial Accuracy, 10ppm/°C Max Drift
LT1461-2.5	Precision Voltage Reference		3ppm/°C Drift, 0.05% Max Initial Accuracy
DACs			
LTC1451	12-Bit V_{OUT} DAC		SO-8 Package, 12-Bit Monotonic Overtemperature
LTC1452	12-Bit V_{OUT} Multiplying DAC		SO-8 Package, 2.7V to 5.5V Operation
LTC1456	12-Bit V_{OUT} DAC		0.5LSB DNL, SO-8 Package, Internal Reference

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