

Introduction

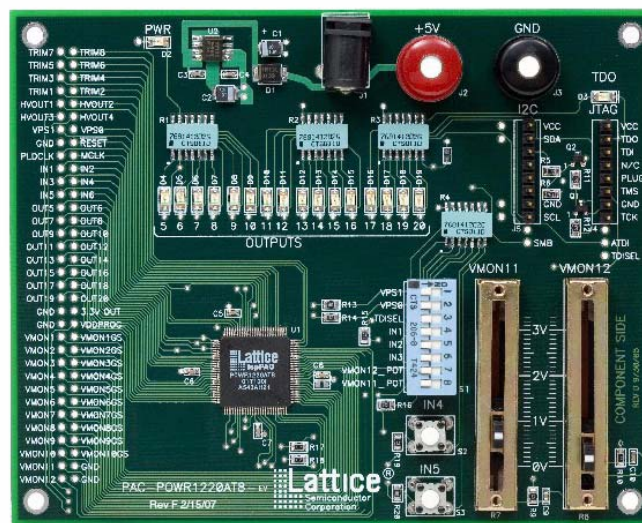
Lattice Semiconductor's Power Manager II ispPAC[®]-POWR1220AT8 device simplifies power supply design by integrating the analog and digital functions of power supply management (sequencing, monitoring, trimming/margining, measurement) into a single device. This device provides designers with a rich set of features: A/D and D/A conversion, precision comparators with a built-in voltage reference, MOSFET drivers with programmable slew rates, an easy-to-use closed-loop power supply voltage trim system, and a programmable logic device (PLD) for sequencing and supervisory logic functions. All of these blocks can be accessed via I²C for enhanced flexibility in systems employing an on-board microcontroller. Configuration for all subsystems in the ispPAC-POWR1220AT8 device is stored in non-volatile E²CMOS[®] memory. Programming is performed via the industry-standard JTAG IEEE 1149.1 interface.

PAC-POWR1220AT8-EV Evaluation Board

The PAC-POWR1220AT8-EV evaluation board (Figure 1) allows the designer to quickly configure and evaluate the ispPAC-POWR1220AT8 device on a fully assembled printed-circuit board. The four-layer board supports a 100-pin TQFP package, pads for user I/O, a JTAG programming cable connector, and a connector for the device's I²C interface. JTAG programming signals can be generated by using an ispDOWNLOAD[®] programming cable connected between the evaluation board and a PC's parallel (printer) port. Both analog and digital features of the ispPAC-POWR1220AT8 device can be easily configured using PAC-Designer[®] software. The actual size of the board is 5" x 4" (12.5 x 10 cm).

The I²C interface includes circuitry to allow the use of either an ispDOWNLOAD cable or standard open collector I²C bus. The I²C software utility that is included in PAC-Designer makes use of the ispDOWNLOAD cable interface to allow designers to evaluate the device's I²C capabilities without having to buy additional cables or adapters. More information about this software tool can be found in application note AN6067, *ispPAC-POWR1220AT8 I²C Hardware Verification Utility Users Guide*. Extra pads are provided adjacent to the I²C connector to allow the user to easily access the SDA and SCL signals as well as the regulated 3.3 volt VCC supply. Connection to a standard I²C bus or cable is done simply by connecting to the SDA, SCL, and GND pins of J5; pin #3 is left floating. Connection to an ispDOWNLOAD cable is done simply by mating the ispDOWNLOAD cable's connector to the I²C header (J5).

Figure 1. PAC-POWR1220AT8-EV Evaluation Board



Programming Interface

Lattice Semiconductor's ispDOWNLOAD cable can be used to program the ispPAC-POWR1220AT8 device on the evaluation board. This cable plugs into a PC-compatible's parallel port connector, and includes active buffer circuitry inside its DB-25 connector housing. The other end of the ispDOWNLOAD cable terminates in an 8-pin 0.100" pitch header connector which plugs directly into a mating connector provided on the PAC-POWR1220AT8-EV evaluation board (J4).

Power Supply Considerations

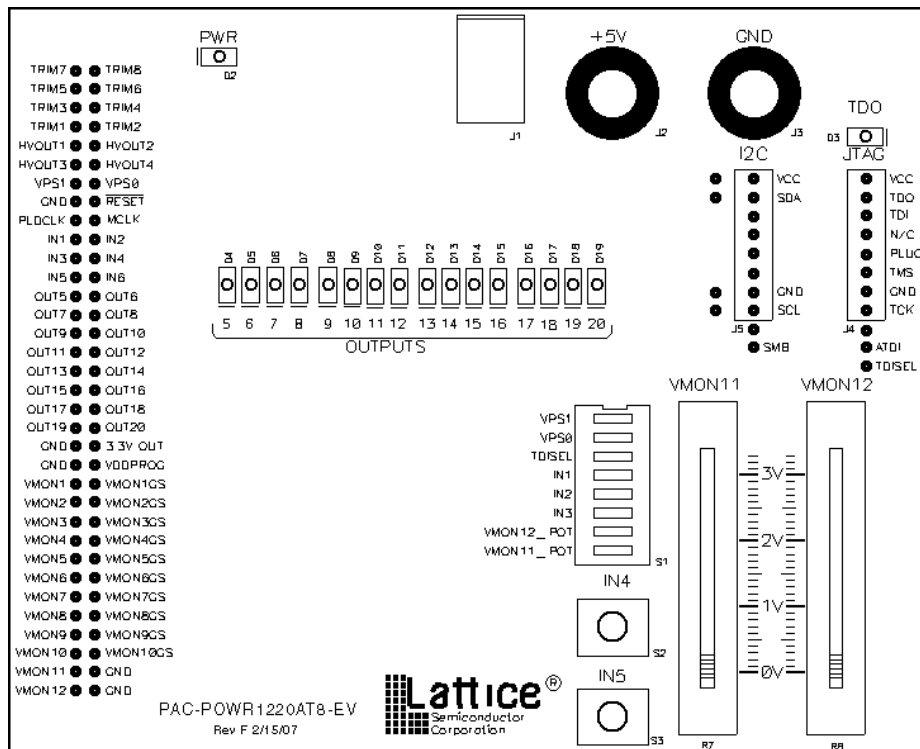
The ispPAC-POWR1220AT8 device operates with analog and digital core power supplies of 3.3V. To simplify evaluation work, the evaluation board was designed to operate from a single 4.5V to 5.5V power supply, which may be brought in through either a pair of banana plugs (J2 and J3), or a standard 5mm power plug (J1 - center tip positive). The evaluation board provides a linear regulator to provide the appropriate operating voltages for the ispPAC-POWR1220AT8 device, as well as reverse polarity protection.

Input/Output Connections

Connectors are provided for key functions and test points on this evaluation board, as shown in Figure 2. Power may be supplied in one of two ways; either through two color coded (RED = +, BLACK = -) banana jacks in the upper right corner of the board or through a 5mm (center pin +) DC power connector (J1). The JTAG programming cable is connected to a keyed header (J4) in the upper right corner of the board. Another header (J5) provides access to the device's I²C port. This header is pinned-out, and associated with interface circuitry so that in addition to providing a standard I²C bus connection (with on-board 2K pull-ups to 3.3V), it may also be driven by the Lattice DL2download cable when the "Power Manager I²C Utility" in PAC-Designer is used.

Access to a subset of the ispPAC-POWR1220AT8 device's I/O pins is available along the left edge of the assembly, where a 2x34 block of pads supports the attachment of test probes or a ribbon-cable connector. Pads for accessing the ATDI and TDISEL signals are provided immediately below the JTAG header (J4). An auxiliary connection for OUT5/SMB Alert is provided on a pad below the I²C header (J5).

Figure 2. I/O Connections, Controls and Indicators



Controls and Indicators

Two momentary switches, S2 and S3, are provided on the evaluation board. They are connected to IN4 and IN5, respectively. An 8-position dipswitch (S1) is provided on the evaluation board for the purpose of setting device inputs. Table 1 shows the options controlled by each switch:

Table 1. Switch S1 User Configuration Functions

Position	Function (when ON)
1	VPS1 – Voltage Profile Select bit 1
2	VPS0 – Voltage Profile Select bit 0
3	TDISEL
4	IN1
5	IN2
6	IN3
7	VMON12_POT
8	VMON11_POT

Switch positions 1 through 6 control logic inputs. When the switch is turned ON, the corresponding logic input goes HIGH. If a logic input is to be driven from an external signal source, then its associated DIP switch should be set to the OFF position.

Switch positions 1 and 2 control Voltage Profile Select pins VPS1 and VPS0, respectively. If the device has been programmed for voltage profile control via VPS0 and VPS1, then these switches are used to select the active voltage profile.

Switch position 3 controls the TDI selector pin, TDISEL. This switch should be in the ON position in order to program the device through J4.

Switch positions 4-6 control logic inputs IN1-IN3, respectively.

When in the ON position, switches 7 and 8 connect VMON11 and VMON12 to the two linear potentiometers provided on the board. This lets the user interactively apply analog voltages to the VMON11 and VMON12 inputs without the use of additional hardware. Note that the ground-sense pins for VMON11 and VMON12 have been hardwired to ground in order to support this feature.

Several red LEDs are also provided on the evaluation board to indicate proper function and as aids to debugging. LED D2 indicates that the on-board 3.3V supply is powered up. LED D3 is connected to the ispPAC-POWR1220AT8 device's TDO line, and will briefly flash when downloading, indicating that download data has made it to the device.

LEDs are also provided on digital outputs OUT5 through OUT20 so that a user may easily monitor the progress of sequence programs run on the evaluation board. Each of these LEDs uses a dual-resistor bias circuit that provides CMOS-3.3V compatible logic levels.

Schematics

The following four figures comprise the schematics for the ispPAC-POWR1220AT8-EV evaluation board. Figure 3 shows the on-board power-supply circuitry, Figure 4 shows the LED display and I²C adapter circuitry, Figure 5 shows user control circuits, while Figure 6 shows connections to the device itself.

Figure 3. On-Board Power Supply

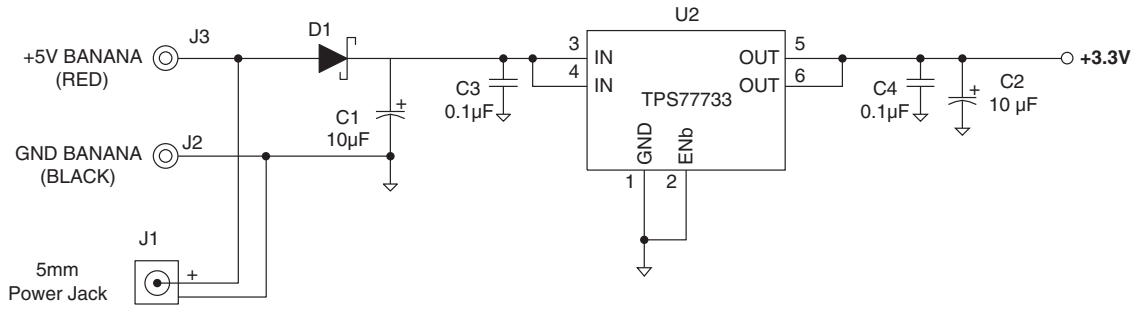


Figure 4. LED Indicators and I²C Port Interface

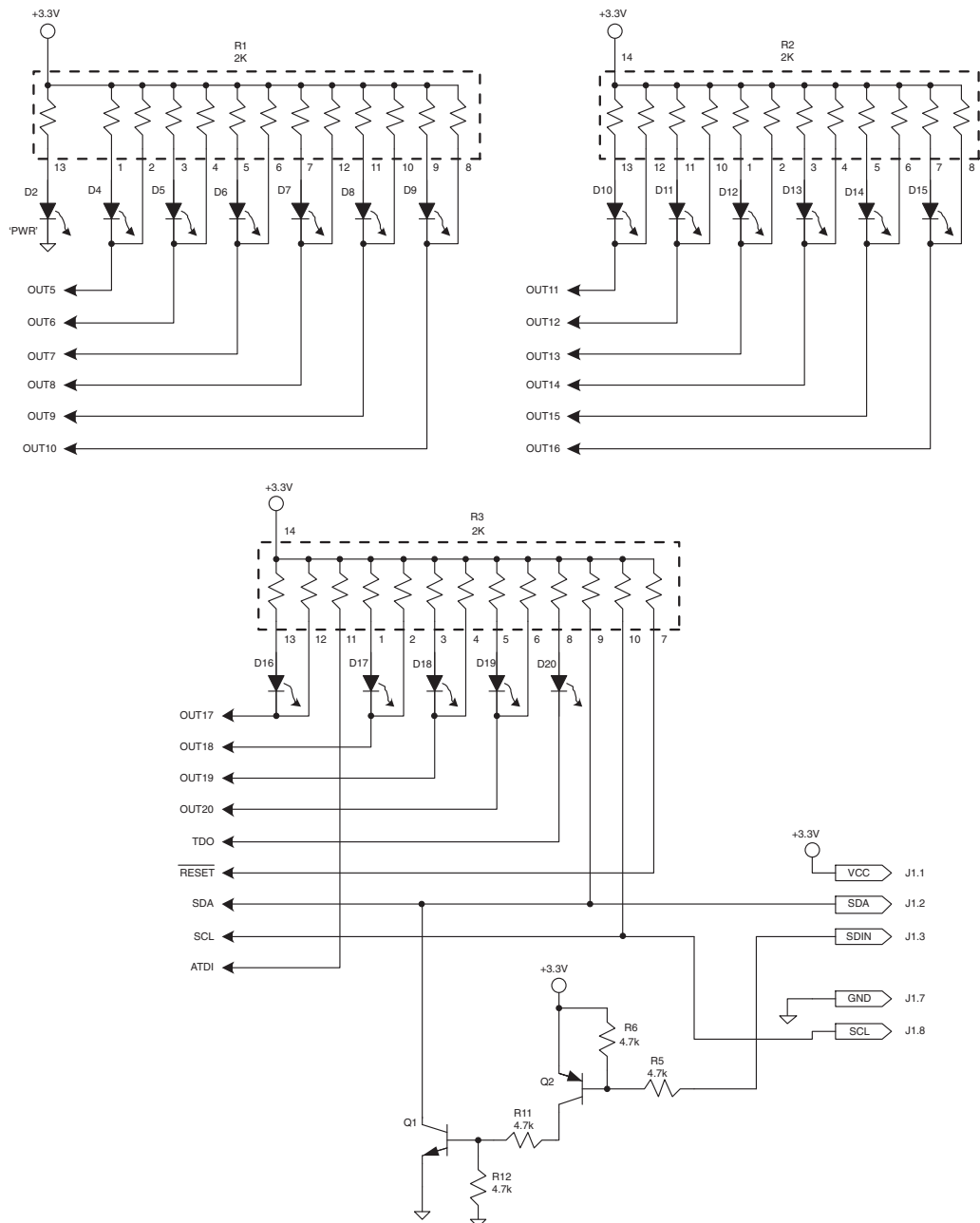


Figure 5. User Controls

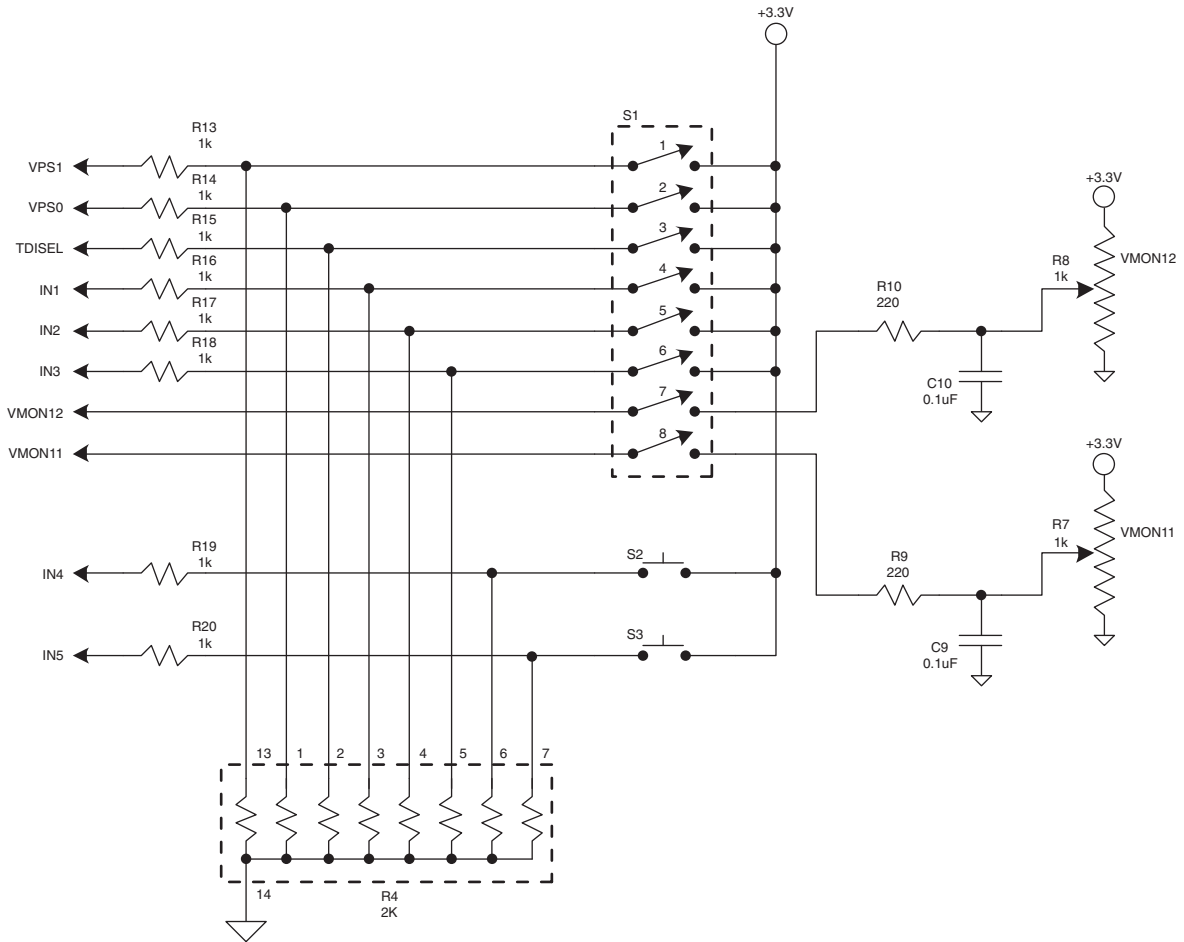
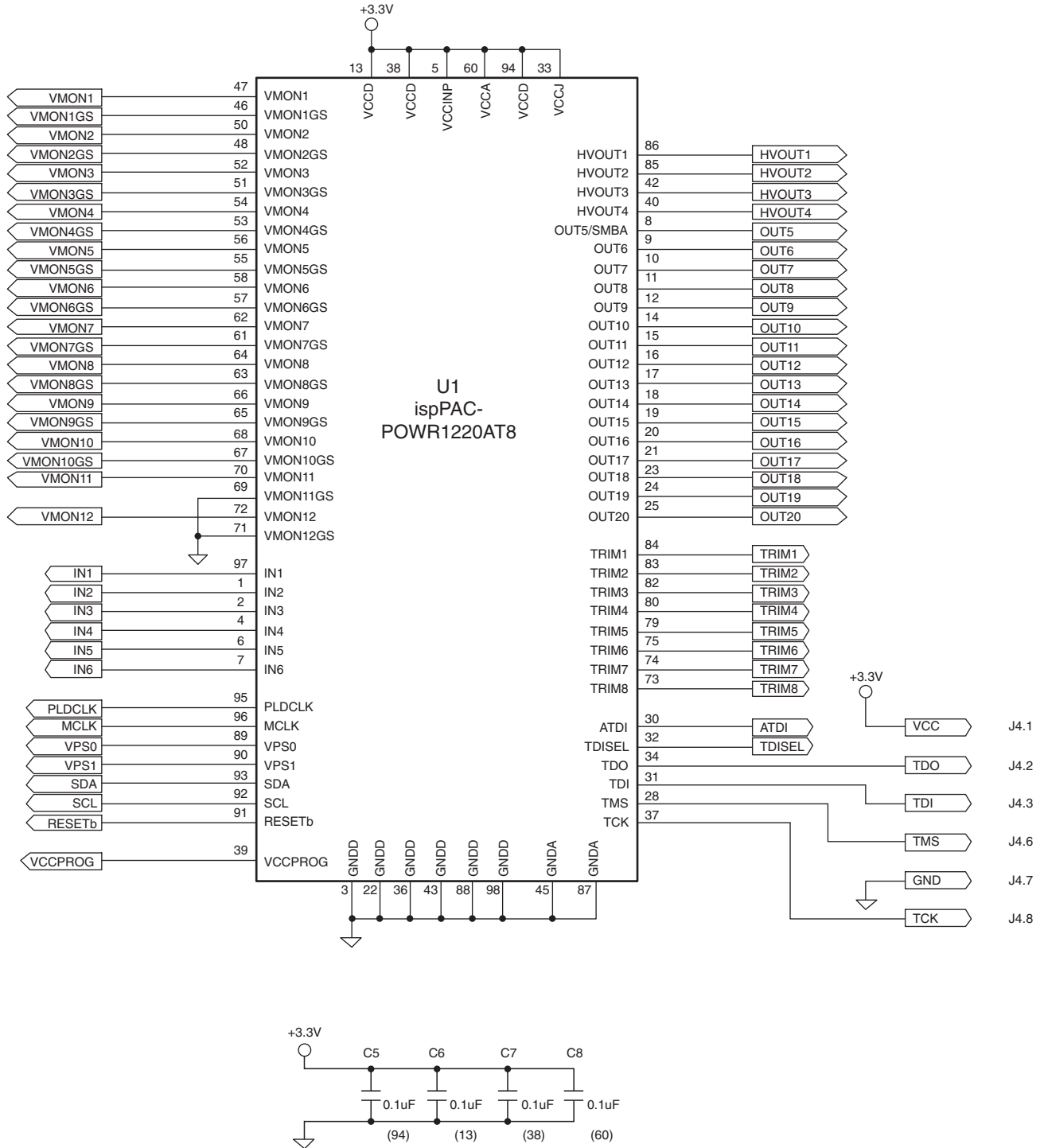


Figure 6. Device Connections



PCB Artwork

Figure 7. Silk Screen

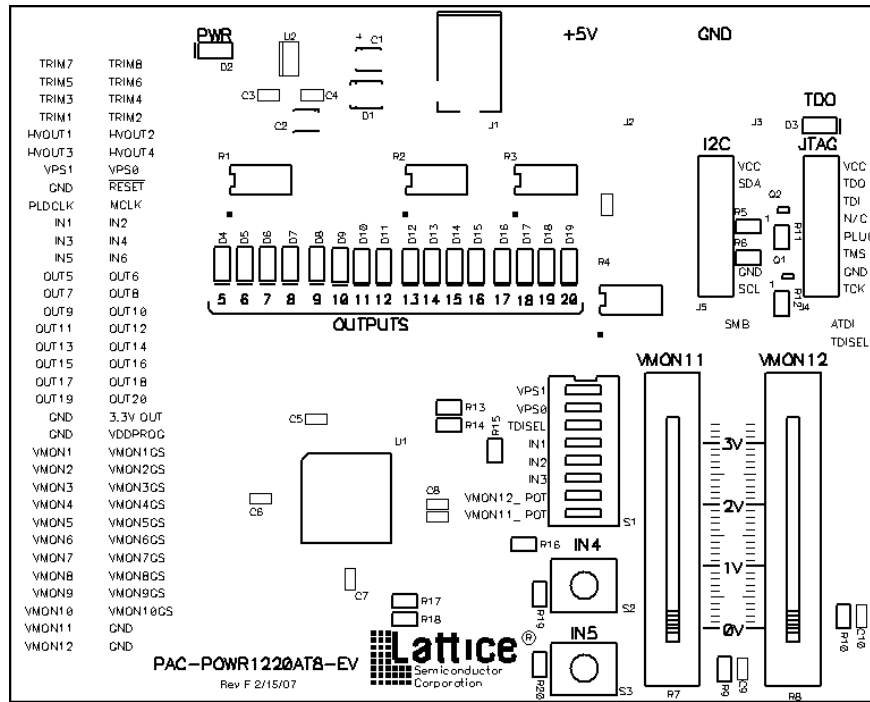


Figure 8. Component Side Copper (Layer 1)

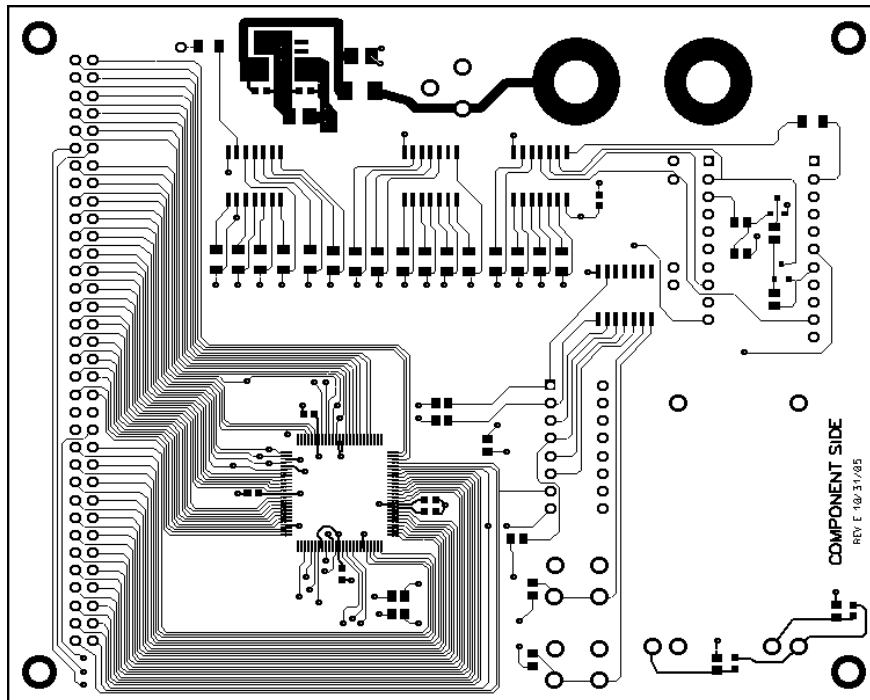


Figure 9. Ground Plane (Layer 2)

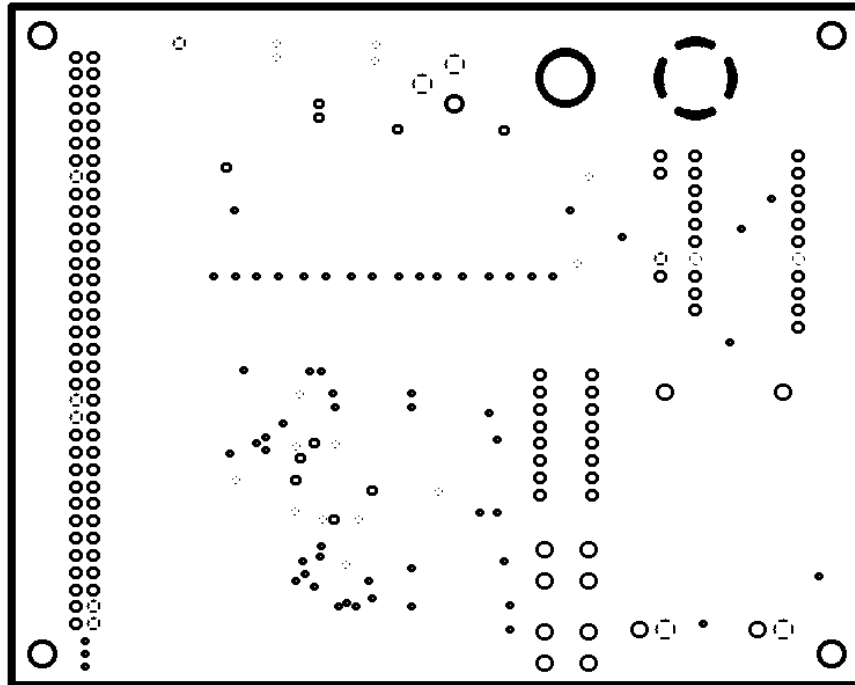


Figure 10. Power Plane (Layer 3)

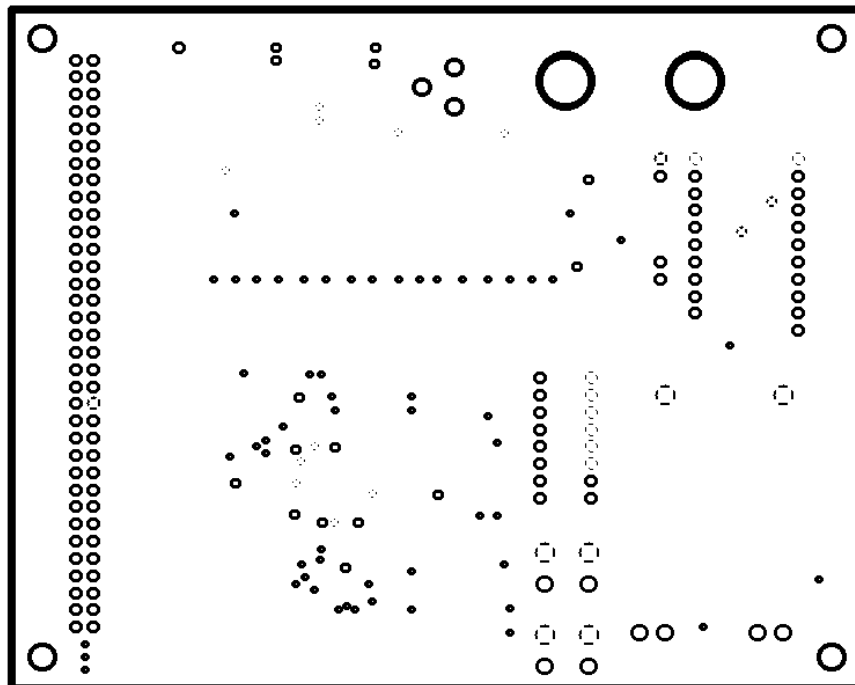
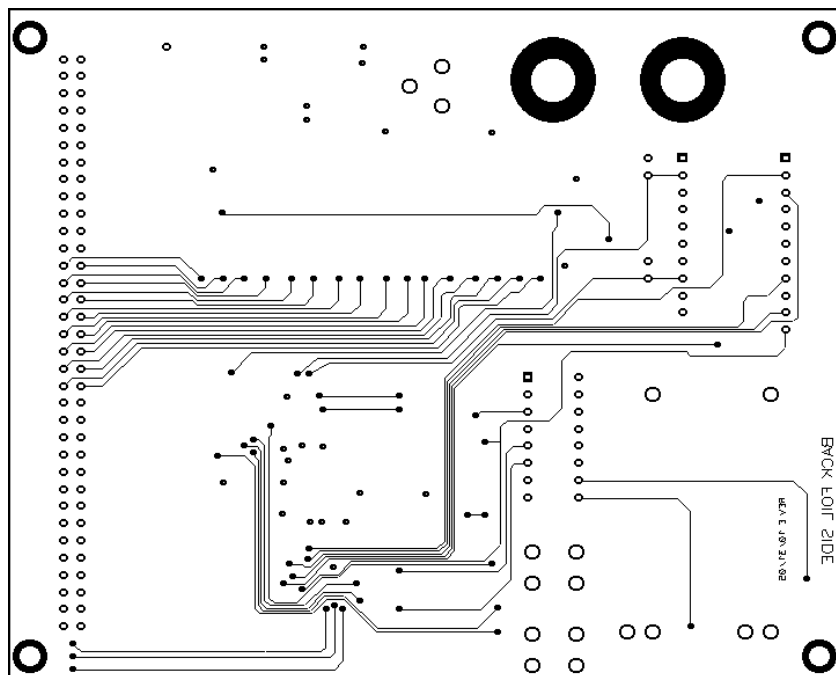


Figure 11. Solder-side Copper (Layer 4)




Component List

Quantity	Reference Designators	Description
2	C1, C2	10µF 10V tantalum cap, Nichicon F931A106MBA
8	C3 to C10	0.1µF 0603 SMD cap, Panasonic ECJ-1VB1C104K
1	D1	Schottky diode, International Rectifier MBRS130LTR
18	D2 to D19	Red LED, SMD1206 package, LiteOn LTST-C150KRKT
1	J1	5mm DC power connector, CUI PJ-102BH
1	J2	Banana Jack, red, SPC Technology 845-R
1	J3	Banana Jack, Black, SPC Technology 845-B
2	J4, J5	8-position pin header, Molex 22-28-4084
1	Q1	MMBT3904LT1 NPN transistor, On-Semiconductor
1	Q2	MMBT3906LT1 PNP transistor, On-Semiconductor
4	R1, R2, R3, R4	2K resistor network, CTS 768141202G
2	R5, R6, R11, R12	4.7K 5% 0805 resistor, Yageo 9C08052A4701JLHFT
2	R7, R8	35mm slide pot, 1K, Alpha-Taiwan RA3043-20-10EB1-B13
2	R9, R10	220 Ohm 5% 0805 resistor, Yageo RC0805JR-07220RL
2	S2, S3	Momentary switch, Panasonic EVQPAD04M
8	R13 to R20	1k ohm 5% 0805 resistor, Yageo 9C08052A1001JLHFT
1	S1	8-position dipswitch, CTS 206-8ST
1	U1	ispPAC-POWR1220AT8
1	U2	3.3V fixed regulator SOIC8, Texas Instruments TPS77733D
1	n/a	Printed circuit board, 4" x 5", 4-layer
4	n/a	Rubber feet, 3M SJ-5003

Related Literature

- ispPAC-POWR1220AT8 Data Sheet
- Lattice Application Note AN6067, *ispPAC-POWR1220AT8 I2C Hardware Verification Utility Users Guide*.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ispPAC Power Manager 1220AT8 Design System	PAC-SYSPWR1220AT8	

Technical Support Assistance

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Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
March 2007	01.2	Corrected silk screen error in the labeling of the VPS0 and VPS1 connections, located on the left side of the board at the 34 dual row set of interconnect holes. VPS1 is on the left and VPS0 is on the right. Added Ordering Information section.

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