NCV6356

Configurable 5.0 A AOT Step Down Converter

Description

The NCV6356 is a synchronous AOT (Adaptive On−time) buck converter optimized to supply the different sub systems of automotive applications post regulation system up to 5 V input. The device is able to deliver up to 5.0 A, with programmable output voltage from 0.6 V to 1.4 V. Operation at up to 2.4 MHz switching frequency allows the use of small components. Synchronous rectification and automatic PFM Pseudo−PWM (PPWM) transitions improve overall solution efficiency. The NCV6356 is in low profile 3.0 x 4.0 mm DFN−14 package.

Features

- Input Voltage Range from 2.5 V to 5.5 V : Battery, 3.3 V and 5.0 V Rail Powered Applications
- Power Capability : 3.0 A Ta = 105°C – 5.0 A Ta = 85°C
- Programmable Output Voltage : 0.6 V to 1.4 V in 6.25 mV Steps
- Up to 2.4 MHz Switching Frequency with On Chip Oscillator
- Uses 330 nH Inductor and at least 22 μF Capacitors for Optimized Footprint and Solution Thickness
- PFM/PPWM Operation for Optimum Efficiency
- Low 60 μA Quiescent Current
- I^2C Control Interface with Interrupt and Dynamic Voltage Scaling Support
- Enable / VSEL Pins, Power Good / Interrupt Signaling
- Thermal Protections and Temperature Management
- Transient Load Helper: Share the Same Rail with Another Rail
- 3.0 x 4.0 mm / 0.5 mm Pitch DFN 14 Package
- AEC−Q100 Qualified and PPAP Capable

Typical Applications

- Snap Dragon
- Automotive POL
- Instrumentation, Clusters
- Infotainment
- ADAS System (Vision, Radar)

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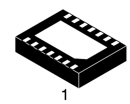
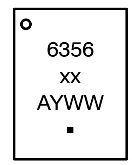


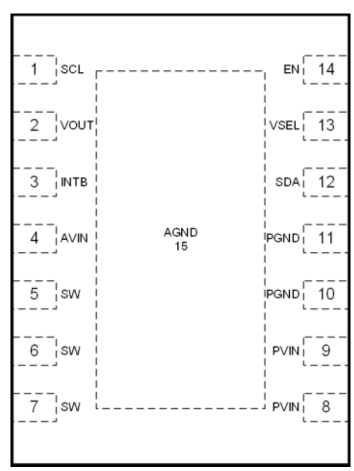
WDFNW14 4x3, 0.5P
CASE 511CM

MARKING DIAGRAM



6356	= Specific Device Code
xx	= C: 1.150 V / 1.150 V
	= B: 1.200 V / 1.200 V
	= Q: 0.875 V / 0.906 V
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package*

(Note: Microdot may be in either location)



(Top View)
14−Pin 0.50 mm pitch DFN

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 32 of this data sheet.

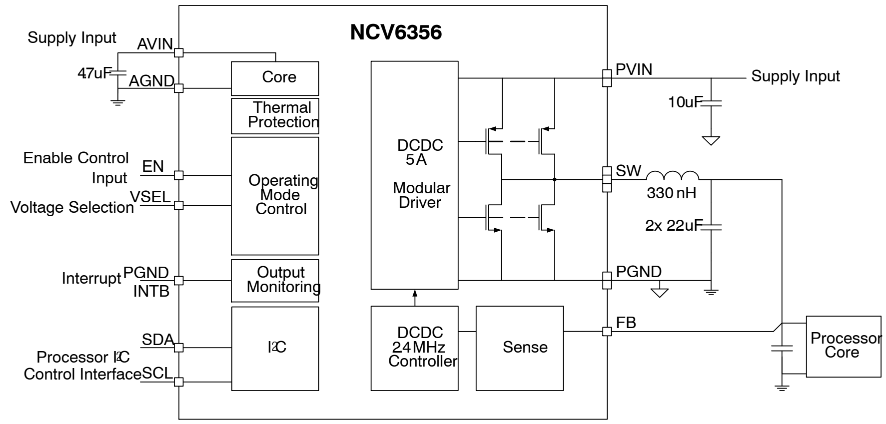


Figure 1. Typical Application Circuit

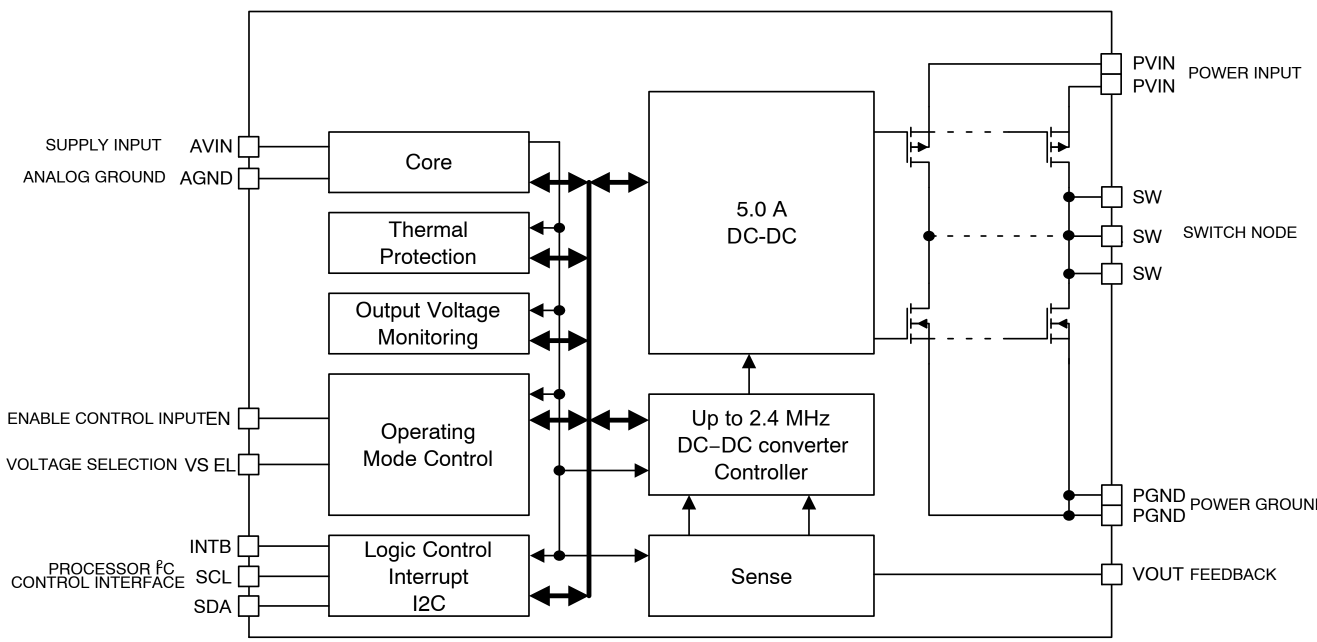


Figure 2. Simplified Block Diagram

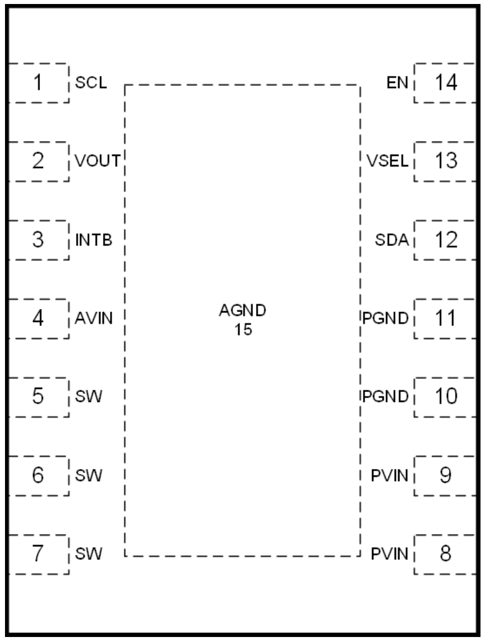


Figure 3. Pin Out (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
REFERENCE			
4	AVIN	Analog Input	**Analog Supply**. This pin is the device analog and digital supply. Could be connected directly to the VIN plane with a dedicated 4.7 μF ceramic capacitor. Must be equal to PVIN
15	AGND	Analog Ground	**Analog Ground**. Analog and digital modules ground. Must be connected to the system ground.
CONTROL AND SERIAL INTERFACE			
14	EN	Digital Input	**Enable Control**. Active high will enable the part. There is an internal pull down resistor on this pin.
13	VSEL	Digital Input	**Output voltage** / **Mode Selection**. The level determines which of two programmable configurations to utilize (operating mode / output voltage). There is an internal pull down resistor on this pin; could be left open if not used.
3	INTB	Digital Output	**Interrupt** open drain output. Must be connected to the ground plane if not used.
1	SCL	Digital Input	I^2C interface **Clock** line. There is an internal pull down resistor on this pin; could be left open if not used
12	SDA	Digital Input/Output	I^2C interface Bi−directional **Data** line. There is an internal pull down resistor on this pin; could be left open if not used
DC to DC CONVERTER			
8, 9	PVIN	Power Input	**Switch Supply**. These pins must be decoupled to ground by at least a 10 μF ceramic capacitor. It should be placed as close as possible to these pins. All pins must be used with short heavy connections. Must be equal to AVIN
5, 6, 7	SW	Power Output	**Switch Node**. These pins supply drive power to the inductor. Typical application uses 0.33 μH inductor; refer to application section for more information. All pins must be used with short heavy connections.
10, 11	PGND	Power Ground	**Switch Ground**. This pin is the power ground and carries the high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local ground plane that connects all PGND pins together is recommended. Analog and power grounds should only be connected together in one location with a trace.
2	VOUT	Analog Input	**Feedback Voltage Input**. Must be connected to the output capacitor positive terminal with a trace, not to a plane. This is the positive input to the error amplifier.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Analog and power pins (Note 1): AVIN, PVIN, SW, INTB, VOUT, DC non switching PVIN−PGND pins, transient 3 ns – 2.4 MHz	V_A	 −0.3 to +6.0 −0.3 to +7.5	V
I^2C pins: SDA, SCL	V_{I2C}	−0.3 to +6.0	V
Digital pins : EN, VSEL Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_A +0.3 ≤ 6.0 10	 V mA
Human Body Model (HBM) ESD Rating (Note 2)	ESD HBM	2500	V
Charged Device Model (CDM) ESD Rating (Note 2)	ESD CDM	1000	V
Latch Up Current: (Note 3) Digital Pins All Other Pins	I_{LU}	 100 100	mA
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Junction Temperature	T_{JMAX}	−40 to +150	°C
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series contains ESD protection and passes the following ratings:
   Human Body Model (HBM) ± 2.5 kV per JEDEC standard: JESD22 – A114.
   Charged Device Model (CDM) ± 1.0 kV per JEDEC standard: JESD22−C101 Class IV
3. Latch up Current per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AV_{IN}, PV_{IN}	Power Supply	$AV_{IN} = PV_{IN}$	2.5		5.5	V
T_J	Junction Temperature Range (Note 6)		−40	25	+125	°C
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Note 7)	DFN−14 on Demo−board	–	30	–	°C/W
P_D	Power Dissipation Rating (Note 8)	$T_A \le 105°C$, $R_{\theta JA} = 30°C/W$	–	666	–	mW
		$T_A \le 85°C$ $R_{\theta JA} = 30°C/W$	–	1333	–	mW
		$T_A = 65°C$ $R_{\theta JA} = 30°C/W$	–	2000	–	mW
L	Inductor for DC to DC converter (Note 5)		0.15	0.33	0.47	μH
Co	Output Capacitor for DC to DC Converter (Note 5)		15	–	200	μF
Cin	Input Capacitor for DC to DC Converter (Note 5)	Per 1.0 A of I_{OUT}	6.0	10.0	–	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Including de−ratings (Refer to the Application Information section of this document for further details)
6. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation
7. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a NCV6356EVB board. It is a multilayer board with 1−once internal power and ground planes and 2−once copper traces on top and bottom of the board
8. The maximum power dissipation (PD) is dependent on input voltage, maximum output current, pcb stack up and layout, and external components selected.

$$R_{\theta JA} = \frac{125 - T_A}{P_D}, \text{ by taking } R_{\theta JA} = 30°C$$

Table 4. ELECTRICAL CHARACTERISTICS (Note 9)
Min and Max Limits apply for T_J = −40°C to +125°C, AVIN = PVIN = 3.3 V and default configuration, unless otherwise specified.
Typical values are referenced to T_A = + 25°C, AVIN = PVIN = 3.3 V and default configuration, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Current: Pins AVIN – PVINx						
I_{Q-PPWM}	Operating quiescent current PPWM	DCDC active in Forced PPWM no load	–	22	25	mA
$I_{Q\ PFM}$	Operating quiescent current PFM	DCDC active in Auto mode no load – minimal switching	–	60	90	μA
I_{SLEEP}	Product sleep mode current	Product in sleep mode V_{IN} = 5.5 V, T_J up to 85°C	–	5	10	μA
I_{OFF}	Product in off mode	EN, VSEL and Sleep_Mode low, No I^2C pull up V_{IN} = 5.5 V, T_J up to 85°C	–	0.8	3	μA
DC to DC Converter						
PV_{IN}	Input Voltage Range		2.5	–	5.5	V
I_{OUT}	Load Current Range	NCV6356B and NCV6356C (Note 11, 12) Ipeak[1..0] = 00 Ipeak[1..0] = 01 Ipeak[1..0] = 10 Ipeak[1..0] = 11	 0 0 0 0	 – – – –	 3.5 4.0 4.5 5.0	A
		NCV6356Q (Note 11, 12) Ipeak[1..0] = 00 Ipeak[1..0] = 01 Ipeak[1..0] = 10 Ipeak[1..0] = 11	 0 0 0 0	 – – – –	 5.3 5.8 6.3 6.8	
ΔV_{OUT}	Output Voltage DC Error	Forced PPWM mode, V_{IN} range, No load	−1.5	–	1.5	%
		Forced PPWM mode, V_{IN} range, I_{OUT} up to I_{OUTMAX} (Note 11)	−2	–	2	
		Auto mode, V_{IN} range, I_{OUT} up to I_{OUTMAX} (Note 11)	−3	–	2	
F_{SW}	Switching Frequency		2.16	2.4	2.64	MHz
R_{ONHS}	P−Channel MOSFET On Resistance	From PVIN to SW V_{IN} = 5.0 V	–	38	50	mΩ
R_{ONLS}	N−Channel MOSFET On Resistance	From SW to PGND V_{IN} = 5.0 V	–	29	40	mΩ
I_{PK}	Peak Inductor Current	NCV6356B and NCV6356C Open loop – Ipeak[1..0] = 00 Open loop – Ipeak[1..0] = 01 Open loop – Ipeak[1..0] = 10 Open loop – Ipeak[1..0] = 11	 4.6 5.2 5.6 6.2	 5.2 5.8 6.2 6.8	 5.8 6.4 6.8 7.4	A
		NCV6356QM Open loop – Ipeak[1..0] = 00 Open loop – Ipeak[1..0] = 01 Open loop – Ipeak[1..0] = 10 Open loop – Ipeak[1..0] = 11	 6.4 7.2 7.6 8.4	 7.0 7.8 8.2 9.0	 7.7 8.4 8.8 9.6	
DC_{LOAD}	Load Regulation	I_{OUT} from 0 A to I_{OUTMAX} (Note 11) Forced PPWM mode	–	5	–	mV
DC_{LINE}	Line Regulation	2.5 V ≤ V_{IN} ≤ 5.5 V Forced PPWM mode	–	6	–	mV

Table 4. ELECTRICAL CHARACTERISTICS (Note 9)
Min and Max Limits apply for T_J = −40°C to +125°C, AVIN = PVIN = 3.3 V and default configuration, unless otherwise specified.
Typical values are referenced to T_A = + 25°C, AVIN = PVIN = 3.3 V and default configuration, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AC_{LOAD}	Transient Load Response	$t_r = t_f$ = 100 ns Load step 1.5 A (Note 11)	–	±20	–	mV
		NCV6356Q $t_r = t_f$ = 200 ns, V_{OUT} = 1.0 V L = 0.24 μH, C_{OUT} = 4 x 47 μF Load step 0.4A / 6.6 A (Note 11)	−60	50	67	
AC_{LINE}	Transient Line Response	$t_r = t_f$ = 10 μs Line step 3.3 V / 3.9 V (Note 11)	–	±20	–	mV
D	Maximum Duty Cycle		–	100	–	%
t_{START}	Turn on time	Time from EN transitions from Low to High to 90% of Output Voltage (DVS[1..0] = 00b)	–	100	130	Us
$R_{DISDCDC}$	DCDC Active Output Discharge	Vout = 1.15 V	–	12	20	Ω
EN, VSEL						
V_{IH}	High input voltage		1.05	–	–	V
V_{IL}	Low input voltage		–	–	0.4	V
T_{FTR}	Digital input X Filter	EN, VSEL rising and falling DBN_Time = 01 (Note 11)	0.5	–	4.5	μs
I_{PD}	Digital input X Pull−Down (input bias current)	For EN and VSEL pins	–	0.05	1.00	μA
INTB (Optional)						
V_{INTBL}	INTB low output voltage	I_{INT} = 5 mA	0	–	0.2	
V_{INTBH}	INTB high output voltage	Open drain	–	–	5.5	
$INTB_{LK}$	INTB leakage current	3.6V at INTB pin when INTB valid	–	–	100	
I^2C						
V_{I2CINT}	High level at SCL/SCA line		1.7	–	4.5	V
V_{I2CIL}	SCL, SDA low input voltage	SCL, SDA pin (Note 10)	–	–	0.4	V
V_{I2CIH}	SCL high input voltage	SCL pin (Note 10, 11)	1.6	–	–	V
	SDA high input voltage	SDA pin (Note 10, 11)	1.2	–	–	
V_{I2COL}	SDA low output voltage	I_{SINK} = 3 mA	–	–	0.4	V
F_{SCL}	I^2C clock frequency	(note 11)	–	–	3.4	MHz
TOTAL DEVICE						
V_{UVLO}	Under Voltage Lockout	V_{IN} falling	–	–	2.5	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	V_{IN} rising	60	–	200	mV
T_{SD}	Thermal Shut Down Protection		–	150	–	°C
$T_{WARNING}$	Warning Rising Edge		–	135	–	°C
T_{PWTH}	Pre – Warning Threshold	I^2C default value	–	105	–	°C
T_{SDH}	Thermal Shut Down Hysteresis		–	30	–	°C
$T_{WARNINGH}$	Thermal warning Hysteresis		–	15	–	°C
$T_{PWTH\ H}$	Thermal pre−warning Hysteresis		–	6	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
9. Refer to the Application Information Section of this data sheet for more details.
10. Devices that use non−standard supply voltages which do not conform to the intent I^2C bus system levels must relate their input levels to the V_{DD} voltage to which the pull−up resistors R_P are connected.
11. Guaranteed by design and characterized.
12. Junction temperature must be maintained below 125°C. Output load current capability depends on the application thermal capability.

Typical Operating Characteristics

$AV_{IN} = PV_{IN} = 3.3$ V, $T_J = +25°C$
DCDC=1.15 V, Ipeak =6.8 A (Unless otherwise noted). L=0.33 uH DFE252012F – Cout = 2 x 22uF 0603, Cin = 4.7 uF 0603.

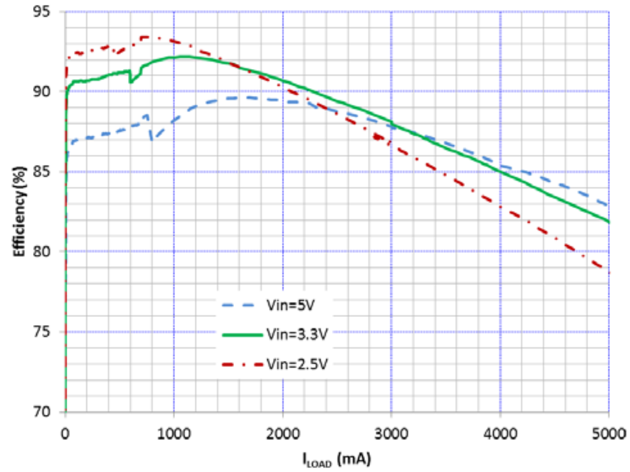


Figure 4. Efficiency vs I_{LOAD} and V_{IN}, V_{OUT} = 1.39375 V, SPM5030 Inductor

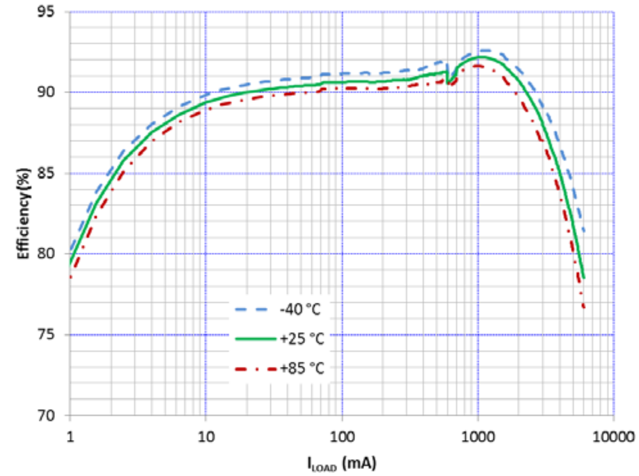


Figure 5. Efficiency vs I_{LOAD} and Temperature, V_{OUT} = 1.39375 V, SPM5030 Inductor

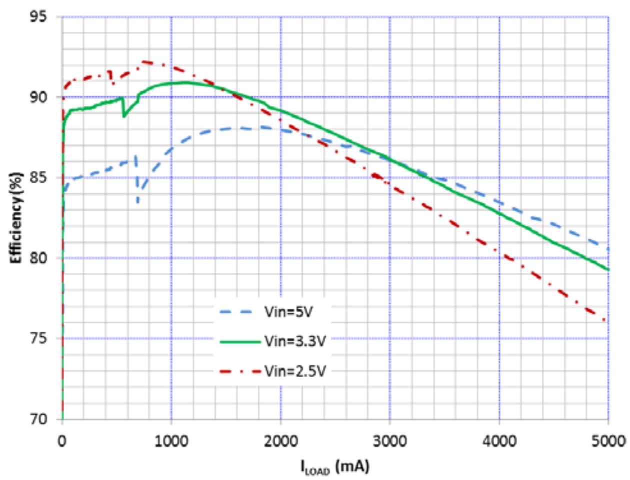


Figure 6. Efficiency vs I_{LOAD} and V_{IN}, V_{OUT} = 1.15 V, SPM5030 Inductor

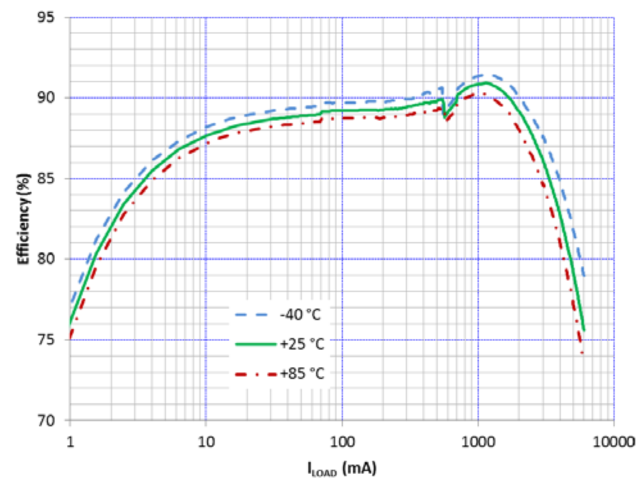


Figure 7. Efficiency vs I_{LOAD} and Temperature, V_{OUT} = 1.15 V, SPM5030 Inductor

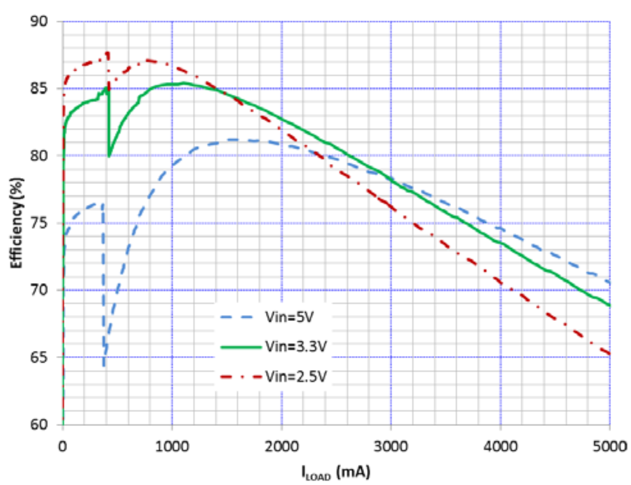


Figure 8. Efficiency vs I_{LOAD} and V_{IN}, V_{OUT} = 0.60 V, SPM5030 Inductor

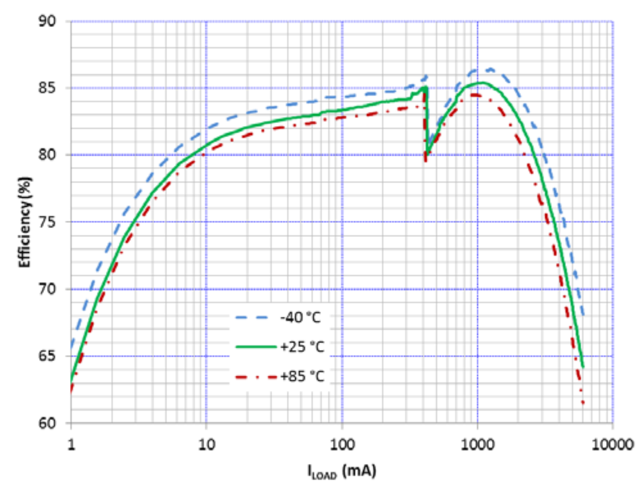


Figure 9. Efficiency vs I_{LOAD} and Temperature, V_{OUT} = 0.60 V, SPM5030 Inductor

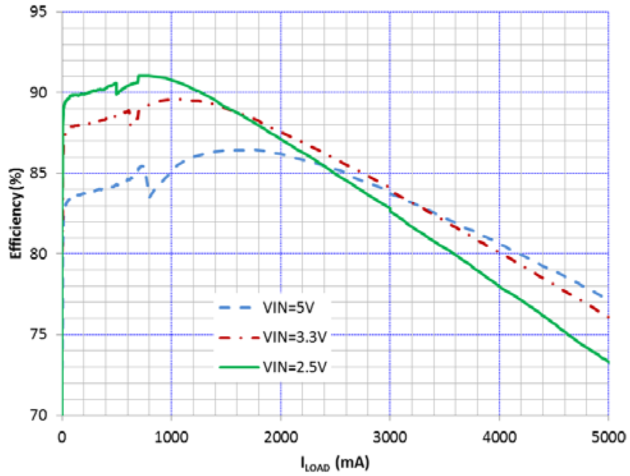


Figure 10. Efficiency vs I_{LOAD} and V_{IN}, V_{OUT} = 1.150 V

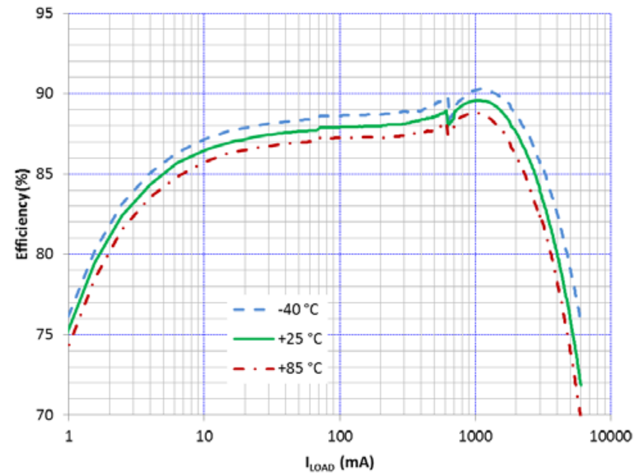


Figure 11. Efficiency vs I_{LOAD} and Temperature, V_{OUT} = 1.150 V

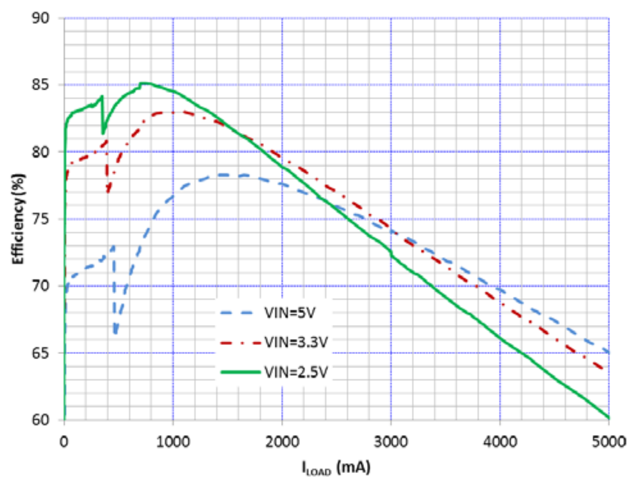


Figure 12. Efficiency vs I_{LOAD} and V_{IN}, V_{OUT} = 0.600 V

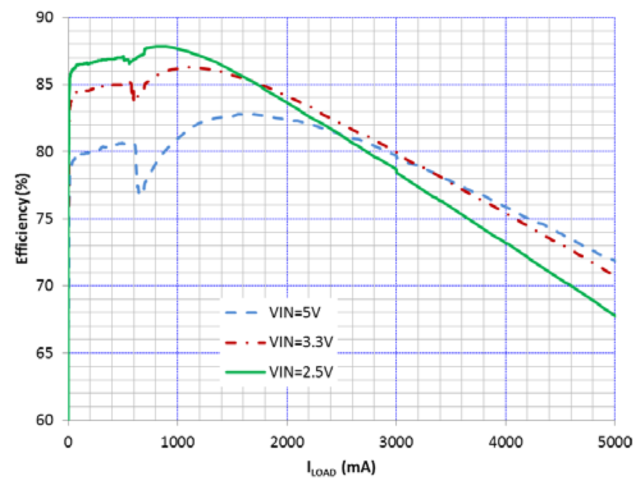


Figure 13. Efficiency vs I_{LOAD} and Temperature, V_{OUT} = 0.875 V, HEI201612A−R24M Inductor

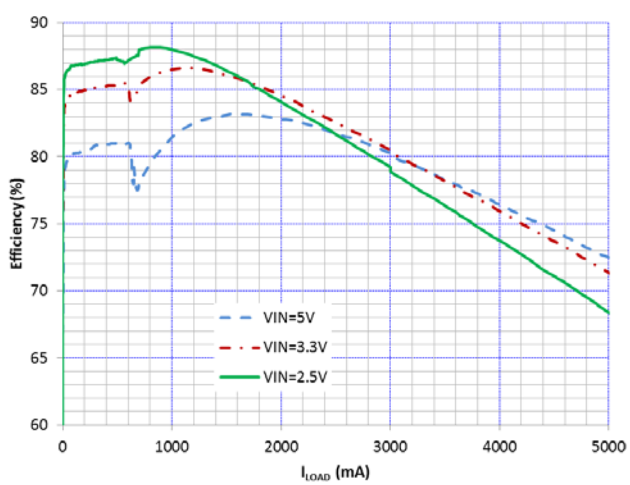


Figure 14. Efficiency vs I_{LOAD} and Temperature, V_{OUT} = 0.906 V, HEI201612A−R24M Inductor

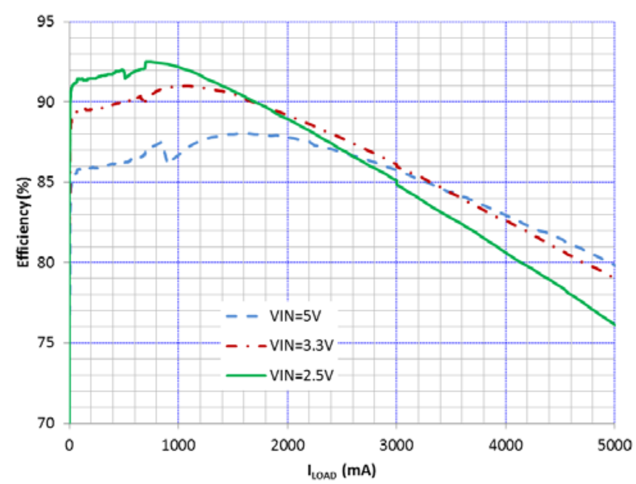


Figure 15. Efficiency vs I_{LOAD} and Temperature, V_{OUT} = 1.394 V

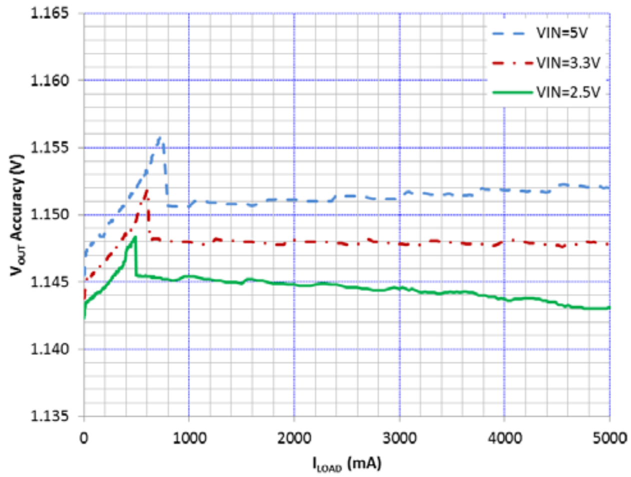


Figure 16. V_{OUT} Accuracy vs I_{LOAD} and V_{IN}, V_{OUT} = 1.150 V

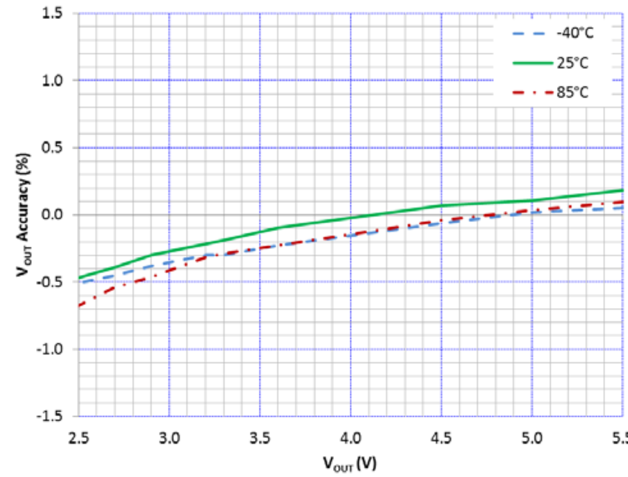


Figure 17. V_{OUT} Accuracy vs V_{IN} and Temperature, V_{OUT} = 1.150 V

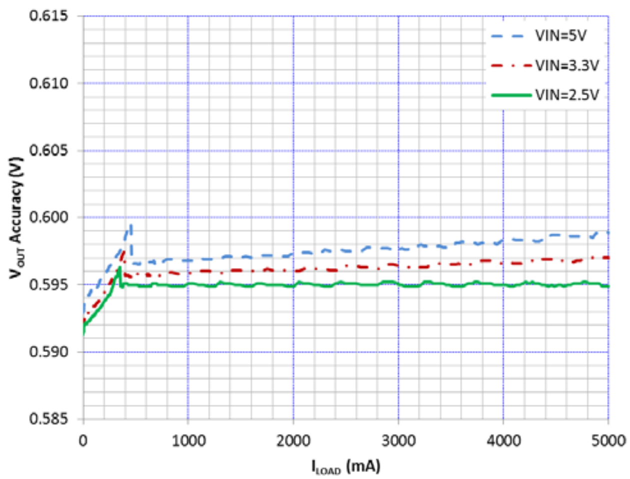


Figure 18. V_{OUT} Accuracy vs I_{LOAD} and V_{IN}, V_{OUT} = 0.600 V

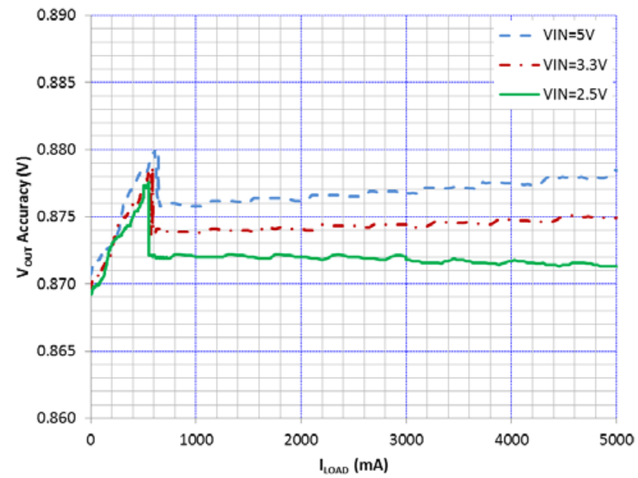


Figure 19. V_{OUT} Accuracy vs I_{LOAD} and V_{IN}, V_{OUT} = 0.875 V, HEI201612A−R24M Inductor

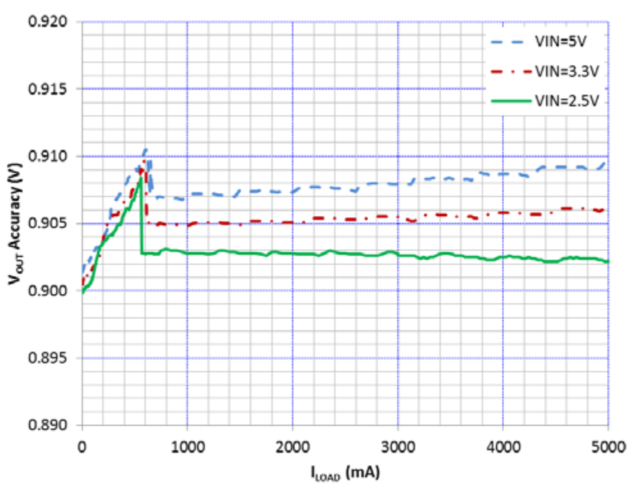


Figure 20. V_{OUT} Accuracy vs I_{LOAD} and V_{IN}, V_{OUT} = 0.906 V, HEI201612A−R24M Inductor

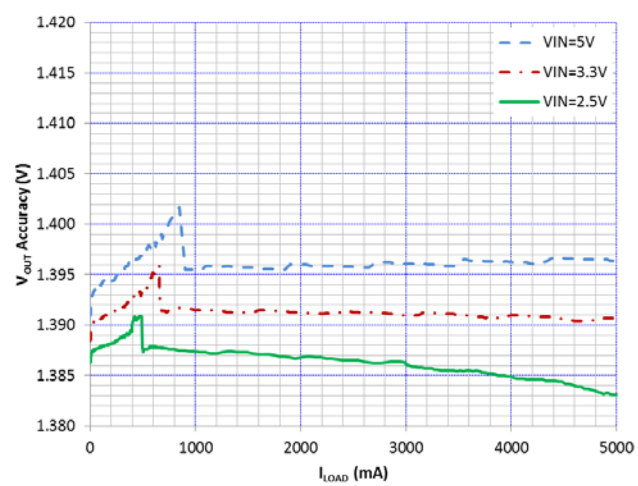


Figure 21. V_{OUT} Accuracy vs I_{LOAD} and V_{IN}, V_{OUT} = 1.394 V

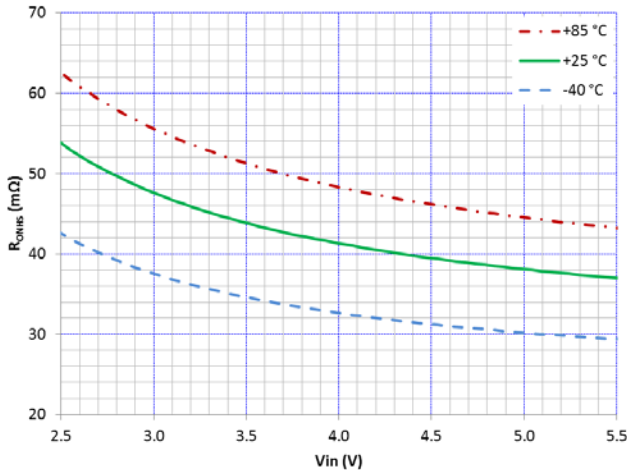


Figure 22. HSS R_{ON} vs V_{IN} and Temperature

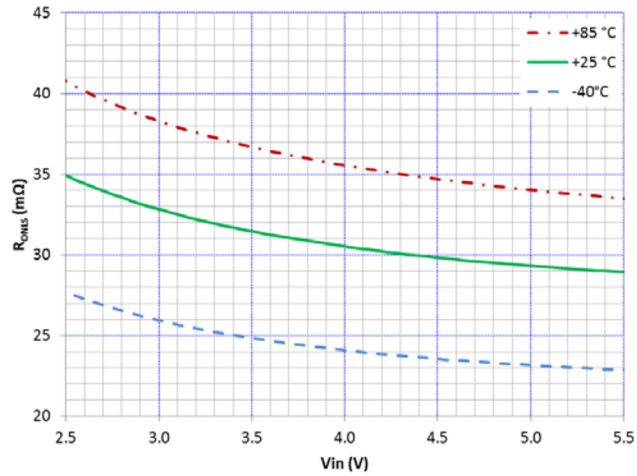


Figure 23. LSS R_{ON} vs V_{IN} and Temperature

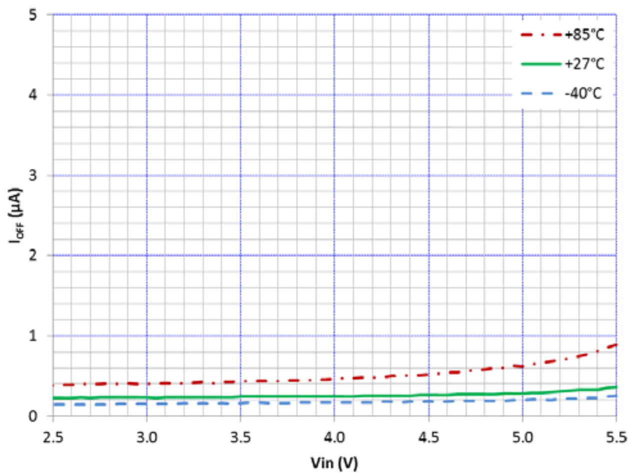


Figure 24. I_{OFF} vs V_{IN} and Temperature

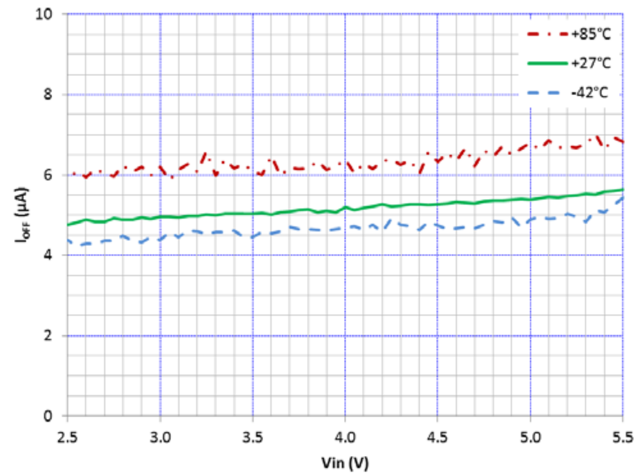


Figure 25. I_{SLEEP} vs V_{IN} and Temperature

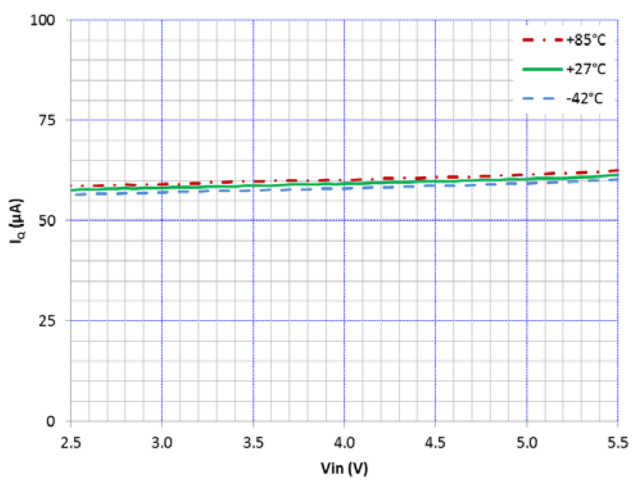


Figure 26. I_{QPFM} vs V_{IN} and Temperature

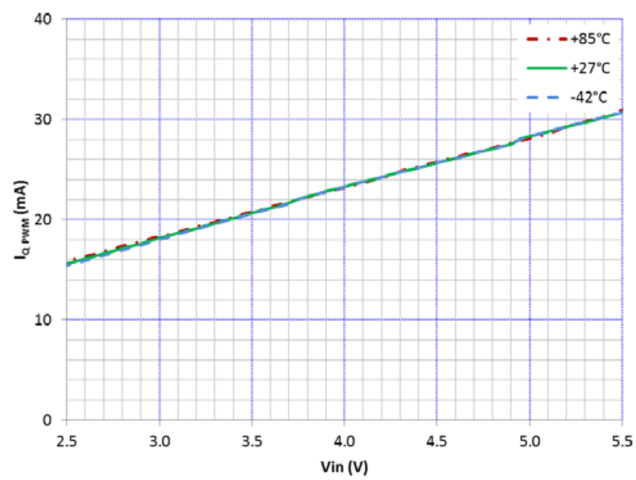


Figure 27. I_{QPPWM} vs V_{IN} and Temperature

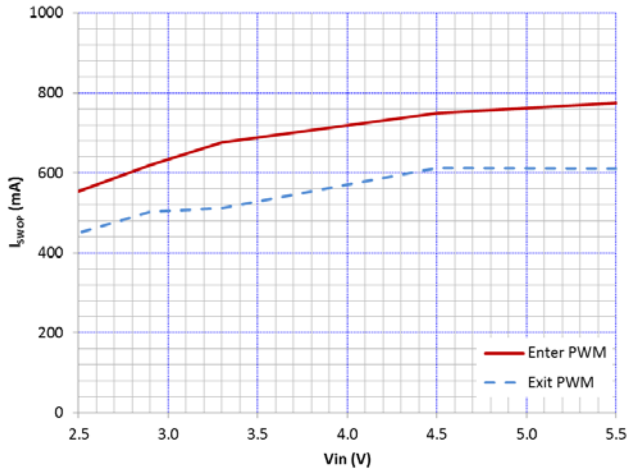


Figure 28. Switchover Point V_{OUT} = 1.15 V

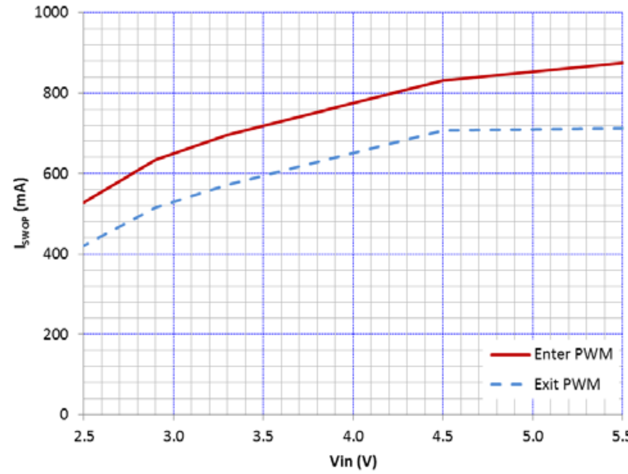


Figure 29. Switchover Point V_{OUT} = 1.4 V

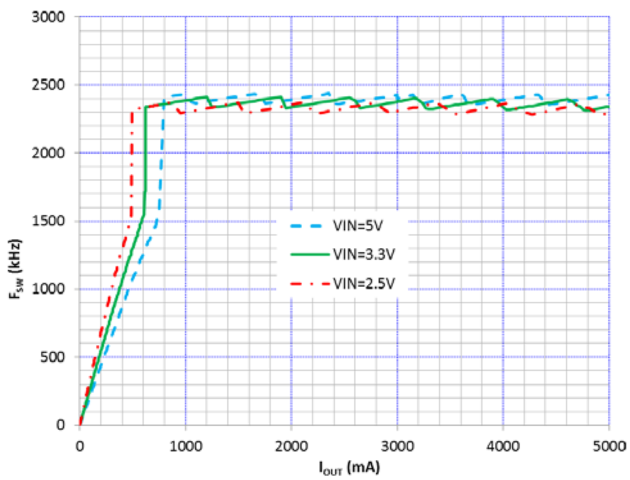


Figure 30. Switching Frequency vs I_{LOAD} and V_{IN}, V_{OUT} = 1.150 V

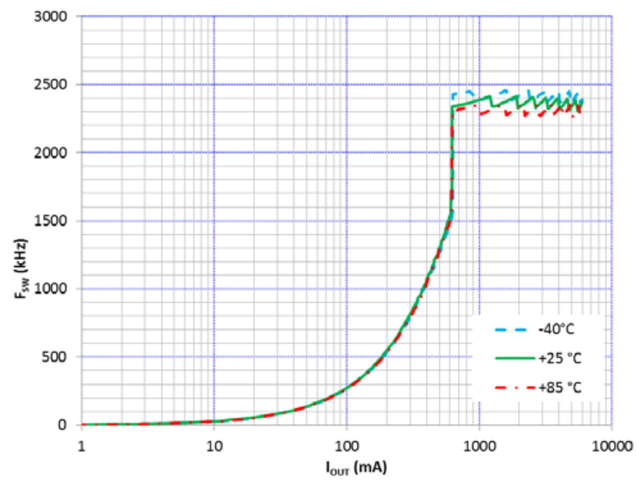


Figure 31. Switching Frequency vs I_{LOAD} and Temperature, V_{OUT} = 1.150 V

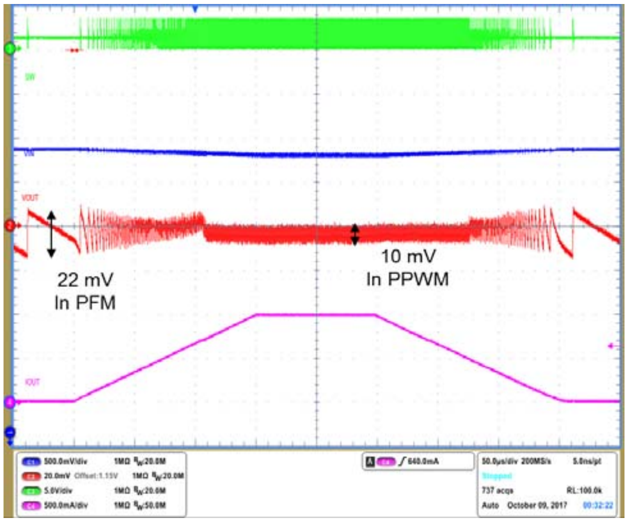


Figure 32. Ripple

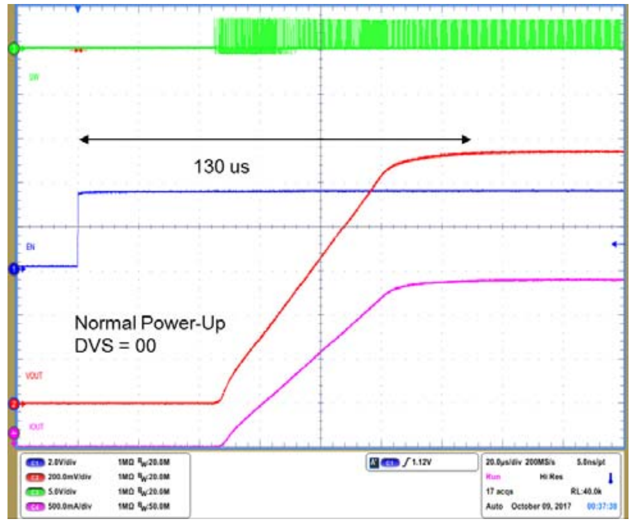


Figure 33. Normal Power Up, V_{OUT} = 1.15 V, DVS[1..0] = 00

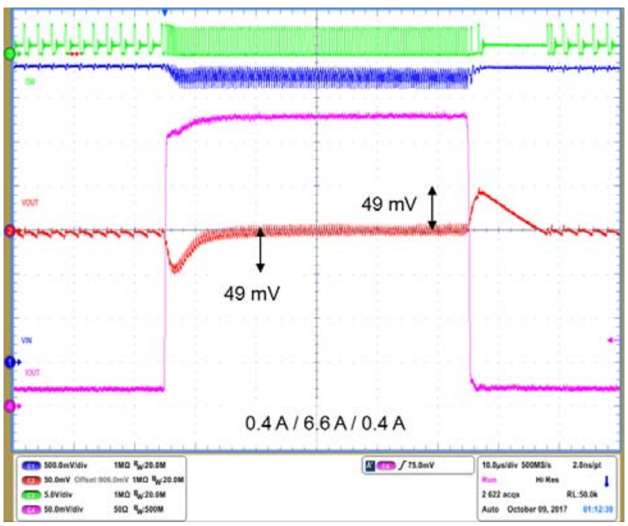


Figure 34. Transient Load 0.4 to 6.6 A − Auto Mode, V_{IN} = 3.3 V − V_{OUT} = 1.0 V − L = 0.24 uH − C_{OUT} = 4 x 47 uF

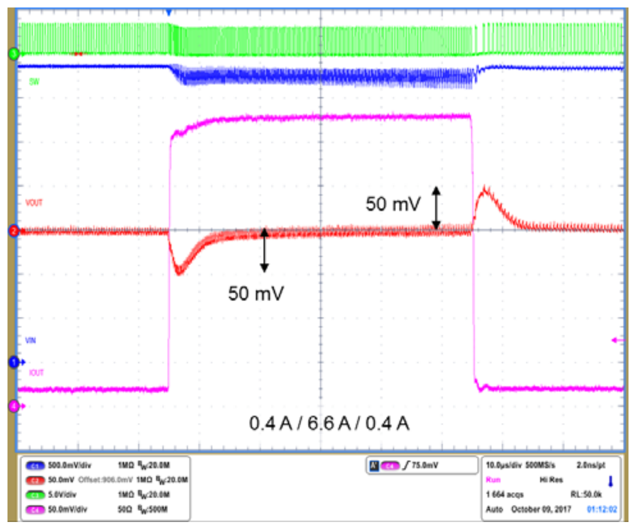


Figure 35. Transient Load 0.4 to 6.6 A − Forced PPWM, V_{IN} = 3.3 V − V_{OUT} = 1.0 V − L = 0.24 uH − C_{OUT} = 4 x 47 uF

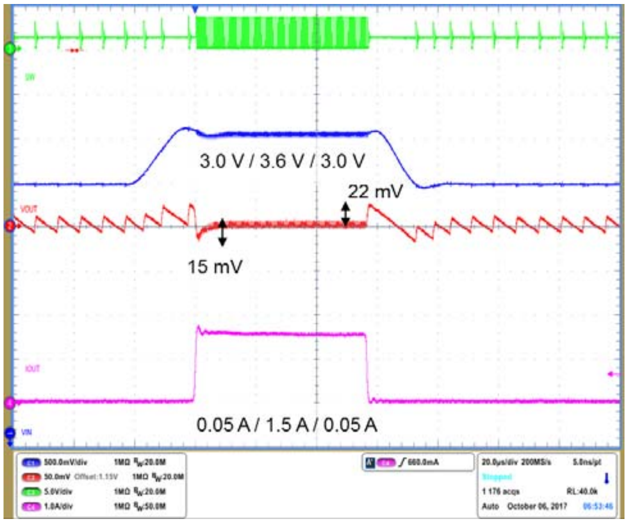


Figure 36. Transient Load 0.05 to 1.5 A, Transient Line 3.0 − 3.6 V Auto Mode

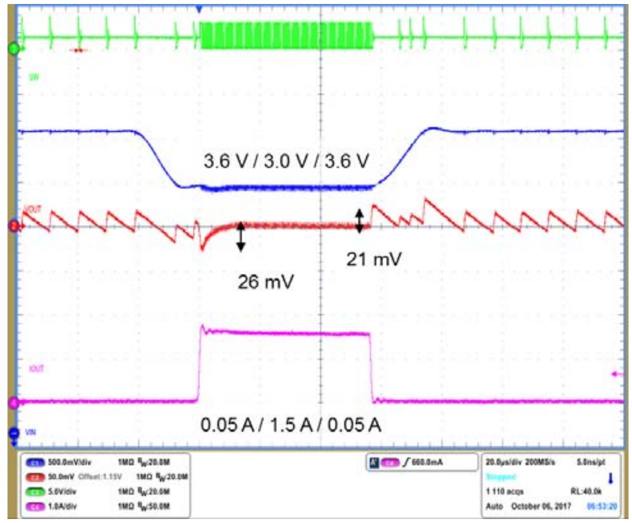


Figure 37. Transient Load 0.05 to 1.5 A, Transient Line 3.6 − 3.0 V Auto Mode

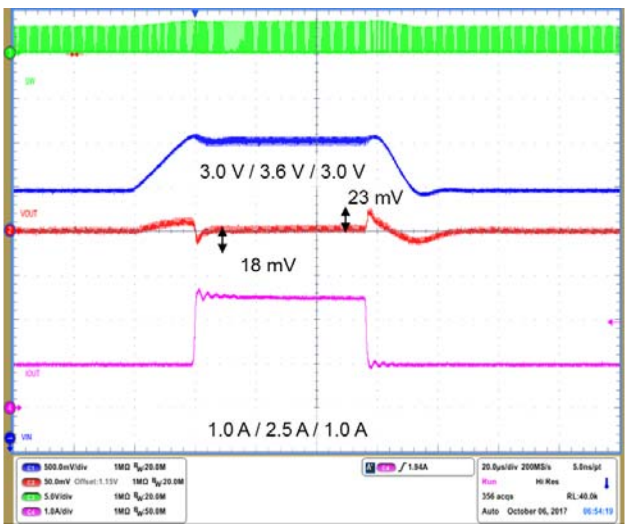


Figure 38. Transient Load 1 to 2.5 A, Transient Line 3.0 − 3.6 V Auto Mode

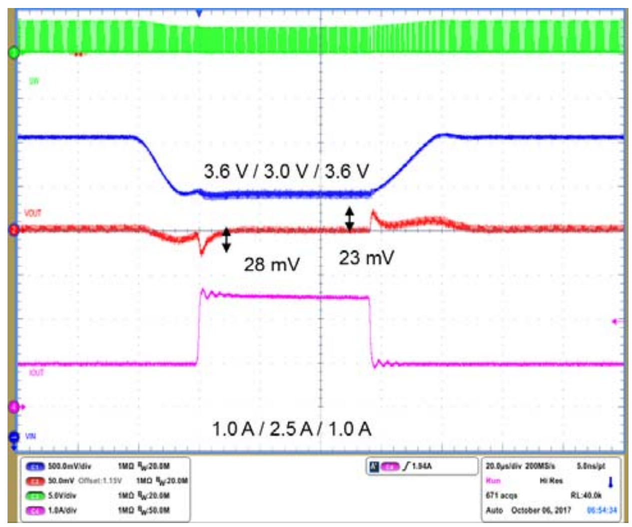


Figure 39. Transient Load 1 to 2.5 A, Transient Line 3.6 − 3.0 V Auto Mode

DETAILED OPERATING DESCRIPTION

Detailed Descriptions

The NCV6356 is voltage mode stand−alone DC to DC converter optimized to supply different sub systems of automotive applications post regulation system up to 5 V input. It can deliver up to 5 A at an I^{2}C selectable voltage ranging from 0.6 V to 1.40 þV. The switching frequency up to 2.4 MHz allows the use of small output filter components. Power Good indicator and Interrupt management are available. Operating modes, configuration, and output power can be easily selected either by using digital I/O pins or by programming a set of registers using an I^{2}C compatible interface capable of operation up to 3.4 MHz.

Default I^{2}C settings are factory programmable.

DC to DC Converter Operation

The converter integrates both high side and low side (synchronous) switches. Neither external transistors nor diodes are required for NCV6356 operation. Feedback and compensation network are also fully integrated.

It uses the AOT (Adaptive On−Time) control scheme and can operate in two different modes: PFM and PPWM (Pseudo−PWM). The transition between modes can occur automatically or the switcher can be placed in forced PPWM mode by I^{2}C programming (PPWMVSEL0 / PPWMVSEL1 bits of COMMAND register).

PPWM (Pseudo Pulse Width Modulation) Operating Mode

In medium and high load conditions, NCV6356 operates in PPWM mode to regulate the desired output voltage. In this mode, the inductor current is in CCM (Continuous Conduction Mode) and the AOT guaranties a pseudo−fixed frequency with 10% accuracy. The internal N−MOSFET switch operates as synchronous rectifier and is driven complementary to the P−MOSFET switch.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads, the NCV6356 operates in PFM mode as the inductor current drops into DCM (Discontinuous Conduction Mode). The upper FET on−time is kept constant and the switching frequency becomes proportional to the loading current. As it does in PPWM mode, the internal N−MOSFET operates as a synchronous rectifier after each P−MOSFET on−pulse until there is no longer current in the coil.

When the load increases and the current in the inductor become continuous again, the controller automatically turns back to PPWM mode.

Forced PPWM

The NCV6356 can be programmed to only use PPWM and the transition to PFM can be disabled if so desired, thanks to the PPWMVSEL0 or PPWMVSEL1 I^{2}C bits (COMMAND register).

Output Stage

NCV6356 is a 3.5 A to 5.0 A output current capable DC to DC converter with both high side and low side (synchronous) switches integrated.

Inductor Peak Current Limitation / Short Protection

During normal operation, peak current limitation monitors and limits the inductor current by checking the current in the P−MOSFET switch. When this current exceeds the Ipeak threshold, the P−MOSFET is immediately opened.

To protect again excessive load or short circuit, the number of consecutive Ipeak is counted. When the counter reaches 16, the DCDC is powered down during about 2 ms and the ISHORT interrupt is flagged. It will re−start following the REARM bit in the LIMCONF register:

- If REARM = 0, then NCV6356 does not re−start automatically, an EN pin toggle is required.
- If REARM = 1, NCV6356 re−starts automatically after the 2 ms with register values set prior the fault condition.

This current limitation is particularly useful to protect the inductor. The peak current can be set by writing IPEAK[1..0] bits in the LIMCONF register.

Table 5. IPEAK VALUES

OPN	IPEAK[1..0]	Inductor Peak Current (A)
NCV6356B NCV6356C	00	5.2 – for 3.5 output current
	01	5.8 – for 4.0 output current
	10	6.2 – for 4.5 output current
	11	6.8 – for 5.0 output current
NCV6356Q	00	7.0 – for 5.3 output current
	01	7.7 – for 5.8 output current
	10	8.2 – for 6.3 output current
	11	8.8 – for 6.8 output current

Output Voltage

The output voltage is set internally by an integrated resistor bridge and no extra components are needed to set the output voltage. Writing in the VoutVSEL0[6..0] bits of the PROGVSEL0 register or VoutVSEL1[6..0] bits of the PROGVSEL1 register will change the output voltage. The output voltage level can be programmed by 6.26 mV steps between 0.6 V to 1.39375 V. The VSEL pin and VSELGT bit will determine which register between PROGVSEL0 and PROGVSEL1 will set the output voltage.

- If VSELGT = 1 AND VSEL=0 → Output voltage is set by VoutVSEL0[6..0] bits (PROGVSEL0 register)
- Else → Output voltage is set by VoutVSEL1[6..0] bits (PROGVSEL1 register)

Under Voltage Lock Out (UVLO)

NCV6356 core does not operate for voltages below the Under Voltage Lock Out (UVLO) level. Below the UVLO threshold, all internal circuitry (both analog and digital) is held in reset. NCV6356 operation is guaranteed down to UVLO as the battery voltage is dropping off. To avoid erratic on / off behavior, a maximum 200 mV hysteresis is implemented. Restart is guaranteed at 2.7 V when the VBAT voltage is recovering or rising.

Thermal Management

Thermal Shut Down (TSD)

The thermal capability of the NCV6356 can be exceeded due to the step down converter output stage power level. A thermal protection circuitry with associated interrupt is therefore implemented to prevent the IC from damage. This protection circuitry is only activated when the core is in active mode (output voltage is turned on). During thermal shut down, output voltage is turned off.

During thermal shut down, the output voltage is turned off.

When NCV6356 returns from thermal shutdown, it can re−start in 2 different configurations depending on the REARM bit in the LIMCONF register (refer to the register description section):

- If REARM = 0 then NCV6356 does not re−start after TSD. To restart, an EN pin toggle is required.
- If REARM = 1, NCV6356 re−starts with register values set prior to thermal shutdown.

The thermal shut down threshold is set at 150°C (typical) and a 30°C hysteresis is implemented in order to avoid erratic on / off behavior. After a typical 150°C thermal shut down, NCV6356 will resume to normal operation when the die temperature cools to 120°C.

Thermal Warnings

In addition to the TSD, the die temperature monitoring circuitry includes a thermal warning and thermal pre−warning sensor and interrupts. These sensors can inform the processor that NCV6356 is close to its thermal shutdown and preventive measures to cool down die temperature can be taken by software.

The Warning threshold is set by hardware to 135°C typical. The Pre−Warning threshold is set by default to 105°C but it can be changed by setting the TPWTH[1..0] bits in the LIMCONF register.

Active Output Discharge

To make sure that no residual voltage remains in the power supply rail when disabled, an active discharge path can ground the NCV6356 output voltage. For maximum flexibility, this feature can be easily disabled or enabled with the DISCHG bit in the PGOOD register. By default the discharge path is enabled and is activated during the first 100 µs after battery insertion.

Enabling

The EN pin controls NCV6356 start up. EN pin Low to High transition starts the power up sequencer. If EN is low, the DC to DC converter is turned off and device enters:

- Sleep Mode if Sleep_Mode I^{2}C bit is high or VSEL is high or I^{2}C pull up present,
- Off Mode if Sleep_Mode I^{2}C bit and VSEL are low and no I^{2}C pull up.

When EN pin is set to a high level, the DC to DC converter can be enabled / disabled by writing the ENVSEL0 or ENVSEL1 bit of the PROGVSEL0 and PROGVSEL1 registers:

- Enx I^{2}C bit is high, the DC to DC converter is activated.
- Enx I^{2}C is low, the DC to DC converter is turned off and the device enters in Sleep Mode.

A built in pull down resistor disables the device when this pin is left unconnected or not driven. EN pin activity does not generate any digital reset.

Power Up Sequence (PUS)

In order to power up the circuit, the input voltage AVIN has to rise above the VUVLO threshold. This triggers the internal core circuitry power up which is the “Wake Up Time” (including “Bias Time”)

This delay is internal and cannot be bypassed. EN pin transition within this delay corresponds to the “Initial power up sequence” (IPUS):

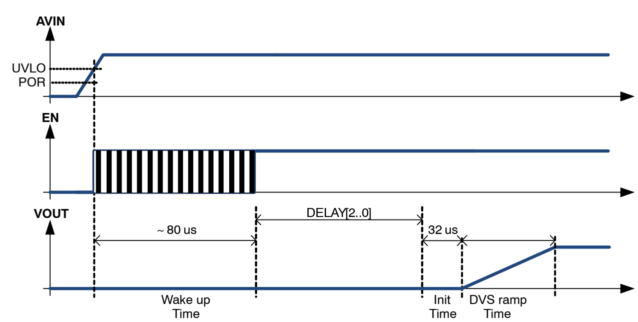


Figure 40. Initial Power Up Sequence

In addition a user programmable delay will also take place between the Wake Up Time and the Init time: The DELAY[2..0] bits of the TIME register will set this user programmable delay with a 2 ms resolution. With default delay of 0 ms, the NCV6356 IPUS takes roughly 100 µs, and the DC to DC converter output voltage will be ready within 150 µs.

The power up output voltage is defined by the VSEL state.

NOTE: During the Wake Up time, the I^{2}C interface is not active. Any I^{2}C request to the IC during this time period will result in a NACK reply.

Normal, Quick and Fast Power Up Sequence

The previous description applies only when the EN transitions during the internal core circuitry power up (Wake up and calibration time). Otherwise 3 different cases are possible:

- Enabling the part by setting the EN pin from Off Mode will result in “Normal power up sequence” (NPUS, with DELAY;[2..0]).
- Enabling the part by setting the EN pin from Sleep Mode will result in “Quick power up sequence” (QPUS, with DELAY;[2..0]).
- Enabling the DC to DC converter, whereas EN is already high, either by setting the ENVSEL0 or ENVSEL1 bits or by VSEL pin transition will results in “Fast power up sequence” (FPUS, without DELAY[2..0]).

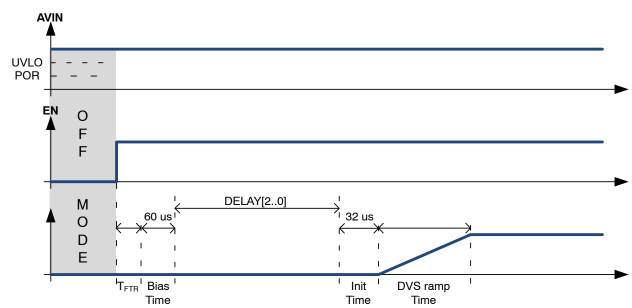


Figure 41. Normal Power Up Sequence

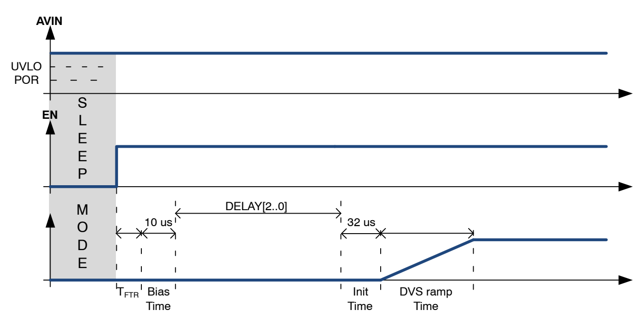


Figure 42. Quick Power Up Sequence

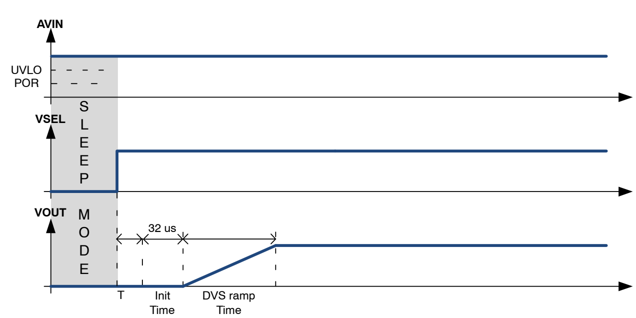


Figure 43. Fast Power Up Sequence

In addition the delay set in DELAY[2..0] bits in TIME register will apply only for the EN pins turn ON sequence (NPUS and QPUS).

The power up output voltage is defined by VSEL state.

DC to DC Converter Shut Down

When shutting down the device, no shut down sequence is required. The output voltage is disabled and, depending on the DISCHG bit state of the PGOOD register, the output may be discharged.

DC to DC converter shutdown is initiated by either grounding the EN pin (Hardware Shutdown) or, depending on the VSEL internal signal level, by clearing the ENVSEL0 or ENVSEL1 bits (Software shutdown) in the PROGVSEL0 or PROGVSEL1 registers.

In hardware shutdown (EN = 0), the internal core is still active and I^{2}C accessible.

The internal core of the NCV6356 shuts down when AVIN falls below UVLO.

Dynamic Voltage Scaling (DVS)

The NCV6356 supports dynamic voltage scaling (DVS) allowing the output voltage to be reprogrammed via I^{2}C commands and provides the different voltages required by the processor. The change between set points is managed in a smooth fashion without disturbing the operation of the processor.

When programming a higher voltage, the output raises with controlled dV/dt defined by DVS[1..0] bits in the TIME register. When programming a lower voltage the output voltage will decrease accordingly. The DVS step is fixed and the speed is programmable.

The DVS sequence is automatically initiated by changing the output voltage settings. There are two ways to change these settings:

- Directly change the active setting register value (VoutVSEL0[6..0] of the PROGVSEL0 register or VoutVSEL1[6..0] of the PROGVSEL1 register) via an I^{2}C command
- Change the VSEL internal signal level by toggling the VSEL pin.

The second method eliminates the I^{2}C latency and is therefore faster.

The DVS transition mode can be changed with the DVSMODE bit in the COMMAND register:

- In forced PPWM mode when accurate output voltage control is needed. Rise and fall time are controlled with the DVS[1..0] bits.

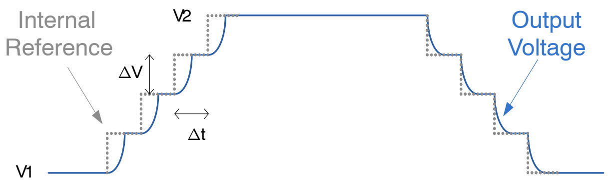


Figure 44. DVS in Forced PPWM Mode Diagram

- In Auto mode when the output voltage must not be discharged. Rise time is controlled by the DVS[1..0], and fall time depends of the load and cannot be faster than the DVS[1..0] settings.

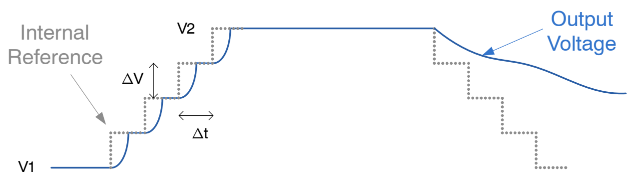


Figure 45. DVS in Auto Mode Diagram

Power Good Indicator

To indicate the output voltage level is established, a power good signal is available. The power good signal is low when the DC to DC converter is off. Once the output voltage reaches 95% of the expected output level, the power good logic signal becomes high (ACK_PG, SEN_PG bits).

During operation, when the output drops below 90% of the programmed level, the power good logic signal goes low, indicating a power failure. When the voltage rises again to above 95%, the power good signal goes high again.

During a DVS sequence, the Power Good signal is set low during the transition and goes back high once the transition is completed.

The Power Good signal during normal operation can be disabled by clearing the PGDCDC bit in the PGOOD register. The Power good operation during DVS can be activated with PGDVS bit if the PGOOD register.

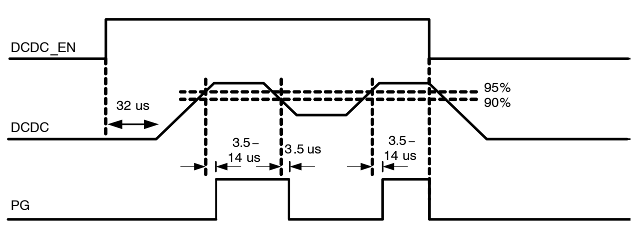


Figure 46. Power Good Signal when PGDCDC = 1

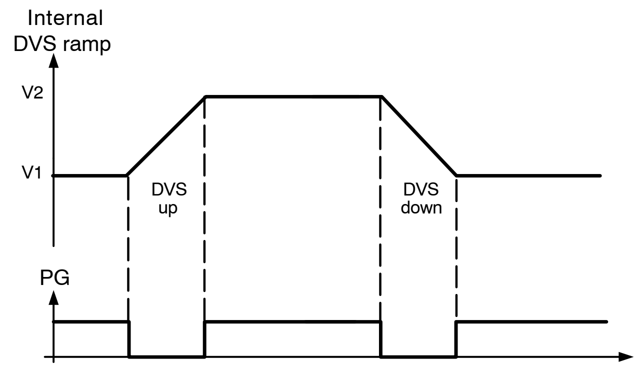


Figure 47. Power Good during DVS Transition

Digital IO Settings

VSEL Pin

By changing VSEL pin levels, the user has a latency free way to change NCV6356 configuration: operating mode (Auto or PWM forced), the output voltage as well as enable.

Table 6. VSEL PIN PARAMETERS

Parameter VSEL Pin Can Set	REGISTER VSEL = LOW	REGISTER VSEL = HIGH
ENABLE	ENVSEL0 PROGVSEL0[7]	ENVSEL1 PROGVSEL1[7]
VOUT	VoutVSEL0[6..0]	VoutVSEL1[6..0]
OPERATING MODE (Auto / PPWM Forced)	PWMVSEL0 COMMAND[7]	PWMVSEL1 COMMAND[6]

VSEL pin action can be masked by writing 0 to the VSELGT bit in the COMMAND register. In that case I^2C bit corresponding to VSEL high will be taken into account.

EN pin

The EN pin can be gated by writing the ENVSEL0 or ENVSEL1 bits of the PROGVSEL0 and PROGVSEL1 registers, depending on which register is activated by the VSEL internal signal.

Interrupt Pin (Optional)

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected (dual edge monitoring).

Table 7. INTERRUPT SOURCES

Interrupt Name	Description
TSD	Thermal Shut Down
TWARN	Thermal Warning
TPREW	Thermal Pre Warning
UVLO	Under Voltage Lock Out
IDCDC	DC to DC converter Current Over / below limit
ISHORT	DC to DC converter Short−Circuit Protection
PG	Power Good

Individual bits generating interrupts will be set to 1 in the INT_ACK register (I^2C read only registers), indicating the interrupt source. INT_ACK register is automatically reset by an I^2C read. The INT_SEN register (read only register) contains real time indicators of interrupt sources.

All interrupt sources can be masked by writing in the register INT_MSK. Masked sources will never generate an interrupt request on the INTB pin.

The INTB pin is an open drain output. A non−masked interrupt request will result in the INTB pin being driven low.

When the host reads the INT_ACK registers the INTB pin is released to high impedance and the interrupt register INT_ACK is cleared.

Figure 48 is an example of a TWARN event of the INTB pin with INT_SEN/INT_MSK/INT_ACK and an I^2C read access behavior.

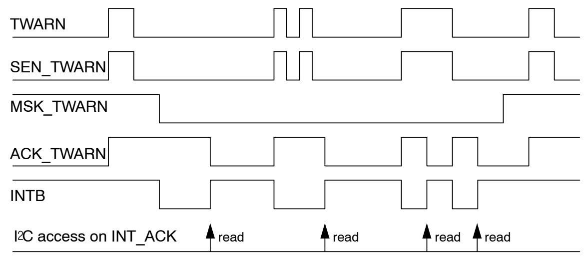


Figure 48. TWARN Interrupt Operation Example

Configurations

Default output voltages, enables, DCDC modes, current limit and other parameters can be factory programmed upon request.

Below is the default configurations pre−defined:

Table 8. NCV6356 CONFIGURATION

Configuration	5.0 A NCV6356CM	5.0 A NCV6356BM	6.8 A NCV6356QM
Default I^2C address PID product identification RID revision identification FID feature identification	ADD1 – 14h : 0010100R/W 20h Metal 00h	ADD1 – 14h : 0010100R/W 20h Metal 01h	ADD6 – 68h : 1101000R/W 20h Metal 02h
Default VOUT – VSEL=1	1.15 V	1.20 V	0.90625 V
Default VOUT – VSEL=0	1.15 V	1.20 V	0.875 V
Default MODE – VSEL=1	Forced PPWM	Forced PPWM	Forced PPWM
Default MODE – VSEL=0	Auto mode	Auto mode	Forced PPWM
Default IPEAK	6.8 A	6.8 A	8.8 A
OPN	NCV6356CMTWTXG	NCV6356BMTWTXG	NCV6356QMTWTXG
Marking	6356C	6356B	6356Q

I²C Compatible Interface

NCV6356 can support a subset of the I²C protocol as detailed below.

I²C Communication Description

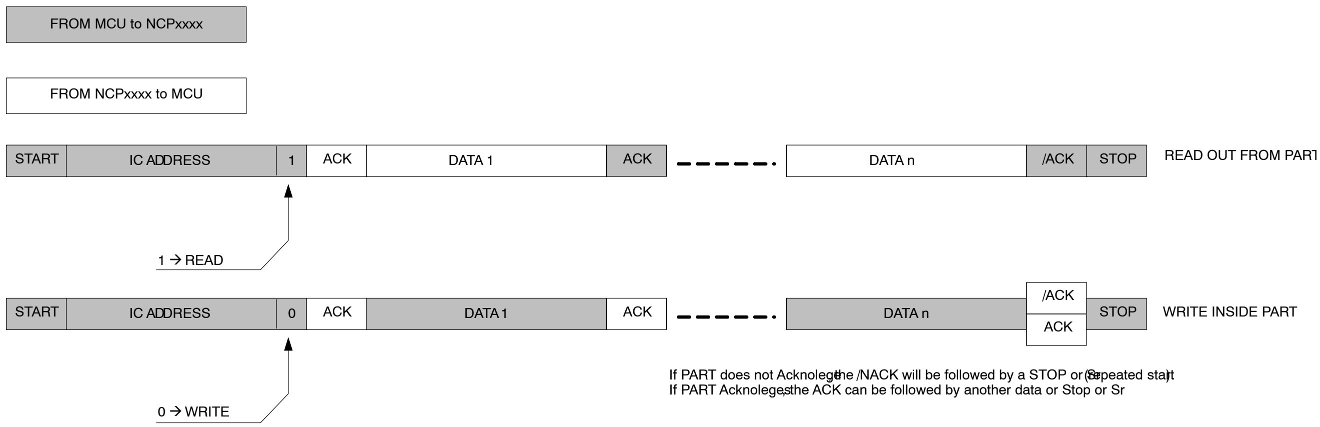


Figure 49. General Protocol Description

The first byte transmitted is the Chip address (with the LSB bit set to 1 for a read operation, or set to 0 for a Write operation). The following data will be:

- During a Write operation, the register address (@REG) is written in followed by the data. The writing process is auto−incremental, so the first data will be written in @REG, the contents of @REG are incremented and the next data byte is placed in the location pointed to by @REG + 1 ..., etc.
- During a Read operation, the NCV6356 will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto−incremental.

Read Sequence

The Master will first make a "Pseudo Write" transaction with no data to set the internal address register. Then, a stop then start or a Repeated Start will initiate the read transaction from the register address the initial write transaction has pointed to:

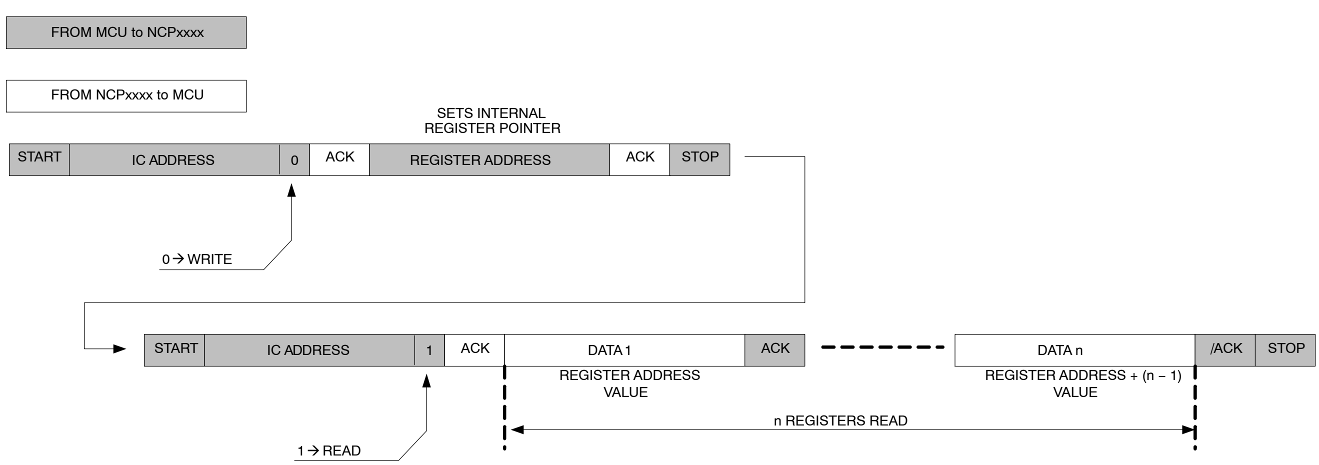


Figure 50. Read Sequence

The first WRITE sequence will set the internal pointer to the register that is selected. Then the read transaction will start at the address the write transaction has initiated.

Write Sequence

Write operation will be achieved by only one transaction. After chip address, the REG address has to be set, then following data will be the data we want to write in REG, REG + 1, REG + 2, ..., REG +n.

Write n Registers:

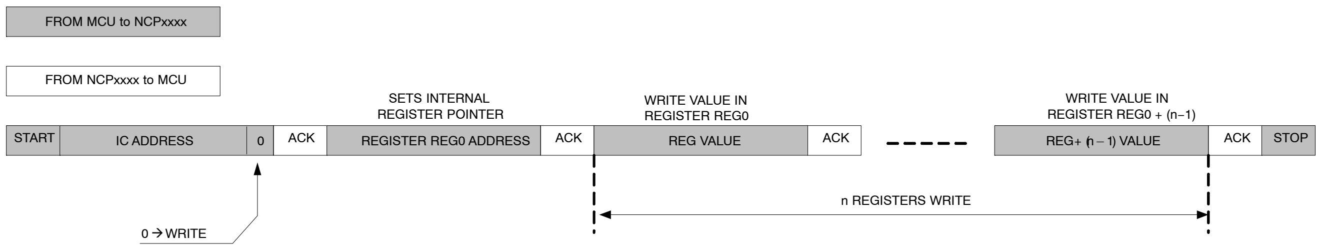


Figure 51. Write Sequence

Write then Read Sequence

With Stop Then Start

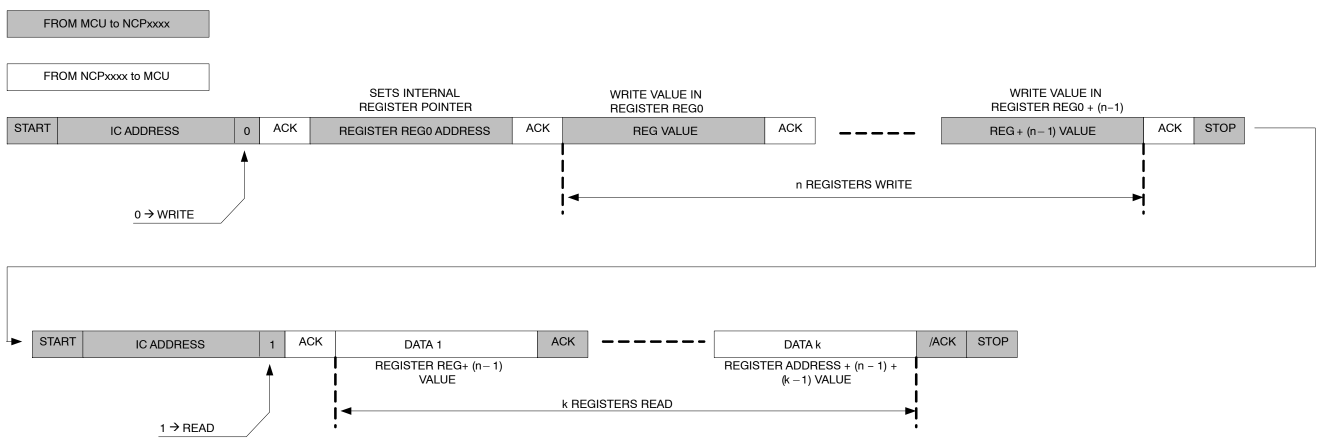


Figure 52. Write Followed by Read Transaction

I²C Address

The NCV6356 has 8 available I²C addresses selectable by factory settings (ADD0 to ADD7). Different address settings can be generated upon request to ON Semiconductor. See Table 8 (NCV6356 Configuration) for the default I²C address.

Table 9. I²C ADDRESS

I²C Address	Hex	A7	A6	A5	A4	A3	A2	A1	A0
ADD0	W 0x20 R 0x21	0	0	1	0	0	0	0	R/W
	Add	0x10							–
ADD1	W 0x28 R 0x29	0	0	1	0	1	0	0	R/W
	Add	0x14							–
ADD2	W 0x30 R 0x31	0	0	1	1	0	0	0	R/W
	Add	0x18							–
ADD3	W 0x38 R 0x39	0	0	1	1	1	0	0	R/W
	Add	0x1C							–
ADD4	W 0xC0 R 0xC1	1	1	0	0	0	0	0	R/W
	Add	0x60							–
ADD5	W 0xC8 R 0xC9	1	1	0	0	1	0	0	R/W
	Add	0x64							–
ADD6	W 0xD0 R 0xD1	1	1	0	1	0	0	0	R/W
	Add	0x68							–
ADD7	W 0xD8 R 0xD9	1	1	0	1	1	0	0	R/W
	Add	0x6C							–

Register Map

The tables below describe the I²C registers.

Registers / bits Operations:

R	Read only register
RC	Read then Clear
RW	Read and Write register
Reserved	Address is reserved and register / bit is not physically designed
Spare	Address is reserved and register / bit is physically designed

Table 10. I²C REGISTERS MAP CONFIGURATION (NCV6356C)

Add.	Register Name	Type	Def.	Function
00h	INT_ACK	RC	00h	Interrupt register
01h	INT_SEN	R	01h	Sense register (real time status)
02h	INT_MSK	RW	FFh	Mask register to enable or disable interrupt sources (trim)
03h	PID	R	20h	Product Identification
04h	RID	R	Metal	Revision Identification
05h	FID	R	00h	Features Identification (trim)
06h to 0Fh	–	–	–	Reserved for future use
10h	PROGVSEL1	RW	D8h	Output voltage settings and EN for VSEL pin = High (trim)
11h	PROGVSEL0	RW	D8h	Output voltage settings and EN for VSEL pin = Low (trim)
12h	PGOOD	RW	10h	Power good and active discharge settings (trim)
13h	TIME	RW	09h	Enabling and DVS timings (trim)
14h	COMMAND	RW	43h	Enabling and Operating mode Command register (trim)
15h	–	–	–	Reserved for future use
16h	LIMCONF	RW	E3h	Reset and limit configuration register (trim)
17h to 1Fh	–	–	–	Reserved for future use
20h to FFh	–	–	–	Reserved. Test Registers

Table 11. I²C REGISTERS MAP CONFIGURATION (NCV6356B)

Add.	Register Name	Type	Def.	Function
00h	INT_ACK	RC	00h	Interrupt register
01h	INT_SEN	R	01h	Sense register (real time status)
02h	INT_MSK	RW	FFh	Mask register to enable or disable interrupt sources (trim)
03h	PID	R	20h	Product Identification
04h	RID	R	Metal	Revision Identification
05h	FID	R	01h	Features Identification (trim)
06h to 0Fh	–	–	–	Reserved for future use
10h	PROGVSEL1	RW	E0h	Output voltage settings and EN for VSEL pin = High (trim)
11h	PROGVSEL0	RW	E0h	Output voltage settings and EN for VSEL pin = Low (trim)
12h	PGOOD	RW	10h	Power good and active discharge settings (trim)
13h	TIME	RW	09h	Enabling and DVS timings (trim)
14h	COMMAND	RW	43h	Enabling and Operating mode Command register (trim)
15h	–	–	–	Reserved for future use
16h	LIMCONF	RW	E3h	Reset and limit configuration register (trim)
17h to 1Fh	–	–	–	Reserved for future use
20h to FFh	–	–	–	Reserved. Test Registers

Table 12. I²C REGISTERS MAP CONFIGURATION (NCV6356Q)

Add.	Register Name	Type	Def.	Function
00h	INT_ACK	RC	00h	Interrupt register
01h	INT_SEN	R	01h	Sense register (real time status)
02h	INT_MSK	RW	FFh	Mask register to enable or disable interrupt sources (trim)
03h	PID	R	20h	Product Identification
04h	RID	R	Metal	Revision Identification
05h	FID	R	02h	Features Identification (trim)
06h to 0Fh	–	–	–	Reserved for future use
10h	PROGVSEL1	RW	B1h	Output voltage settings and EN for VSEL pin = High (trim)
11h	PROGVSEL0	RW	ACh	Output voltage settings and EN for VSEL pin = Low (trim)
12h	PGOOD	RW	10h	Power good and active discharge settings (trim)
13h	TIME	RW	09h	Enabling and DVS timings (trim)
14h	COMMAND	RW	C3h	Enabling and Operating mode Command register (trim)
15h	–	–	–	Reserved for future use
16h	LIMCONF	RW	E3h	Reset and limit configuration register (trim)
17h to 1Fh	–	–	–	Reserved for future use
20h to FFh	–	–	–	Reserved. Test Registers

Registers Description

Table 13. INTERRUPT ACKNOWLEDGE REGISTER

Name: INTACK				Address: 00h			
Type: RC				**Default: 00000000b (00h)**			
Trigger: Dual Edge [D7..D0]							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
ACK_TSD	ACK_TWARN	ACK_TPREW	Spare = 0	ACK_ISHORT	ACK_UVLO	ACK_IDCDC	ACK_PG

Bit	Bit Description
ACK_PG	Power Good Sense Acknowledgement 0: Cleared 1: DCDC Power Good Event detected
ACK_IDCDC	DCDC Over Current Sense Acknowledgement 0: Cleared 1: DCDC Over Current Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected
ACK_ISHORT	DCDC Short−Circuit Protection Sense Acknowledgement 0: Cleared 1: DCDC Short circuit protection detected
ACK_TPREW	Thermal Pre Warning Sense Acknowledgement 0: Cleared 1: Thermal Pre Warning Event detected
ACK_TWARN	Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected

Table 14. INTERRUPT SENSE REGISTER

Name: INTSEN				Address: 01h			
Type: R				Default: 00000000b (00h)			
Trigger: N/A							
D7	D6	D5	D4	D3	D2	D1	D0
SEN_TSD	SEN_TWARN	SEN_TPREW	Spare = 0	SEN_ISHORT	SEN_UVLO	SEN_IDCDC	SEN_PG

Bit	Bit Description
SEN_PG	Power Good Sense 0: DCDC Output Voltage below target 1: DCDC Output Voltage within nominal range
SEN_IDCDC	DCDC over current sense 0: DCDC output current is below limit 1: DCDC output current is over limit
SEN_UVLO	Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold
SEN_ISHORT	DCDC Short−Circuit Protection Sense 0: Short−Circuit detected not detected 1: Short−Circuit not detected
SEN_TPREW	Thermal Pre Warning Sense 0: Junction temperature below thermal pre−warning limit 1: Junction temperature over thermal pre−warning limit
SEN_TWARN	Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit
SEN_TSD	Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit

Table 15. INTERRUPT MASK REGISTER

Name: INTMSK				Address: 02h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	D6	D5	D4	D3	D2	D1	D0
MSK_TSD	MSK_TWARN	MSK_TPREW	Spare = 1	MSK_ISHORT	MSK_UVLO	MSK_IDCDC	MASK_PG

Bit	Bit Description
MSK_PG	Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_IDCDC	DCDC over current interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVLO	Under Voltage interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ISHORT	DCDC Short−Circuit Protection source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TPREW	Thermal Pre Warning interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TWARN	Thermal Warning interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TSD	Thermal Shutdown interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 16. PRODUCT ID REGISTER

Name: PID				Address: 03h			
Type: R				Default: 00011011b (20h)			
Trigger: N/A				Reset on N/A			
D7	D6	D5	D4	D3	D2	D1	D0
PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Table 17. REVISION ID REGISTER

Name: RID				Address: 04h			
Type: R				Default: Metal			
Trigger: N/A							
D7	D6	D5	D4	D3	D2	D1	D0
RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Bit	Bit Description
RID[7..0]	Revision Identification 00000000: First Silicon 00000001: Final Silicon

Table 18. FEATURE ID REGISTER

Name: FID				Address: 05h			
Type: R				Default: See Register map			
Trigger: N/A							
D7	D6	D5	D4	D3	D2	D1	D0
Spare	Spare	Spare	Spare	FID_3	FID_2	FID_1	FID_0

Bit	Bit Description
FID[3..0]	Feature Identification 00000000: NCV6356C 5.0 A, 1.15 V configuration 00000001: NCV6356B 5.0 A, 1.20 V configuration 00000010: NCV6356Q 6.8 A, 0.875 V – 0.906 V configuration

Table 19. DC TO DC VOLTAGE PROG (VSEL = 1) REGISTER

Name: PROGVSEL1				Address: 10h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	D6	D5	D4	D3	D2	D1	D0
ENVSEL1	VoutVSEL1[6..0]						

Bit	Bit Description
VoutVSEL1[6..0]	Sets the DC to DC converter output voltage when VSEL pin = 1 and VSEL pin function is enabled in register COMMAND.D0, or when VSEL pin function is disabled in register COMMAND.D0 0000000b = 600 mV – 1111111b = 1393.75 mV (steps of 6.25 mV)
ENVSEL1	EN Pin Gating for VSEL internal signal = High 0: Disabled 1: Enabled

Table 20. DC TO DC VOLTAGE PROG (VSEL = 0) REGISTER

Name: PROGVSEL0				Address: 11h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	D6	D5	D4	D3	D2	D1	D0
ENVSEL0	VoutVSEL0[6..0]						

Bit	Bit Description
VoutVSEL0[6..0]	Sets the DC to DC converter output voltage when VSEL pin = 0 and VSEL pin function is enabled in register COMMAND.D0 0000000b = 600 mV – 1111111b = 1393.75 mV (steps of 6.25 mV)
ENVSEL0	EN Pin Gating for VSEL internal signal = Low 0: Disabled 1: Enabled

Table 21. POWER GOOD REGISTER

Name: PGOOD				**Address: 12h**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	Spare = 0	Spare = 0	DISCHG	Spare = 0	Spare = 0	PGDVS	PGDCDC

Bit	Bit Description
PGDCDC	Power Good Enabling 0 = Disabled 1 = Enabled
PGDVS	Power Good Active On DVS 0 = Disabled 1 = Enabled
DISCHG	Active discharge bit Enabling 0 = Discharge path disabled 1 = Discharge path enabled

Table 22. TIMING REGISTER

Name: TIME				**Address: 13h**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DELAY[2..0]			DVS[1..0]		Spare = 0	DBN_Time[1..0]	

Bit	Bit Description
DBN_Time[1..0]	EN and VSEL debounce time 00 = No debounce 01 = 1–2 us 10 = 2–3 us 11 = 3–4 us
DVS[1..0]	DVS Speed 00 = 6.25 mV step / 0.333 us 01 = 6.25 mV step / 0.666 us 10 = 6.25 mV step / 1.333 us 11 = 6.25 mV step / 2.666 us
DELAY[2..0]	Delay applied upon enabling (ms) 000b = 0 ms – 111b = 14 ms (Steps of 2 ms)

Table 23. COMMAND REGISTER

Name: COMMAND				Address: 14h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PPWMVSEL0	PPWMVSEL1	DVSMODE	Sleep_Mode	Spare = 0	Spare = 0	Spare	VSELGT

Bit	Bit Description
VSELGT	VSEL Pin Gating 0 = Disabled 1 = Enabled
Sleep_Mode	Sleep mode 0 = Low Iq mode when EN and VSEL low 1 = Force product in sleep mode (when EN and VSEL are low)
DVSMODE	DVS transition mode selection 0 = Auto 1 = Forced PPWM
PPWMVSEL1	Operating mode for MODE internal signal = High 0 = Auto 1 = Forced PPWM
PPWMVSEL0	Operating mode for MODE internal signal = Low 0 = Auto 1 = Forced PPWM

Table 24. LIMITS CONFIGURATION REGISTER

Name: LIMCONF				Address: 16h			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IPEAK[1..0]		TPWTH[1..0]		Spare = 0	FORCERST	RSTSTATUS	REARM

Bit	Bit Description
REARM	Rearming of device after TSD / ISHORT 0: No re−arming after TSD / ISHORT 1: Re−arming active after TSD / ISHORT with no reset of I^2C registers: new power−up sequence is initiated with previously programmed I^2C registers values
RSTSTATUS	Reset Indicator Bit 0: Must be written to 0 after register reset 1: Default (loaded after Registers reset)
FORCERST	Force Reset Bit 0 = Default value. Self cleared to 0 1: Force reset of internal registers to default
TPWTH[1..0]	Thermal pre−Warning threshold settings 00 = 83°C 01 = 94°C 10 = 105°C 11 = 116°C
IPEAK	Inductor peak current settings 00 = 5.2 A (for 3.5 A output current) 01 = 5.8 A (for 4.0 A output current) 10 = 6.2 A (for 4.5 A output current) 11 = 6.8 A (for 5.0 A output current)

APPLICATION INFORMATION

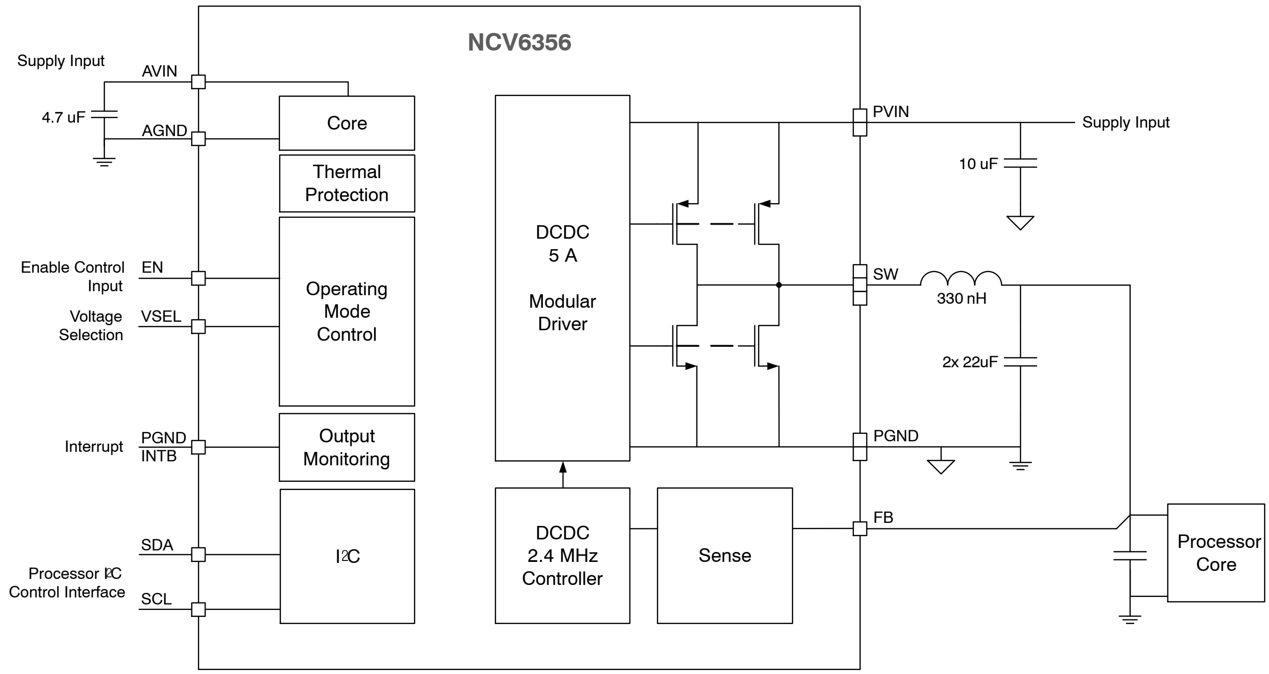


Figure 53. Typical Application Schematic

Output Filter Considerations

The output filter introduces a double pole in the system at a frequency of:

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}}$$

The NCV6356 internal compensation network is optimized for a typical output filter comprising a 330 nH inductor and 47 uF capacitor as describes in the basic application schematic in Figure 53.

Voltage Sensing Considerations

In order to regulate the power supply rail, the NCV6356 must sense its output voltage. The IC can support two sensing methods:

- Normal sensing: The FB pin should be connected to the output capacitor positive terminal (voltage to regulate).
- Remote sensing: The power supply rail sense should be made close to the system powered by the NCV6356. The voltage to the system is more accurate, since the PCB line impedance voltage drop is within the regulation loop. In this case, we recommend connecting the FB pin to the system decoupling capacitor positive terminal.

Components Selection

Inductor Selection

The inductance of the inductor is chosen such that the peak−to−peak ripple current I_{L_PP} is approximately 20% to 50% of the maximum output current I_{OUT_MAX}. This provides the best trade−off between transient response and output ripple. The inductance corresponding to a given current ripple is:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot I_{L\_PP}}$$

The selected inductor must have a saturation current rating higher than the maximum peak current which is calculated by:

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{I_{L\_PP}}{2}$$

The inductor must also have a high enough current rating to avoid self−heating. A low DCR is therefore preferred. Refer to Table 25 for recommended inductors.

Table 25. INDUCTOR SELECTION

Supplier	Part #	Value (uH)	Size (L x l x T) (mm)	Saturation Current Max (A)	DCR Max at 25°C (mΩ)
Cyntec	PIFE20161B−R33MS−11	0.33	2.0 x 1.6 x 1.2	4.0	33
Cyntec	PIFE25201B−R33MS−11	0.33	2.5 x 2.0 x 1.2	5.2	17
Cyntec	PIFE32251B−R33MS−11	0.33	3.2 x 2.5 x 1.2	6.5	14

Table 25. INDUCTOR SELECTION

Supplier	Part #	Value (uH)	Size (L x l x T) (mm)	Saturation Current Max (A)	DCR Max at 25°C (mΩ)
TOKO	DFE252012F−H−R33M	0.33	2.5 x 2.0 x 1.2	5.1	13
TOKO	DFE201612E−H−R33M	0.33	2.0 x 1.6 x 1.2	4.8	21
TOKO	FDSD0412−H−R33M	0.33	4.2 x 4.2 x 1.2	7.5	19
TDK	VLS252012HBX−R33M	0.33	2.5 x 2.0 x 1.2	5.3	25
TDK	SPM5030T−R35M	0.35	7.1 x 6.5 x 3.0	14.9	4
Chilisin	HEI201612A−R24M−AUDG	0.24	2.0 x 1.6 x 1.2	4.8	13.5

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance a high output capacitor value must be used. For a given peak−to−peak ripple current I_{L_PP} in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three components as shown below.

$$V_{OUT\_PP} \approx V_{OUT\_PP(C)} + V_{OUT\_PP(ESR)} + V_{OUT\_PP(ESL)},$$

With:

$$V_{OUT\_PP(C)} = \frac{I_{L\_PP}}{8 \cdot C \cdot f_{SW}}$$

$$V_{OUT\_PP(ESR)} = I_{L\_PP} \cdot ESR$$

$$V_{OUT\_PP(ESL)} = \frac{L_{ESL}}{L} \cdot V_{IN}$$

Where the peak−to−peak ripple current is given by

$$I_{L\_PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot L}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUT\_PP(C)}$. The minimum output capacitance can be calculated based on a given output ripple requirement V_{OUT_PP} in PPWM operation mode.

$$C_{MIN} = \frac{I_{L\_PP}}{8 \cdot V_{OUT\_PP} \cdot f_{SW}}$$

Input Capacitor Selection

One of the input capacitor selection requirements is the input voltage ripple. To minimize the input voltage ripple and get better decoupling at the input power supply rail, a ceramic capacitor is recommended due to low ESR and ESL.

The minimum input capacitance with respect to the input ripple voltage V_{IN_PP} is

$$C_{IN\_MIN} = \frac{I_{OUT\_MAX} \cdot (D - D^2)}{V_{IN\_PP} \cdot f_{SW}} \quad \text{Where} \quad D = \frac{V_{OUT}}{V_{IN}}$$

In addition, the input capacitor must be able to absorb the input current, which has a RMS value of

$$I_{IN\_RMS} = I_{OUT\_MAX} \cdot \sqrt{D - D^2}$$

The input capacitor also must be sufficient to protect the device from over voltage spikes, and a 4.7 uF capacitor or greater is required. The input capacitor should be located as close as possible to the IC. All PGND pins must be connected together to the ground terminal of the input cap which then must be connected to the ground plane. All PVIN pins must be connected together to the Vbat terminal of the input cap which then connects to the Vbat plane.

Power Capability

The NCV6356's power capability is driven by the difference in temperature between the junction (T_J) and ambient (T_A), the junction−to−ambient thermal resistance ($R\theta_{JA}$), and the on−chip power dissipation (P_{IC}).

The on−chip power dissipation P_{IC} can be determined as $P_{IC} = P_T - P_L$ with the total power losses P_T being $P_T = V_{OUT} \cdot I_{OUT} \cdot \left(\frac{1}{\eta} - 1\right)$ where η is the efficiency and P_L the simplified inductor power losses $P_L = I_{LOAD}^2 \cdot DCR$.

Now the junction temperature T_J can easily be calculated as $T_J = R\theta_{JA} \cdot P_{IC} + T_A$

Please note that the T_J should stay within the recommended operating conditions.

The $R\theta_{JA}$ is a function of the PCB layout (number of layers and copper and PCB size). For example, the NCV6356 mounted on the EVB has a $R\theta_{JA}$ about 30°C/W.

Layout Considerations

Electrical Rules

Good electrical layout is key to proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- Use wide and short traces for power paths (such as PVIN, VOUT, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- The device should be well decoupled by input capacitor and the input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission.
- SW track should be wide and short to reduce losses and noise radiation.
- It is recommended to have separated ground planes for PGND and AGND and connect the two planes at one point. Try to avoid overlap of input ground loop and output ground loop to prevent noise impact on output regulation.
- Arrange a "quiet" path for output voltage sense, and make it surrounded by a ground plane.

Thermal Rules

Good PCB layout improves the thermal performance and thus allows for high power dissipation even with a small IC package. Thermal layout guidelines are:

- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- Use multiple vias around the IC to connect the inner ground layers to reduce thermal impedance.
- Use a large and thick copper area especially in the top layer for good thermal conduction and radiation.
- Use two layers or more for the high current paths (PVIN, PGND, SW) in order to split current into different paths and limit PCB copper self−heating.

Component Placement

- Input capacitor placed as close as possible to the IC.
- PVIN directly connected to Cin input capacitor, and then connected to the Vin plane. Local mini planes used on the top layer (green) and the layer just below the top layer (yellow) with laser vias.
- AVIN connected to the Vin plane just after the capacitor.
- AGND directly connected to the GND plane.
- PGND directly connected to Cin input capacitor, and then connected to the GND plane: Local mini planes used on the top layer (green) and the layer just below the top layer (yellow) with laser vias.

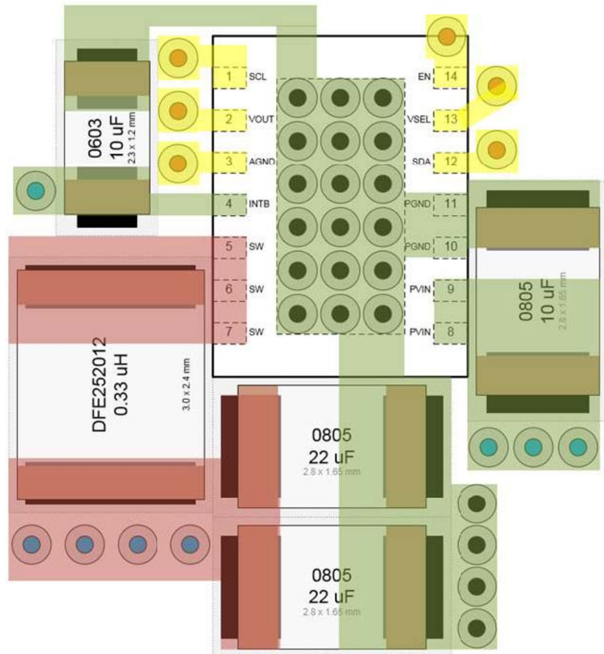


Figure 54. Placement Recommendation

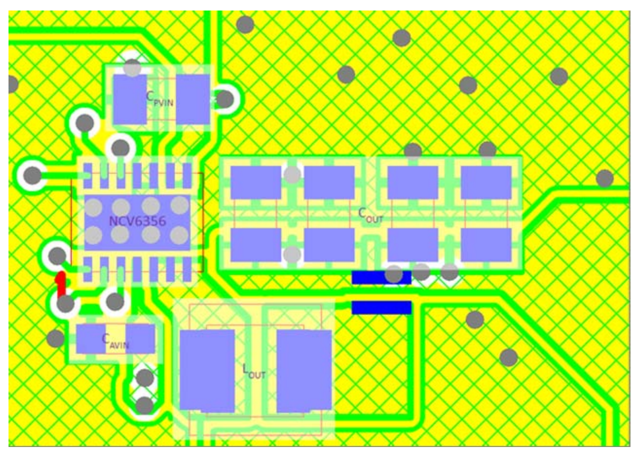


Figure 55. Demo Board Example (INTB not used)

Table 26. ORDERING INFORMATION

OPN	Marking	Configuration	Package	Shipping†
NCV6356CMTWTXG	6356C	5.0 A 1.150 V / 1.150 V	DFN 3.0 x 4.0 mm (Pb−Free)	3,000 Tape & Reel
NCV6356BMTWTXG	6356B	5.0 A 1.200 V / 1.200 V	DFN 3.0 x 4.0 mm (Pb−Free)	3,000 Tape & Reel
NCV6356QMTWTXG	6356Q	5.0 A 0.875 V / 0.906 V	DFN 3.0 x 4.0 mm (Pb−Free)	3,000 Tape & Reel

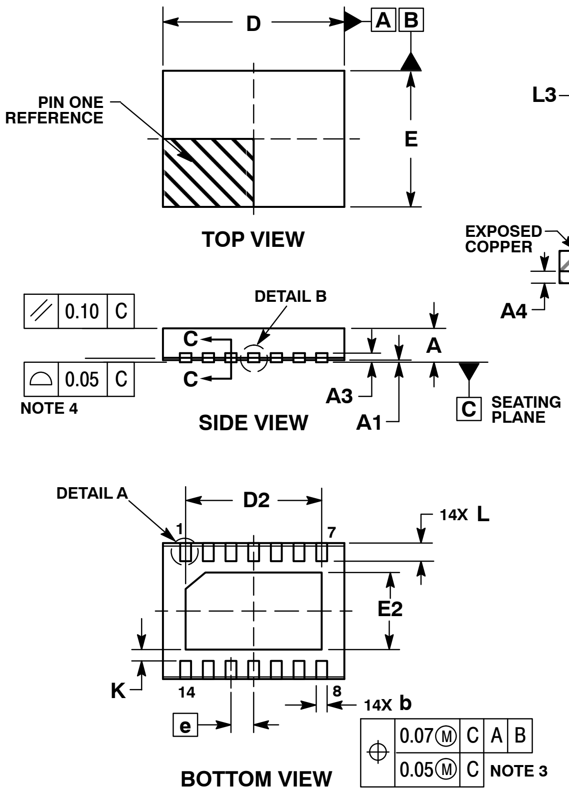
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

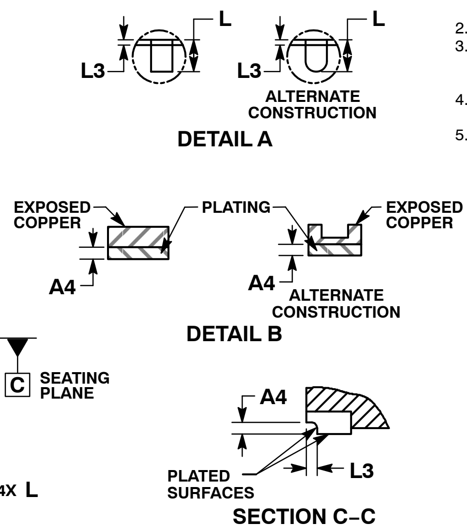
Demo board available:

- The NCV6356GEVB/D evaluation board that configures the device in typical application to supply constant voltage.

PACKAGE DIMENSIONS

WDFNW14 4x3, 0.5P
CASE 511CM
ISSUE O

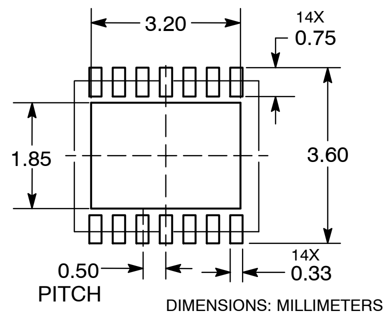




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3		0.20 REF	
A4		0.10 REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.90	3.00	3.10
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
e		0.50 BSC	
K	0.25	---	---
L	0.30	0.40	0.50
L3	0.00	0.05	0.10

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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