Reference Manual

DOC. REV. 4/9/2013

VL-EPMs-E1

Dual Gigabit Ethernet
SUMIT on PC/104 Module

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Notice:

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Product Release Notes

Rev 1.0 Release

Initial production release.

Support Page

The VL-EPMs-E1 support page, at **http://www.versalogic.com/private/epmse1support.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- Photograph of the circuit board
- BIOS information and upgrades
- Utility routines and benchmark software

This is a private page for VL-EPMs-E1 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

VersaTech KnowledgeBase

Contents

Introduction 1

Features

The VL-EPMs-E1 is a high-performance Gigabit Ethernet interface for SUMIT on PC/104 systems. It incorporates a PCI Express Mini Card socket for optional wireless operation. Its features include:

- Dual Intel 82574 based 10BaseT / 100BaseTX / 1000BaseT Ethernet interface
- SUMIT connectors
- PCI Express Mini Card interface for wireless internet, USB 2.0, SSD, or other add-on cards
- TVS devices on Ethernet interfaces for protection against power spikes and surges
- Full compliance with EU Directive 2002/95/EC (RoHS) for devices used in Europe
- Designed to provide -40° to +85°C operation for reliable use in harsh environments
- SUMIT-104 (Legacy Type 1 SUMIT-ISM) compliant footprint
- WiFi card and antenna for PCI Express slot available as optional accessories

The VL-EPMs-E1 features high reliability design and construction. All VL-EPMs-E1 boards are subjected to functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional SBC.

There are two models of the VL-EPMs-E1. The VL-EPMs-E1b includes both the SUMIT-A and SUMIT-B connectors, as well as the PC/104 (ISA) bus. The VL-EPMs-E1a is a simplified, lighter model that eliminates the SUMIT-B and PC/104 connectors.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size:
3.550" x 3.775" (PC/104 standard)
Storage Temperature:
-40° to +85°C
Free Air Operating Temperature:
-40° to +85°C
Power Requirements:
+5.0V 3 watt without PCI-e wireless card during transmission.
Ethernet Controller:
Two Intel 82574L based ports
Ethernet Buffer RAM:
16 KB
Ethernet Compatibility Modes:
10BaseT
100BaseTX
1000BaseT
Compliant with the 1 Gb/s Ethernet 802.3 802.3u 802.3ab specifications
Compatibility:
SUMIT-104 compatible

SUMIT Resources

Form Factor: SUMIT-104

	SUMIT A	SUMIT B*
PCIe x1	1	–
PCIe x4		–
USB	1	
ExpressCard	–	
LPC	–	
SPI / µWire	–	
SMBus/ I^2C	–	
+12V	–	
+5V	✓	✓
+5Vsb	–	–
+3.3V	–	–

** Optional configuration.*

Specifications are subject to change without notice.

Block Diagram

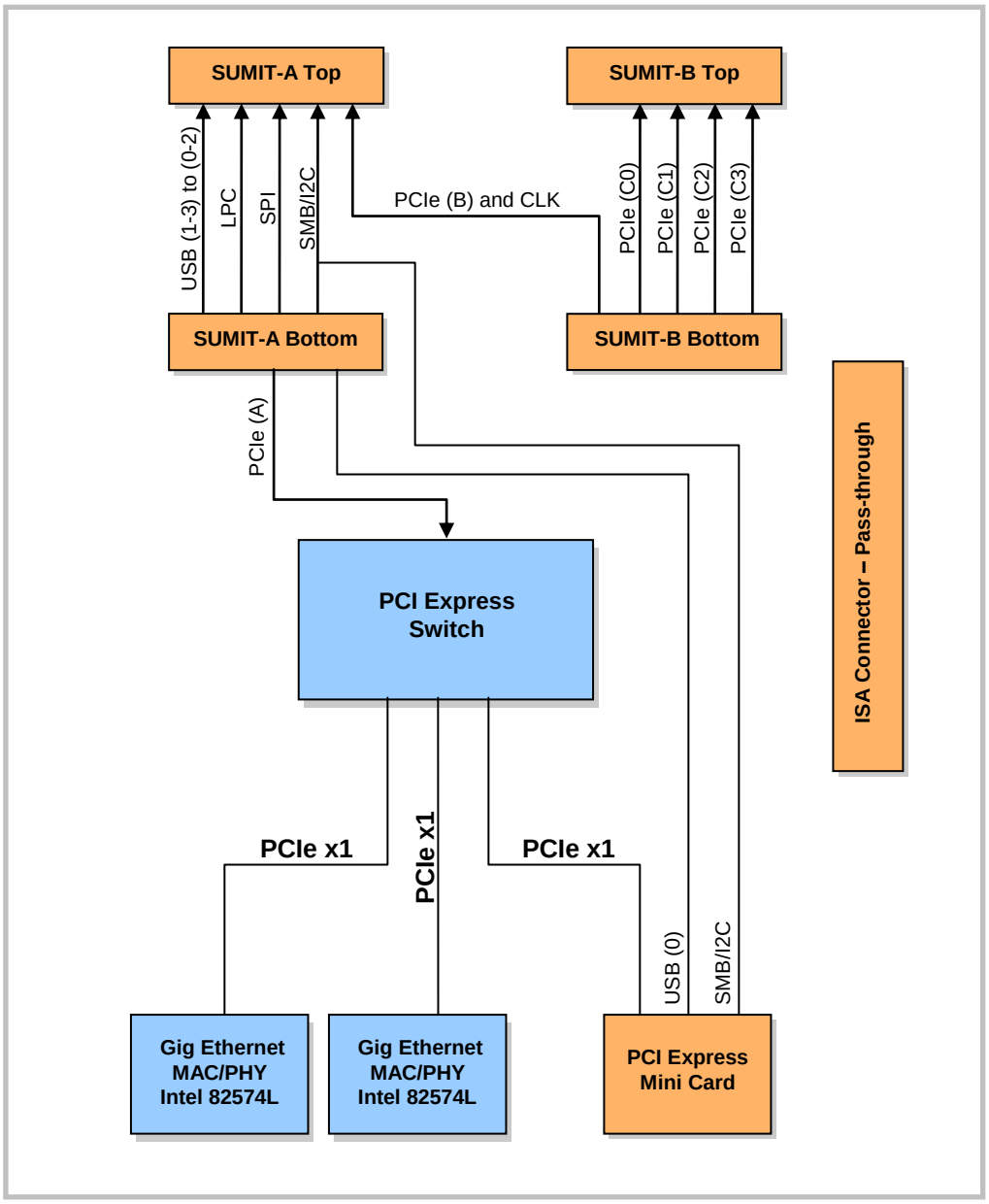

Figure 1. VL-EPMs-E1b Block Diagram

RoHS-Compliance

The VL-EPMs-E1 is RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corp. is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic antistatic envelope during shipment or storage.

ELECTROMAGNETIC INTERFERENCE

The Ethernet connector shields at J4 and J6 are connected to earth ground to protect against electromagnetic interference (EMI). The connection to earth ground is made at the board's lower left mounting hole, as shown in Figure 2. All other mounting holes are floating. Use metal standoffs or a grounding strap to connect the lower left mounting hole to the enclosure chassis, which should be connected to earth ground.

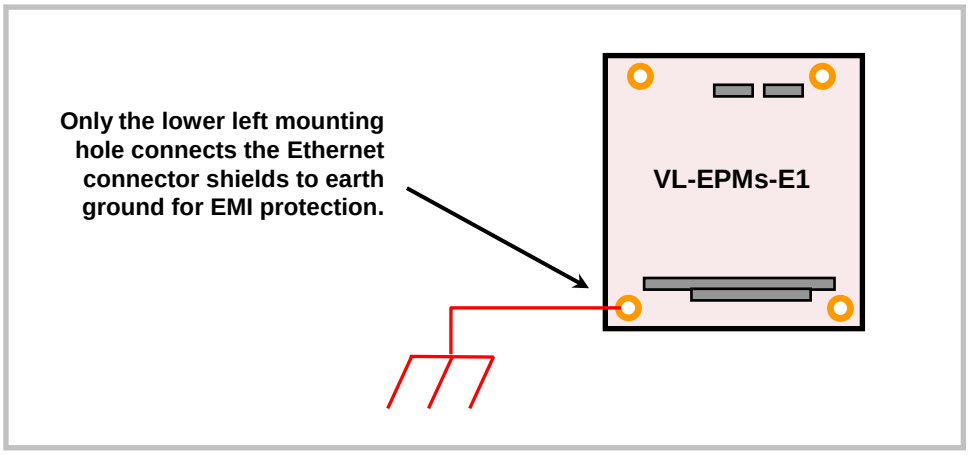

Figure 2. Attaching the VL-EPMs-E1 to Earth Ground

Technical Support

If you are unable to solve a problem after reading this manual, please visit the VL-EPMs-E1 product support web page below. The support page provides links to component datasheets and any available device drivers.

VL-EPMs-E1 Support Page

http://www.versalogic.com/private/epms1support.asp

The VersaTech KnowledgeBase contains a wealth of technical information about VersaLogic products, along with product advisories. Click the link below to see all KnowledgeBase articles related to the VL-EPMs-E1.

VersaTech KnowledgeBase

If you have further questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261.

Please provide the following information:

- Your name, the name of your company, your phone number, and your e-mail address
- The name of a technician or engineer that can be contact if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

Dimensions and Mounting

The VL-EPMs-E1 complies with PC/104-Express dimensional standards, which provide for specific mounting hole and stack locations as shown in the diagram below.

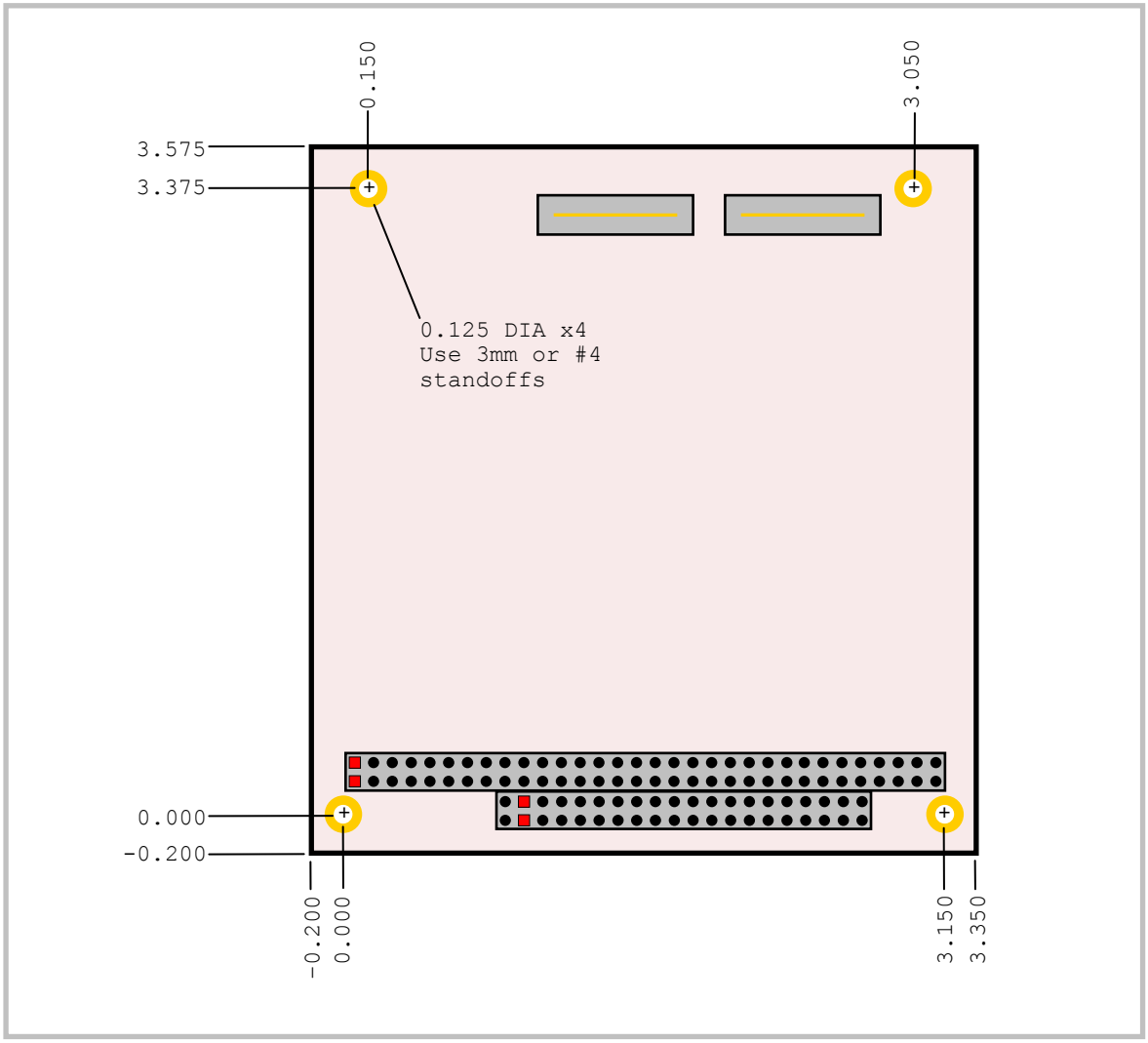

Figure 3. VL-EPMs-E1 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

Caution The board must be supported at all four mounting points to prevent excessive flexing when expansion modules are mated and detached. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.

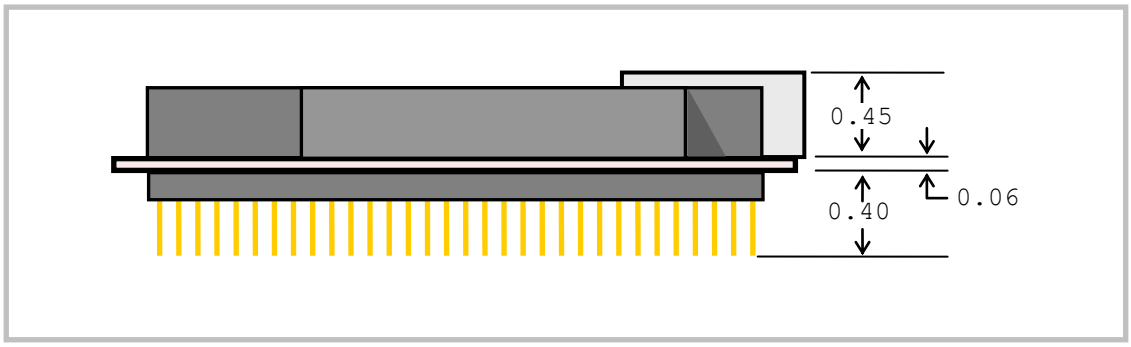

Figure 4. VL-EPMs-E1 Height Dimensions

(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The VL-EPMs-E1b uses PC/104 (ISA) and SUMIT connectors so that the module can be added to the middle or top of the stack. The VL-EPMs-E1a

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Standoffs are secured to the top circuit board using four pan head screws. Standoffs and screws are available as part number VL-HDW-105. Note that the standoffs in this kit are 15.25 mm (0.60"), and must not be mixed with the 15.0 mm standoffs used for non-SUMIT boards.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack. Use caution when using the extractor tool not to damage any board components.

STACK ARRANGEMENT EXAMPLE

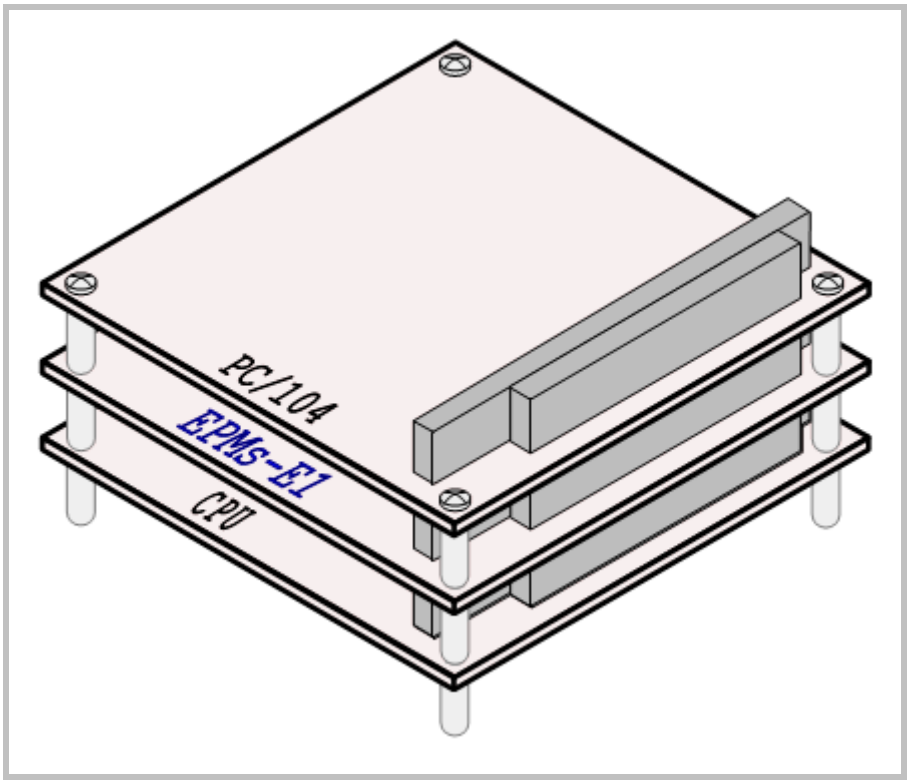

Figure 5. Stack Arrangement Example

External Connectors

VL-EPMs-E1 Connectors

The VL-EPMs-E1b (shown in Figure 6) includes the SUMIT-AB and PC/104 (ISA) connectors. The VL-EPMs-E1a (not shown) does not include the SUMIT-B or PC/104 connectors.

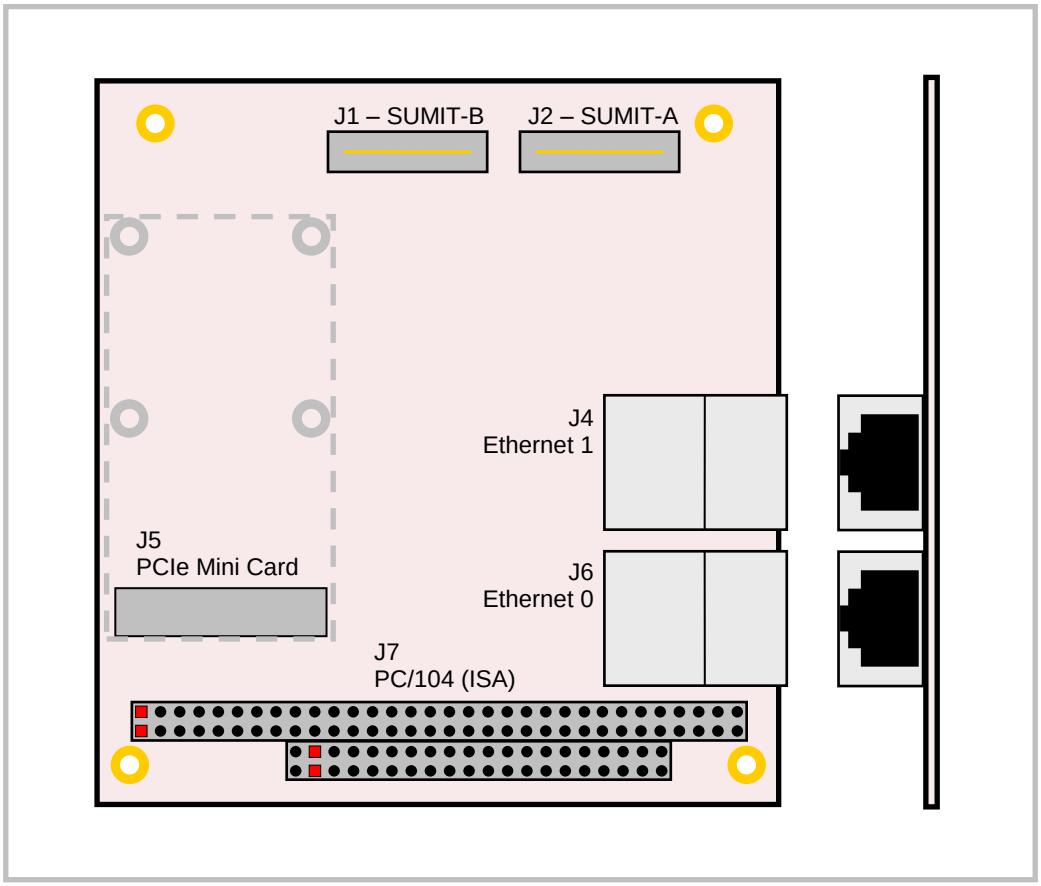

Figure 6. VL-EPMs-E1b Connectors – Top Side

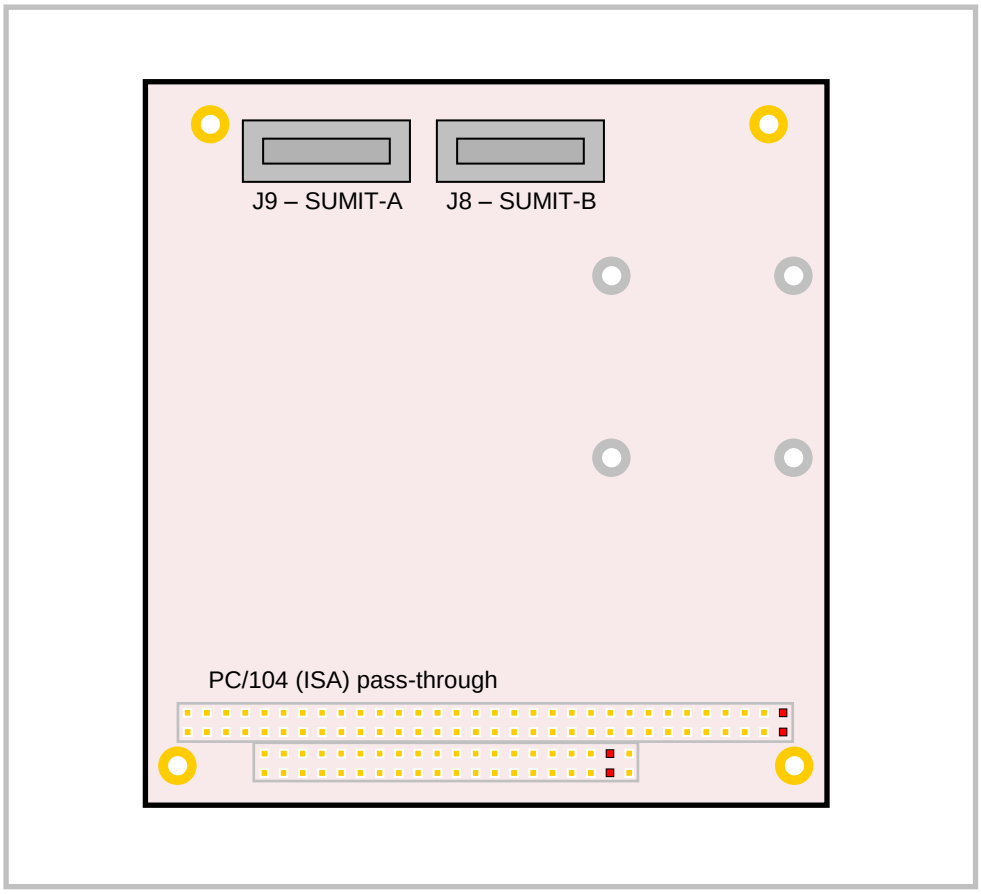

Figure 7. VL-EPMs-E1b Connectors – Bottom Side

VL-EPMs-E1 Connector Functions and Interface Cables

The following table notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Pin 1 Location[1] x coord.	Pin 1 Location[1] y coord.	Page
J1	SUMIT-B Top[2]	Samtec ASP-129637-01	–	–	1.669	3.317	15
J2	SUMIT-A Top	Samtec ASP-129637-01	–	–	2.712	3.317	16
J3	Ethernet LED	–	–	–	3.185	3.101	13
J4	Ethernet 1	RJ-45 Crimp-on Plug	–	–	2.622	1.778	13
J5	PCIe Mini Card	Full-height PCIe Mini Card	–	–	-0.020	0.695	17
J6	Ethernet 0	RJ-45 Crimp-on Plug	–	–	2.622	0.968	13
J7	PC/104[2]	AMP 1375795-2	–	–	0.050	0.200	18
J8	SUMIT-B Bottom[2]	Samtec ASP-129646-01	–	–	1.669	3.317	19
J9	SUMIT-A Bottom	Samtec ASP-129646-01	–	–	2.712	3.317	20

1. The PCB origin is the mounting hole to the lower left, as oriented in Figure 3.
2. VL-EPMs-E1b only.

Ethernet Interface (J4, J6) and LED Connector (J3)

The VL-EPMs-E1 features two Intel 82574L Gigabit Ethernet controllers. Though these controllers are not NE2000-compatible, they are widely supported. Drivers are readily available to support a variety of operating systems. See the VersaLogic website for latest OS support.

STATUS LED

Each RJ-45 connector has two built-in LEDs to provide an indication of the Ethernet status as shown in the following table.

Table 2: RJ-45 Ethernet Status LED

LED	State	Description
Green/Orange (Link Speed)	Orange	1 Gbps speed
	Green	100 Mbps speed
	Off	10 Mbps speed or cable not plugged into active hub
Yellow (Activity)	On	Activity detected on cable (intermittent with activity)
	Off	No activity detected on cable

Connector J3 provides an on-board Ethernet LED interface. The 3.3V power supplied to this connector is protected by a 1 Amp fuse.

Table 3: J3 Ethernet Status Connector Pinout

J3 Pin	Signal Name	Function
1	+3.3V	Protected Power Supply
2	YEL–_A	Ethernet 1 Yellow LED
3	ORN–_A	Ethernet 1 Orange LED
4	GRN–_A	Ethernet 1 Green LED
5	+3.3V	Protected Power Supply
6	YEL–_B	Ethernet 0 Yellow LED
7	ORN–_B	Ethernet 0 Orange LED
8	GRN–_B	Ethernet 0 Green LED
9	GND	Ground
10	W_Disable#	Wireless disable

ETHERNET CONNECTOR

Board-mounted RJ-45 connectors are provided to make connections with Category 5 Ethernet cables. The 82574L Ethernet controller auto-detects 10BaseT/100Base-TX/1000BaseT connections.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 4: RJ-45 Ethernet Connector Pinout

J4/J6 Pin	10/100 Fast Ethernet		10/100/1000 Gigabit Ethernet	
	Signal Name	Function	Signal Name	Function
1	T+	Transmit Data +	MID0+	Media Dependent Interface [0]+
2	T–	Transmit Data –	MID0–	Media Dependent Interface [0]–
3	R+	Receive Data +	MID1+	Media Dependent Interface [1]+
4	IGND	Isolated Ground	MID2+	Media Dependent Interface [2]+
5	IGND	Isolated Ground	MID2–	Media Dependent Interface [2]–
6	R–	Receive Data –	MID1–	Media Dependent Interface [1]–
7	IGND	Isolated Ground	MID3+	Media Dependent Interface [3]+
8	IGND	Isolated Ground	MID3–	Media Dependent Interface [3]–

The NIC can accommodate various TXD/RXD pair reversals and it features auto crossover cable functionality.

SUMIT-B Top Connector (J1)

The table below shows the SUMIT-B Top connections to the VL-EPMs-E1. Signals that are not connected are pass-through only. This connector is present only on the VL-EPMs-E1b. The +5V signals on this connector are available to power the VL-EPMs-E1.

Note: SUMIT technology uses an automatic link alignment feature (also known as "lane shifting") to eliminate the need for jumpers or switches to identify an expansion module's position in the stack. Signals are not simply passed straight up from the bottom connector to the top on SUMIT modules. Links that are used by the expansion module are automatically selected, and the remaining unused signals are shifted down to the consumed link's pins on the top connector for use by the next board. Both PCIe and USB signals are subject to auto-alignment. See page 28 of the SUMIT Specification for an explanation of this feature.

Table 5: SUMIT-B Top Connector Pinout

Pin	Signal Name	Function
1	GND	Ground
3	B_PETp0	Link B, lane 0 transmit +
5	B_PETn0	Link B, lane 0 transmit –
7	GND	Ground
9	NC	No connect
11	NC	No connect
13	NC	No connect
15	C_PETp0	Link C, lane 0 transmit +
17	C_PETn0	Link C, lane 0 transmit –
19	GND	Ground
21	C_PETp1	Link C, lane 1 transmit +
23	C_PETn1	Link C, lane 1 transmit –
25	GND	Ground
27	C_PETp2	Link C, lane 2 transmit +
29	C_PETn2	Link C, lane 2 transmit –
31	GND	Ground
33	NC	No connect
35	NC	No connect
37	GND	Ground
39	PERST#	Reset
41	RSVD_B_3	Reserved/pass-through
43	+5V	+5V power
45	+5V	+5V power
47	+5V	+5V power
49	+5V	+5V power
51	+5V	+5V power

Pin	Signal Name	Function
2	GND	Ground
4	B_PERp0	Link B, lane 0 receive +
6	B_PERn0	Link B, lane 0 receive –
8	BPRSNT#/GND	Link B present
10	B_CLKp	Link B clock +
12	B_CLKn	Link B clock –
14	GND	Ground
16	C_PERp0	Link C, lane 0 receive +
18	C_PERn0	Link C, lane 0 receive –
20	GND	Ground
22	C_PERp1	Link C, lane 1 receive +
24	C_PERn1	Link C, lane 1 receive –
26	GND	Ground
28	C_PERp2	Link C, lane 2 receive +
30	C_PERn2	Link C, lane 2 receive –
32	GND	Ground
34	NC	No connect
36	NC	No connect
38	GND	Ground
40	WAKE#	Wake
42	RSVD_B_1	Reserved/pass-through
44	RSVD_B_2	Reserved/pass-through
46	3.3V	+3.3V power
48	3.3V	+3.3V power
50	3.3V	+3.3V power
52	+5VSB	+5V standby power

SUMIT-A Top Connector (J2)

The table below shows the SUMIT-A Top connections to the VL-EPMs-E1. Signals that are not connected are pass-through only. The +5V signals on this connector are available to power the VL-EPMs-E1.

Note: SUMIT technology uses an automatic link alignment feature (also known as "lane shifting") to eliminate the need for jumpers or switches to identify an expansion module's position in the stack. Signals are not simply passed straight up from the bottom connector to the top on SUMIT modules. Links that are used by the expansion module are automatically selected, and the remaining unused signals are shifted down to the consumed link's pins on the top connector for use by the next board. Both PCIe and USB signals are subject to auto-alignment. See page 28 of the SUMIT Specification for an explanation of this feature.

Table 6: SUMIT-A Top Connector Pinout

Pin	Signal Name	Function
1	+5VSB	+5V power standby
3	3.3V	+3.3V power
5	3.3V	+3.3V power
7	EXPCD_REQ#	ExpressCard request
9	EXPCD_PRSNT#	ExpressCard present
11	USB_OC#0/1	USB0-1 overcurrent flag
13	USB_OC#2/3	USB2-3 overcurrent flag
15	+5V	+5V power
17	NC	No connect
19	NC	No connect
21	+5V	+5V power
23	USB2+	USB2 data +
25	USB2-	USB2 data –
27	+5V	+5V power
29	USB1+	USB1 data +
31	USB1-	USB1 data –
33	+5V	+5V power
35	USB0+	USB0 data +
37	USB0-	USB0 data –
39	GND	Ground
41	A_PETp0	Link A, lane 0 transmit +
43	A_PETn0	Link A, lane 0 transmit –
45	GND	Ground
47	PERST#	Reset
49	WAKE#	Wake
51	+5V	+5V power

Pin	Signal Name	Function
2	+12V	+12V power
4	SMB/I2C_DATA	SMBus data
6	SMB/I2C_CLK	SMBus clock
8	SMB/I2C_ALERT#	SMBus interrupt line in
10	SPI/uWire_DO	SPI data out from master
12	SPI/uWire_DI	SPI data in to master
14	SPI/uWire_CLK	SPI clock
16	SPI/uWire_CS0#	SPI chip select 0
18	SPI/uWire_CS1#	SPI chip select 1
20	Reserved	Reserved
22	LPC_DRQ	LPC DMA request
24	LPC_AD0	LPC line 0
26	LPC_AD1	LPC line 1
28	LPC_AD2	LPC line 2
30	LPC_AD3	LPC line 3
32	LPC_FRAME#	LPC frame
34	SERIRQ#	Serial IRQ legacy
36	LPC_PRSNT#/GND	LPC card present
38	CLK_33MHz	33 MHz clock out
40	GND	Ground
42	A_PERp0	Link A, lane 0 receive +
44	A_PERn0	Link A, lane 0 receive –
46	APRSNT#/GND	Link A card present
48	A_CLKp	Link A clock +
50	A_CLKn	Link A clock –
52	GND	Ground

PCI Express Mini Card Socket (J5)

The PCI Express Mini Card connector at J5 accepts a full-height PCI Express Mini Card. The interface includes one PCIe x1 lane, one USB 2.0 channel, and the SMBus interface. The socket is compatible with 802.11a/b/g Wi-Fi network adapters that operate in both the 2.4 and 5.0 GHz spectra, GPS radio cards that enable time/date stamps and global location applications, 3G modems, solid-state drives (SSDs), and USB (2.0) cards.

An optional Intel WiFi Link 5300 PCI Express Mini card is available for the VL-EPMs-E1 as VersaLogic part number VL-WD10-CBN. A WiFi antenna (VL-CBR-ANT01) and a 12" WiFi card to bulkhead RP-SMA transition cable (VL-CBR-0201) are also available. For more information, contact Sales@VersaLogic.com.

To secure a Mini Card to the VL-EPMs-E1 use two screws (M2 x 5mm, Philips, pan head, 4mm, stainless) and two washers (M2, split lock, OD 4.4mm, stainless). Screw and washer sets are available in 10-count packages as part number VL-HDW-107.

Table 7: PCIe Mini Card Pinout

Pin	Signal Name	Function
1	WAKE#	Wake
3	NC	Not connected
5	NC	Not connected
7	CLKREQ#	Reference clock request
9	GND	Ground
11	REFCLK-	Reference clock input –
13	REFCLK+	Reference clock input +
15	GND	Ground
17	NC	Not connected
19	NC	Not connected
21	GND	Ground
23	PERn0	Lane 0 receive –
25	PERp0	Lane 0 receive +
27	GND	Ground
29	GND	Ground
31	PETn0	PCIe lane 0 transmit –
33	PETp0	PCIe lane 0 transmit +
35	GND	Ground
37	GND	Ground
39	3.3VAUX	3.3V auxiliary source
41	3.3VAUX	3.3V auxiliary source
43	GND	Ground
45	NC	Not connected
47	NC	Not connected
49	NC	Not connected
51	NC	Not connected

Pin	Signal Name	Function
2	3.3VAUX	3.3V auxiliary source
4	GND	Ground
6	1.5V	1.5V power
8	NC	Not connected
10	NC	Not connected
12	NC	Not connected
14	NC	Not connected
16	NC	Not connected
18	GND	Ground
20	W_DISABLE#	Wireless disable
22	PERST#	Card reset
24	3.3VAUX	3.3V auxiliary source
26	GND	Ground
28	1.5V	1.5V power
30	SMB_CLK	SMBus clock
32	SMB_DATA	SMBus data
34	GND	Ground
36	USB_D-	USB data –
38	USB_D+	USB data +
40	GND	Ground
42	LED_WWAN#	Wireless WAN LED
44	LED_WLAN#	Wireless LAN LED
46	LED_WPAN#	Wireless PAN LED
48	1.5V	1.5V power
50	GND	Ground
52	3.3VAUX	3.3V auxiliary source

W_DISABLE# SIGNAL

The W_DISABLE# is for use with optional wireless Ethernet PCIe Mini Cards. The signal allows you to disable a wireless card's radio operation in order to meet public safety regulations or when otherwise desired. The W_DISABLE# signal is an active low signal that when driven low (shorted to ground) disables radio operation on the PCIe Mini Card wireless device. When the W_DISABLE# is not asserted, or in an high impedance state, the radio may transmit if not disabled by other means such as software.

LED_WWAN#, LED_WLAN#, AND LED_WPAN# SIGNALS

The LED status indicator signals are provided to enable wireless communications add-in cards to provide status indications via the built-in LEDs at positions D1 and D2 on the VL-EPMs-E1. The behavior of the LEDs is determined by the add-in card manufacturer. The table below shows the routing of the D1 and D2 LEDs to the Mini Card LED status signals.

Table 8: WiFi Mini Card LED Functions

LED	Color	J5 Pin	Function
D1	Green	46	Defined by Mini Card device LED_WPAN# implementation.
D1	Orange	44	Defined by Mini Card device LED_WLAN# implementation.
D2	Green	42	Defined by Mini Card device LED_WWAN# implementation.
D2	Orange	–	Power status indicator.

PC/104 (ISA) Connector (J7)

The PC/104 (ISA) connector is a pass-through connector only. This connector is present only on the VL-EPMs-E1b. The +5V signals on this connector are available to power the VL-EPMs-E1.

SUMIT-B Bottom Connector (J8)

The table below shows the SUMIT-B Bottom connections to the VL-EPMs-E1. Signals that are not connected are pass-through only. This connector is present only on the VL-EPMs-E1b. The +5V signals on this connector are available to power the VL-EPMs-E1.

Note: SUMIT technology uses an automatic link alignment feature (also known as "lane shifting") to eliminate the need for jumpers or switches to identify an expansion module's position in the stack. Signals are not simply passed straight up from the bottom connector to the top on SUMIT modules. Links that are used by the expansion module are automatically selected, and the remaining unused signals are shifted down to the consumed link's pins on the top connector for use by the next board. Both PCIe and USB signals are subject to auto-alignment. See page 28 of the SUMIT Specification for an explanation of this feature.

Table 9: SUMIT-B Bottom Connector Pinout

Pin	Signal Name	Function
1	GND	Ground
3	B_PETp0	Link B, lane 0 transmit +
5	B_PETn0	Link B, lane 0 transmit –
7	GND	Ground
9	C_CLKp	Link C clock +
11	C_CLKn	Link C clock –
13	CPRSNT#/GND	Link C card present
15	C_PETp0	Link C, lane 0 transmit +
17	C_PETn0	Link C, lane 0 transmit –
19	GND	Ground
21	C_PETp1	Link C, lane 1 transmit +
23	C_PETn1	Link C, lane 1 transmit –
25	GND D	Ground
27	C_PETp2	Link C, lane 2 transmit +
29	C_PETn2	Link C, lane 2 transmit –
31	GND	Ground
33	C_PETp3	Link C, lane 3 transmit +
35	C_PETn3	Link C, lane 3 transmit –
37	GND	Ground
39	PERST#	Reset
41	RSVD_B_3	Reserved/pass-through
43	+5V	+5V power
45	+5V	+5V power
47	+5V	+5V power
49	+5V	+5V power
51	+5V	+5V power

Pin	Signal Name	Function
2	GND	Ground
4	B_PERp0	Link B, lane 0 receive +
6	B_PERn0	Link B, lane 0 receive –
8	BPRSNT#/GND	Link B present
10	B_CLKp	Link B clock +
12	B_CLKn	Link B clock –
14	GND	Ground
16	C_PERp0	Link C, lane 0 receive +
18	C_PERn0	Link C, lane 0 receive –
20	GND	Ground
22	C_PERp1	Link C, lane 1 receive +
24	C_PERn1	Link C, lane 1 receive –
26	GND	Ground
28	C_PERp2	Link C, lane 2 receive +
30	C_PERn2	Link C, lane 2 receive –
32	GND	Ground
34	C_PERp3	Link C, lane 3 receive +
36	C_PERn3	Link C, lane 3 receive –
38	GND	Ground
40	WAKE#	Wake
42	RSVD_B_1	Reserved/pass-through
44	RSVD_B_2	Reserved/pass-through
46	3.3V	+3.3V power
48	3.3V	+3.3V power
50	3.3V	+3.3V power
52	+5VSB	+5V standby power

SUMIT-A Bottom Connector (J9)

The table below shows the SUMIT-A Bottom connections to the VL-EPMs-E1. Signals that are not connected are pass-through only. The +5V signals on this connector are available to power the VL-EPMs-E1.

PCIe Channel A is routed from this connector to PCIe switch, which produces the three downstream PCIe x1 ports for use by the Ethernet ports and the PCIe Mini Card.

Note: SUMIT technology uses an automatic link alignment feature (also known as "lane shifting") to eliminate the need for jumpers or switches to identify an expansion module's position in the stack. Signals are not simply passed straight up from the bottom connector to the top on SUMIT modules. Links that are used by the expansion module are automatically selected, and the remaining unused signals are shifted down to the consumed link's pins on the top connector for use by the next board. Both PCIe and USB signals are subject to auto-alignment. See page 28 of the SUMIT Specification for an explanation of this feature.

Table 10: SUMIT-A Bottom Connector Pinout

Pin	Signal Name	Function
1	+5VSB	+5V power standby
3	3.3V	+3.3V power
5	3.3V	+3.3V power
7	EXPCD_REQ#	ExpressCard request
9	EXPCD_PRSNT#	ExpressCard present
11	USB_OC#0/1	USB0-1 overcurrent flag
13	USB_OC#2/3	USB2-3 overcurrent flag
15	+5V	+5V power
17	USB3+	USB3 data +
19	USB3-	USB3 data –
21	+5V	+5V power
23	USB2+	USB2 data +
25	USB2-	USB2 data –
27	+5V	+5V power
29	USB1+	USB1 data +
31	USB1-	USB1 data –
33	+5V	+5V power
35	USB0+	USB0 data +
37	USB0-	USB0 data –
39	GND	Ground
41	A_PETp0	Link A, lane 0 transmit +
43	A_PETn0	Link A, lane 0 transmit –
45	GND	Ground
47	PERST#	Reset
49	NC	No connect
51	+5V	+5V power

Pin	Signal Name	Function
2	+12V	+12V power
4	SMB/I2C_DATA	SMBus data
6	SMB/I2C_CLK	SMBus clock
8	SMB/I2C_ALERT#	SMBus interrupt line in
10	SPI/uWire_DO	SPI data out from master
12	SPI/uWire_DI	SPI data in to master
14	SPI/uWire_CLK	SPI clock
16	SPI/uWire_CS0#	SPI chip select 0
18	SPI/uWire_CS1#	SPI chip select 1
20	Reserved	Reserved
22	LPC_DRQ	LPC DMA request
24	LPC_AD0	LPC line 0
26	LPC_AD1	LPC line 1
28	LPC_AD2	LPC line 2
30	LPC_AD3	LPC line 3
32	LPC_FRAME#	LPC frame
34	SERIRQ#	Serial IRQ legacy
36	LPC_PRSNT#/GND	LPC card present
38	CLK_33MHz	33 MHz clock out
40	GND	Ground
42	A_PERp0	Link A, lane 0 receive +
44	A_PERn0	Link A, lane 0 receive –
46	APRSNT#/GND	Link A card present
48	A_CLKp	Link A clock +
50	A_CLKn	Link A clock –
52	GND	Ground

Appendix A – References

Ethernet Controller *Intel 82574 Ethernet Controller*	Intel 82574 Datasheet
SUMIT Interface	SUMIT Specification
PC/104 Interface	PC/104 Specification
General PC Documentation *The Programmer's PC Sourcebook*	Amazon.com
General PC Documentation *The Undocumented PC*	Amazon.com