PIC18(L)F24/25/45K50 Family Silicon Errata and Data Sheet Clarification

The PIC18(L)F24/25/45K50 family devices that you have received conform functionally to the current Device Data Sheet (DS30684**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F24/25/45K50 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F24/25/45K50 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1) (11-bit)	Revision ID for Silicon Revision(2) (5-bit)	
		A1	A2
PIC18F24K50	5C6h	0 0001	0 0010
PIC18LF24K50	5CEh	0 0001	0 0010
PIC18F25K50	5C2h	0 0001	0 0010
PIC18LF25K50	5CAh	0 0001	0 0010
PIC18F45K50	5C0h	0 0001	0 0010
PIC18LF45K50	5C8h	0 0001	0 0010

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID:DEVREV".

2: Refer to the *"PIC18(L)F2X/4XK50 Flash Memory Programming Specification"* (DS41630) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A1	A2
Oscillator	Fail-Safe Clock Monitor	1.	HS oscillator remains biased if the crystal fails and the clock has switched to Fail-Safe Clock, causing high Sleep currents.	X	X
Timer1/3 Module with Gate Control	Asynchronous Counter Mode	2.	When using the Timer1 or Timer3 module as an Asynchronous Counter either separately or simultaneously, a false overflow interrupt can occur after reloading the TMRxL and TMRxH registers.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Oscillator

Higher Sleep currents will be observed if the HS oscillator fails and the PIC® MCU switches to the Fail-Safe Clock.

Issue occurs if:

- The device is running off of the HS clock
- The device experiences a failure on the HS clock and the Fail-Safe Clock activates
- The device then goes to Sleep without the HS clock returning
- The Sleep current observed will differ from base I_{PD} by an amount equal to the HS bias current.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: Timer1/3 Module with Gate Control

When using the Timer1 or Timer3 module, either separately or simultaneously, a false overflow event may occur after reloading the timer. The event only occurs when the timer is configured for Asynchronous Counter mode operation, and is only problematic if the timer's interrupt is enabled.

During the Interrupt Service Routine (ISR), after reloading the timer register (TMR1 and/or TMR3) with a new value, the false overflow event can occur upon the very next increment of the timer. This sets the TMRx Overflow Interrupt Flag bit (TMRxIF) and if the timer's interrupts are enabled, the interrupt service handler will again branch to the interrupt vector on the next instruction clock, after leaving the ISR. If interrupts are not enabled, the TMRx Overflow Interrupt Flag bit will be set, however, the firmware will not branch to the interrupt vector.

Work around

While inside the Interrupt Service Routine (ISR), create a loop routine that tests the timer for a minimum increment of one count. Once the timer has incremented by a minimum of one count, test the Overflow Interrupt Flag bit (TMRxIF) and clear it if set before leaving the ISR.

EXAMPLE 1: TMR1/3 FALSE INTERRUPT WORK AROUND

```
Load TMRx
   movlw       0xAA            ;W = 0xAA
   movlwf      TMR3H           ;Load TMRxH with W
   movlw       0x55            ;W = 0x55
   movwf       TMR3L           ;Load TMRxL with W
   movf        TMRxL, W        ;Move TMRxL to W
CheckTMR
   cpfsgt      TMRxL, 0        ;Compare f with W, skip if f>W
   goto        CheckTMR        ;Goto CheckTMR if TMRx has not incremented yet
   btfsc       PIRx, TMRxIF    ;Test for false TMRxIF
   bcf         PIRx, TMRxIF    ;Clear TMRx Overflow Interrupt Flag bit

   btfss       INTCON, GIE     ;Test if all interrupts including peripherals were
                               disabled
   bsf         INTCON, GIE     ;Enable all interrupts including peripherals if
                               disabled retfie
```

Affected Silicon Revisions

A1	A2						
X	X						

Data Sheet Clarifications

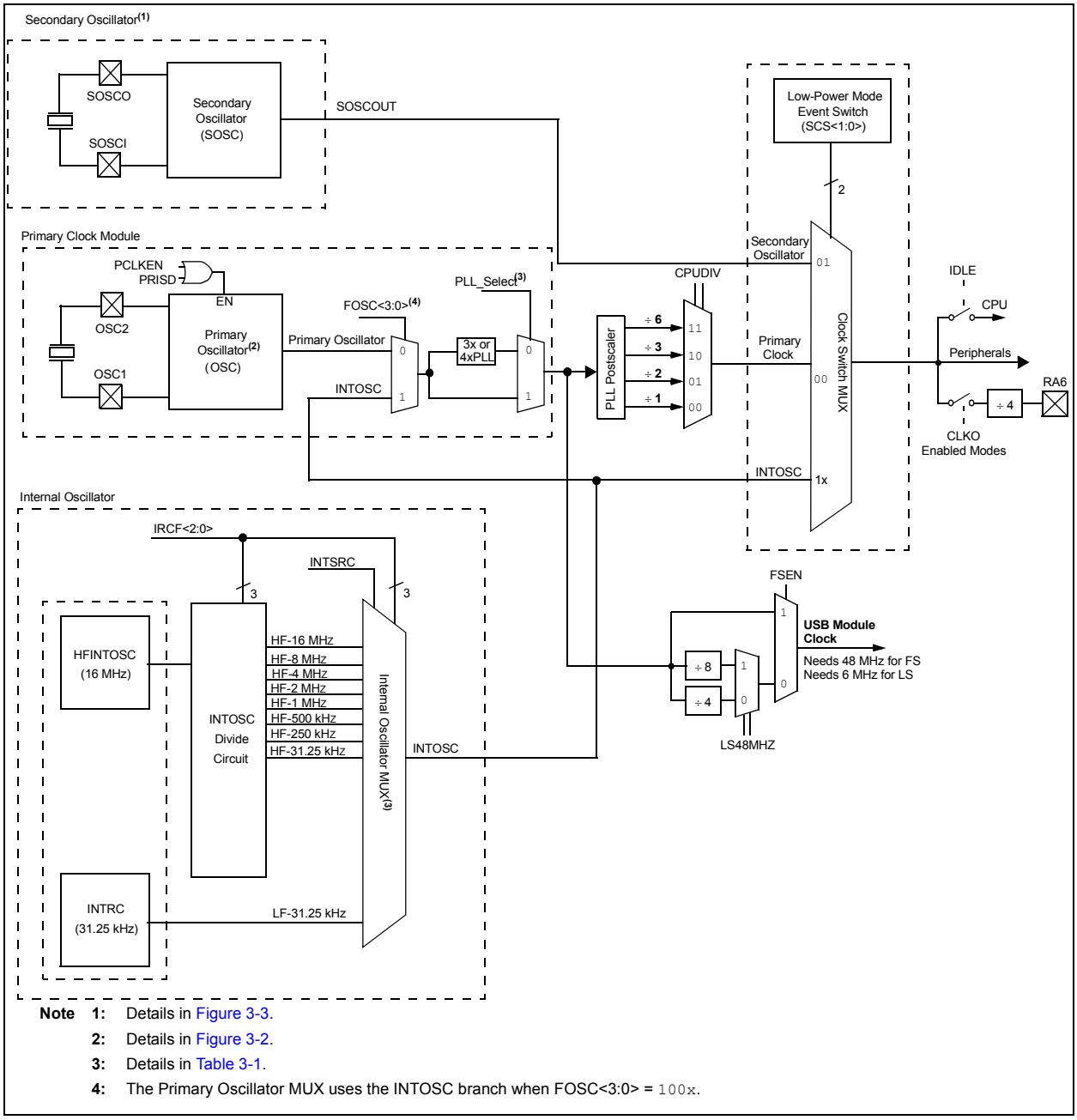
The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30684**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: CPU Divider

Figure 3-1 from **Section 3.1 "Overview"**, as well as Table 3-6 and Table 3-7 from **Section 3.14.1 "Low-Speed Operation"** have incorrect data on the CPUDIV Configuration bits. The corrected versions are below:

FIGURE 3-1: SIMPLIFIED OSCILLATOR SYSTEM BLOCK DIAGRAM



Note 1: Details in Figure 3-3.

2: Details in Figure 3-2.

3: Details in Table 3-1.

4: The Primary Oscillator MUX uses the INTOSC branch when FOSC<3:0> = 100x.

TABLE 3-6: CLOCK FOR LOW-SPEED USB

System Clock	CPUDIV<1:0>	Microcontroller Clock	LS48MHZ	USB Clock
48	11	**48/6 = 8 MHz**	1	48/8 = 6 MHz
48	10	**48/3 = 16 MHz**	1	48/8 = 6 MHz
48	01	**48/2 = 24 MHz**	1	48/8 = 6 MHz
48	00	**48 MHz**	1	48/8 = 6 MHz
24	11	**24/6 = 4 MHz**	0	24/4 = 6 MHz
24	10	**24/3 = 8 MHz**	0	24/4 = 6 MHz
24	01	**24/2 = 12 MHz**	0	24/4 = 6 MHz
24	00	**24 MHz**	0	24/4 = 6 MHz

TABLE 3-7: OSCILLATOR CONFIGURATION OPTIONS FOR USB OPERATION

Input Oscillator Frequency	Clock Mode (FOSC<3:0>)	MCU Clock Division (CPUDIV<1:0>)	Microcontroller Clock Frequency
48 MHz	EC	÷**6** (11)	**6 MHz**
		÷**3** (10)	**12 MHz**
		÷**2** (01)	**24 MHz**
		None (00)	**48 MHz**
16 MHz	EC, HS or INTOSC with 3xPLL	÷6 (11)	**6 MHz**
		÷**3** (10)	**12 MHz**
		÷**2** (01)	**24 MHz**
		None (00)	**48 MHz**
12 MHz	EC or HS with 4xPLL	÷6 (11)	**6 MHz**
		÷**3** (10)	**12 MHz**
		÷**2** (01)	**24 MHz**
		None (00)	**48 MHz**
24 MHz	EC or HS(1)	÷6 (11)	**4 MHz**
		÷**3** (10)	**8 MHz**
		÷**2** (01)	**12 MHz**
		None (00)	**24 MHz**

Note 1: The 24 MHz mode (without PLL) is only compatible with low-speed USB. Full-speed USB requires a 48 MHz system clock.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (08/2012)

Initial release of this document.

Rev B Document (11/2013)

Added Silicon Revision A2; Other minor corrections; Data Sheet Clarifications: Added Module 1 (CPU Divider).

Rev C Document (01/2014)

Added Module 2 (Timer1/3 Module with Gate Control); Other minor corrections.

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