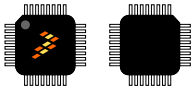
MCR20AVHM Data Sheet

Low power, high-performance 2.4 GHz IEEE 802.15.4 compliant transceiver with connectivity

MCR20AVHM



32 LGA
5 x 5 mm

The MCR20AVHM transceiver (or MCR20A) is a low power, high-performance 2.4 GHz, IEEE 802.15.4 compliant transceiver with connectivity to a broad range of microcontrollers, including the Kinetis family of products.

The MCR20AVHM transceiver enables development of proprietary and standard 802.15.4 based communication protocols such as SMAC, IEEE802.15.4 PHY-MAC, Thread, ZigBeePRO, RF4CE, and others.

Typical applications include Home Area Networks consisting of meters, gateways, in-home displays, and connected appliances, and also networked building control, home automation applications with lighting control, HVAC, and security and remote controls for home entertainment products.

Transceiver Performance
- 2.4 GHz (2360 to 2480 MHz) covers ISM band
- Fractional-N PLL supports 1 MHz and 5 MHz channels
- 250 kbps data rate
- OQPSK modulation
- Programmable output power
- -102 dBm RX sensitivity

Standards
- 802.15.4 Compliant Transceiver
- Thread, IPv6-6LoWPAN

Transceiver Features
- Hardware acceleration for IEEE 802.15.4 2006 packet processing
- Support for Dual PAN mode
- Onboard trim of reference crystal
- 128-byte RAM data buffer
- Low-power operating modes with single SPI command device wake-up
- On-chip voltage regulators
- Clear Channel Assessment, Energy Detect, Link Quality Indicator

Radio peripherals
- 24-bit event timer with interrupts
- Eight (8) software programmable GPIOs
- Control port for antenna diversity mode or external PA and LNA

Microcontroller Interface
- Programmable frequency clock output (CLK_OUT)
- SPI command channel and interface
- Interrupt request output

Operating Characteristics
- 1.8 V to 3.6 V operating voltage
- 17mA TX, 19mA RX, < 1mA idle/doze, < 1uA hybernate typical current
- operational temperature range : –40°C to +105°C

Physical Characteristics
- RoHS compliant, 5 mm x 5 mm, 32-pin MLGA package
- Small RF footprint, low component count

Ordering Information

Device	Operating Temp Range (T_A)	Package	Description
MCR20AVHM	-40 deg C to +105 deg C	MLGA-32	IEEE 802.15.4 - 2.4 GHz ISM Band

Table of Contents

1 Transceiver Description

1.1 Transceiver Architecture

As the figure shows, the MCR20A transceiver consists of a receive RF and analog path, demodulation circuitry, Phased Locked Loop synthesizer (which serves as both the local oscillator for the receiver and the exciter of the transmitter), a power amplifier completes the transmit path, a crystal oscillator to provide the reference, a group of voltage regulators to provide regulated power to internal circuits, blocks of logic to provide control signals or TR switching and diversity antenna selection as well as GPIOs, and digital manager block and MCU interface.

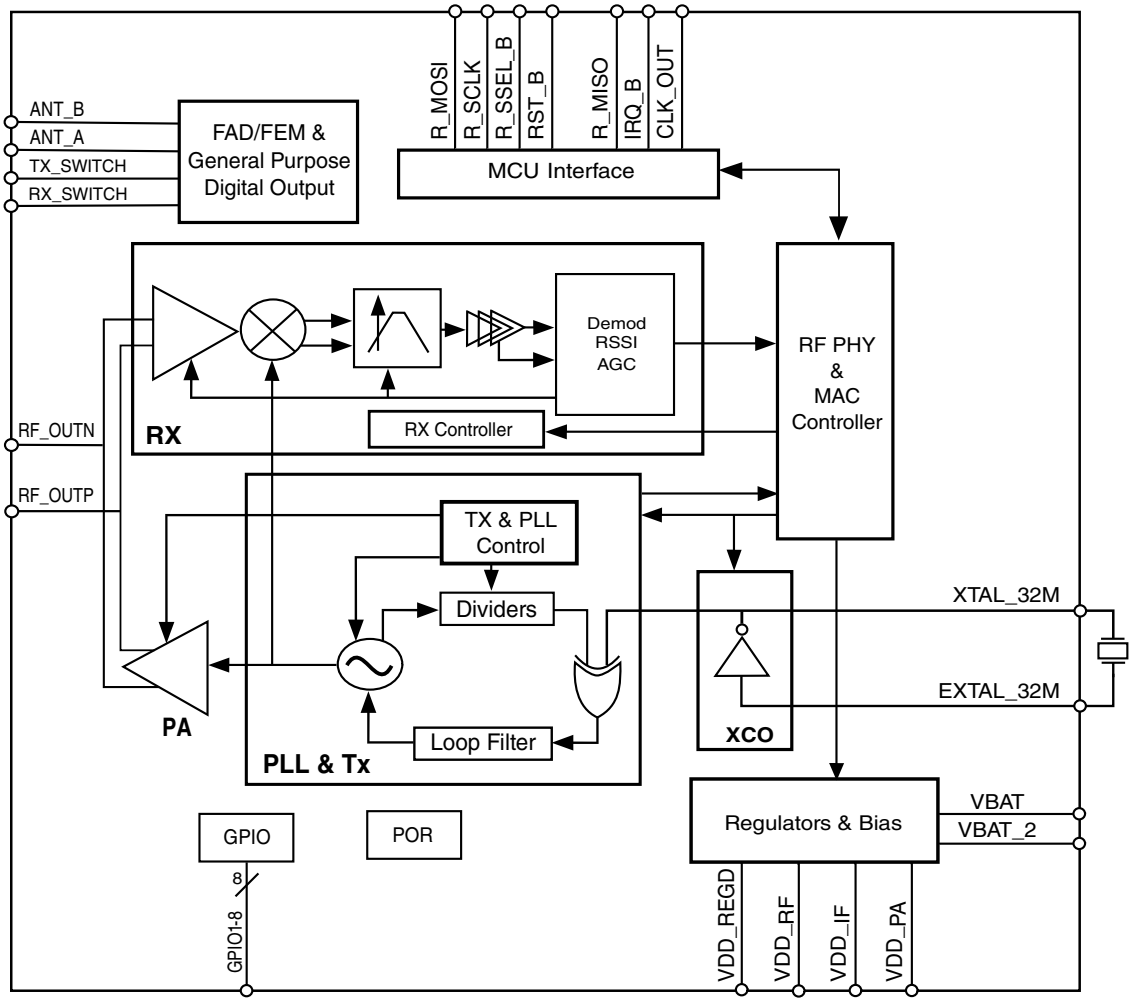


Figure 1. MCR20A Transceiver Simplified Block Diagram

Each of the blocks is described in more detail in the following sections.

1.2 RF interface and usage

The RF output ports are bidirectional (diplexed between receive/transmit modes) and differential enabling interfaces with numerous off-chip devices such as a balun. When using a balun, the MCR20A transceiver provides an interface to directly connect between a single-ended antenna and the RF ports. In addition, the MCR20A transceiver provides four output driver ports that can have both drive strength and slew rate configured to control external peripheral devices. These signals designated as ANT_A, ANT_B, RX_SWITCH, and TX_SWITCH when enabled are switched via an internal hardware state machine.

1.2.1 Radio to MCU interface

An array of microcontrollers can be supported through the use of dedicated I/Os that route from the package.

This figure shows the interconnection of the MCR20A transceiver and a generic MCU. The *MCR20A Reference Manual* provides more detailed information describing the functionality and connections between the radio and MCU.

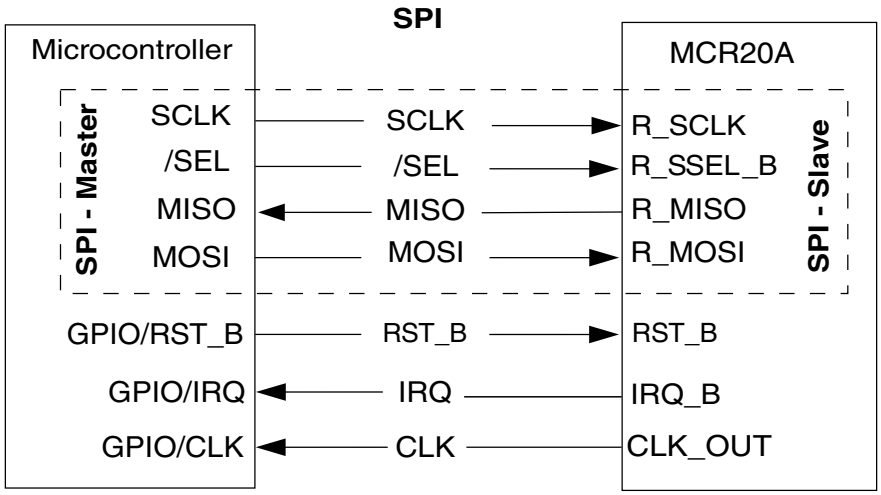


Figure 2. MCU to MCR20A block diagram

1.2.1.1 SPI interface

Microcontroller communication with the MCR20A transceiver is through a 4-wire serial peripheral interface (SPI). Exclusive access to the MCR20A transceiver's register set and packet buffer is provided by the SPI. For specific SPI interface information refer to the SPI section.

1.2.1.2 IRQ management

The MCR20A transceiver has up to 14 individual sources of interrupt requests to the MCU (see Table 1). These are all capable of individual control, and are logically OR-combined to drive a single, active low, interrupt request pin (IRQ_B) to the external MCU. Features supported are:

- The IRQ_B pin can be configured as actively-driven high or open-drain.
- Each interrupt source has its own interrupt status bit in the MCR20A transceiver's direct register space.
- Each interrupt can be individually controlled by an interrupt mask—The IRQ is issued when the mask is cleared to 0.
- There is also a global interrupt mask, TRCV_MSK, which can enable or disable all IRQ_B assertions by programming a single masking bit.
- All status bits use a write-1-to-clear protocol—interrupt status bits are not affected by reads.
- IRQ_B will remain asserted until all active interrupt sources are cleared or masked.

Table 1. IRQ sources

MCR20A interrupt sources
SEQIRQ
TXIRQ
RXIRQ
CCAIRQ
RXWTRMRKIRQ
FILTERFAIL_IRQ
PLL_UNLOCK_IRQ
WAKE_IRQ
PB_ERR_IRQ
AES_IRQ
TMR1IRQ
TMR2IRQ
TMR3IRQ
TMR4IRQ

Any or all of the interrupt sources, can be enabled to cause an assertion on IRQ_B.

1.2.1.3 Memory map and registers

Numerous register bits are provided to control interrupt behavior within the MCR20A transceiver. Detailed information for memory map and registers is located in the *MCR20A Reference Manual*.

1.2.2 Clock output feature

The CLK_OUT digital output can be enabled to drive the system clock to the MCU. This provides a highly accurate clock source based on the transceiver reference oscillator. The clock is programmable over a wide range of frequencies divided down from the reference 32 MHz (see Table 4). The frequency of CLK_OUT will be determined by the state of the GPIO5/BOPT (boot option) pin. If this pin is low upon POR, then the frequency will be 4 MHz (32 MHz/8). If this pin is high upon POR (GPIO5 has a pullup resistor) then the frequency will be 32.78689 kHz (32 MHz/976).

1.3 Transceiver Functions

1.3.1 Receive

The receiver has the functionality to operate in either normal run state or low power run state that can be considered as a partial power down mode. Low power run state can save a considerable amount of current by duty-cycling some sections of the receiver lineup during preamble search and is referred to as low power preamble search mode (LPPS).

The radio receiver path is based upon a near zero IF (NZIF) architecture incorporating front end amplification, one mixed-signal down conversion to IF that is programmably filtered, demodulated, and digitally processed. The RF front end (FE) input port is differential and shares the same off-chip matching network with the transmit path.

1.3.2 Transmit

The MCR20A transceiver transmits OQPSK modulation adjusting power and channel selection determined by the user's application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RFOUTP, RFOUTN) are converted as single ended (SE) signals with off-chip components as required.

1.3.3 PLL Synthesizer

The MCR20A Phase Locked Loop synthesizer provides a signal to either the transmit PA or the receive mixer. The reference is derived from the (typically 32 MHz) crystal oscillator. The PLL divider is a Fractional-N type with a step size of Fref/65536 or 488Hz with a 32 MHz reference.

After the channel of operation is determined, coarse and fine tuning is executed within the Fractional-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. Unlock detect circuitry drives an abort of the transceiver sequence in the event of abnormal behavior and asserts an interrupt. Modulation is performed inside the PLL during transmit and the modulated signal is routed to the PA. This signal is not modulated in receive and the carrier routed to the receive mixer.

1.3.4 Low power preamble search (LPPS)

The MCR20A transceiver provides a unique low power preamble search (LPPS) in the receive mode operation. A summary of this mode of operation when selected is described as follows:

- Whenever a receive cycle is initiated, the receiver is not turned fully on to save current until receive energy of a preset level is detected.
- The receiver will turn fully on only when triggered by energy at a pre-determined preset level thus enabling reception of the expected frame. Afterwards, the receiver will begin operating in the full-on state that is considered to be the same as the standard receive state.
- The preset level can be programmed for various receiver input power levels.

Use of the LPPS mode provides two distinct advantages:

- Reduced “listen” mode current—The receive current is significantly reduced while waiting for a frame. If a node is a coordinator, router, or gateway and it spends a significant percentage of its RF-active time waiting for incoming frames from clients or other devices, the net power savings can be significant.
- Reduced sensitivity as a desired effect—The LPPS mode provides different levels of reduced sensitivity. If a node operates in a densely populated area, it may be desirable to de-sensitize the receiver such that the device does not respond to incoming frames with an energy level below the desired threshold. This could be useful for security, net efficiency, reduced noise triggering, and many other purposes.

1.3.5 Clear channel assessment (CCA), energy detection (ED), and link quality indicator (LQI)

The MCR20A transceiver supports three clear channel assessment (CCA) modes of operation including energy detection (ED) and link quality indicator (LQI). Functionality for each of these modes is as follows.

1.3.5.1 CCA mode 1

CCA mode 1 has two functions:

- To estimate the energy in the received baseband signal. This energy is estimated based on the receiver signal strength indicator (RSSI).
- To determine whether the energy is greater than a set threshold.

The estimate of the energy can also be used as the link quality metric. In CCA mode 1, the MCR20A transceiver must warm-up from idle to receive mode where RSSI averaging takes place.

1.3.5.2 CCA mode 2

CCA mode 2 detects whether there is any 802.15.4 signal transmitting in the frequency band that an 802.15.4 transmitter intends to transmit. From the definition of CCA mode 2 in the 802.15.4 standard, the requirement is to detect an 802.15.4 complied signal. Whether the detected energy is strong or not is not important for CCA mode 2.

1.3.5.3 CCA mode 3

CCA mode 3 as defined by the 802.15.4 standard is implemented using a logical combination of CCA mode 1 and CCA mode 2. Specifically, CCA mode 3 operates in one of two operating modes:

- CCA mode 3 is asserted if both CCA mode 1 and CCA mode 2 are asserted.
- CCA mode 3 is asserted if either CCA mode 1 or CCA mode 2 is asserted.

This mode setting is available through a programmable register.

1.3.5.4 Energy detection (ED)

Energy detection (ED) is based on receiver signal strength indicator (RSSI) and correlator output for the 802.15.4 standard. ED is an average value of signal strength. The magnitude from this measurement is calculated from the digital RSSI value that is averaged over a 128 μs duration.

1.3.5.5 Link quality indicator (LQI)

The link quality indicator (LQI) is based on the receiver signal strength indicator (RSSI) or correlator output for the 802.15.4 standard. In this mode, the RSSI measurement is calculated during normal packet reception. LQI computations for the MKW20 transceiver are based on either digital RSSI or correlator peak values. This setting is executed through a register bit where the final LQI value is available 64 μs after preamble is detected. If a continuous update of LQI based on RSSI throughout the packet is desired, it can be read in a separate 8-bit register by enabling continuous update in a register bit.

1.3.5.6 LQI ED RSSI

The following figure shows the MCR20A transceiver's reported energy detect (ED) as a function of input power. The figure also shows the link quality indication (LQI)/ RSSI_CONT (continuous) and the RSSI as a function of a unitless numeric register reading. LQI is available 64 μs after the preamble is detected. RSSI_CONT can be used to read LQI when a continuous value averaged over the entire received packet is desired. This value may be read as LQI if continuous update of LQI is desired during packet reception (both scaled the same but averaged differently). The curves are measured using the default offset compensation value and can be changed to center the curve if desired.

The following sequences are performed in test software to create the curves that are shown in the figure. Similar sequences are incorporated into NXP software stacks.

- For ED, the device is configured to perform an ED via write to the register 0x7 with 0x00.
  - ED/CCA sequence is started via write to register 0x3 with 0x3
  - Register 0 is polled for bit 3 to be set
  - RSSI_CONT_EN bit is disabled in indirect 0x25 (CCA_CTRL) all other bits are reset/overwrite values
  - Direct register 0x0B is read (CCA final)
  - Direct register 0x25 is read (LQI)
  - Indirect register 0x5B is read (RSSI)
  - Direct register 0x26 is read (RSSI_CONT), however, not enabled in ED case so ignored
- For LQI, the device is configured to perform an LQI via write to the register 0x7 with 0x00.
  - The device is configured to perform an LQI via write to the register 0x7 with 0x00
  - Receive sequence is started via write to register 0x3 with 0x1
  - Register 0 is polled for bit 2 to be set
  - RSSI_CONT_EN bit is enabled in indirect 0x25
  - RSSI_CONT_EN bit is disabled in indirect 0x25 (CCA_CTRL) all other bits are reset or overwrite values
  - Direct register 0x0B is read (CCA final)
  - Direct register 0x25 is read (LQI)
  - Indirect register 0x5B is read (RSSI)
  - Direct register 0x26 is read (RSSI_CONT), valid for LQI

For both LQI and ED the input power is swept with a modulated input signal from -100 dBm to -20 dBm in steps of 1 dBm and the ED and LQI sequences are called during each step and the results recorded.

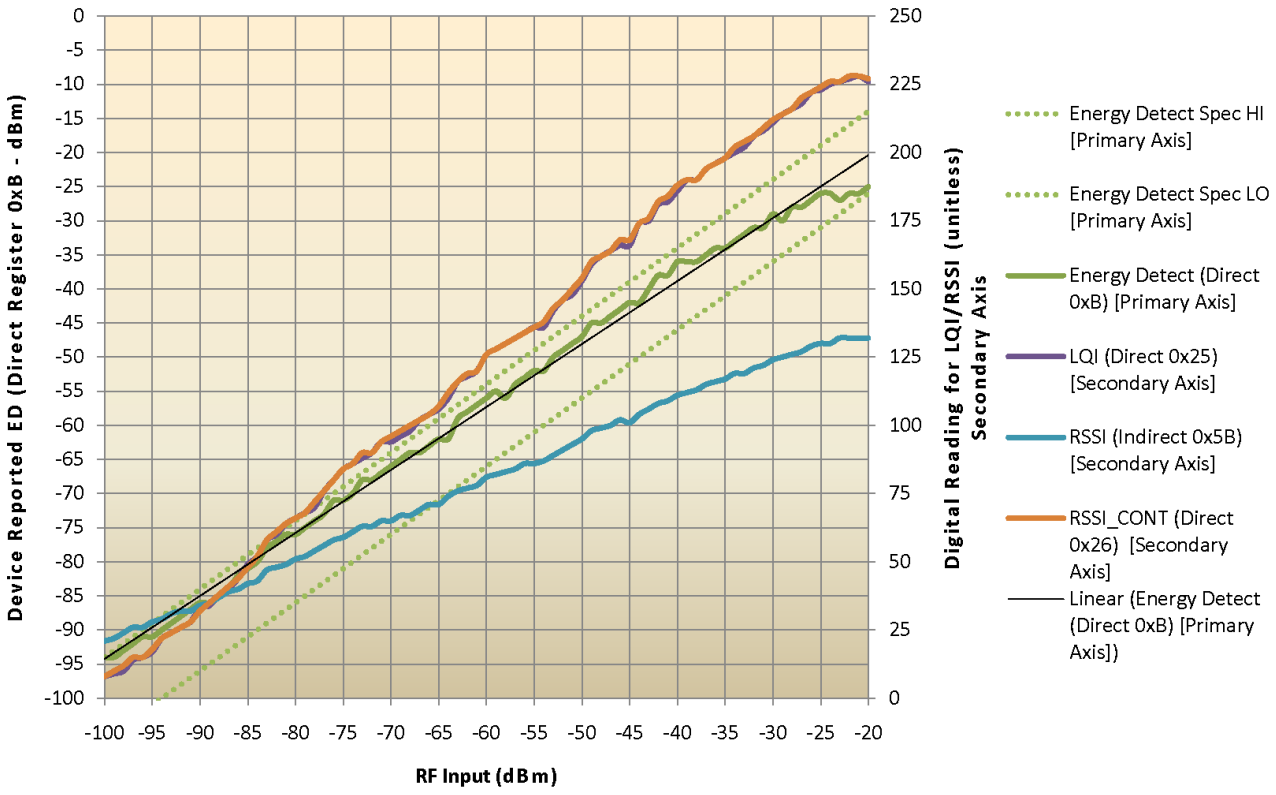


Figure 3. ED/LQI relation to RSSI/RSSI_CONT

Based on the figure, an equation can be derived as follows. Using Y(LQI) and X(RF), the minimum and maximum values from the secondary axis are determined as:

Table 2. Minimum and Maximum Values

LQI	Y(LQI)	X(RF)
Maximum	225	-25
Minimum	12	-100
Dynamic range mid point	125	-60

Therefore the slope = 2.84 and B = 295.4. So to convert the 8-bit unitless number read from direct register 0x25 to an ideal RF equivalent, use the following equation:

RF = (LQI – 295.4) / 2.84

1.3.6 IEEE 802.15.4 acceleration hardware

The 802.15.4 transceiver integrates (as listed below) hardware features that reduce the software stack size, off-loads functions from the CPU, supports security and improves performance:

- Complete IEEE®802.15 modem
- 2006 packet processor/sequencer
- Internal event timer block with four comparators to assist sequencer and provide timer capability.

1.3.7 Packet processor

The MCR20A transceiver's packet processor performs sophisticated hardware filtering of the incoming received packet to determine whether the packet is both PHY- and MAC-compliant, is addressed to this device, if the device is a PAN coordinator, and whether a message is pending for the sending device. The packet processor greatly reduces the packet filtering burden on software enabling it to tend to higher-layer tasks with a lower latency and smaller software footprint.

1.3.7.1 Features

The MCR20A transceiver's packet processor has the following features:

- Aggressive packet filtering to enable long, uninterrupted MCU sleep periods
- Fully compliant with both 2003 and 2006 versions of the 802.15.4 wireless standard
- Supports all frame types, including reserved types
- Supports all valid 802.15.4 frame lengths
- Enables auto-Tx acknowledge frames (no MCU intervention) by parsing of frame control field and sequence number
- Supports all source and destination address modes, and also PAN ID compression
- Supports broadcast address for PAN ID and short address mode
- Supports “promiscuous” mode, to receive all packets regardless of address- and rules-checking
- Enables frame type-specific filtering—that is, it rejects all but beacon frames
- Supports SLOTTED and non-SLOTTED modes

- Includes special filtering rules for PAN coordinator devices
- Enables minimum-turnaround transmit-acknowledge frames for data-polling requests by automatically determining message-pending status
- Assists the MCU to locate pending messages in its indirect queue for data-polling end devices
- Makes available to MCU detailed status of frames that fail address-checking or rules-checking
- Supports dual PAN mode, to enable the device to exist on two PANs simultaneously
- Supports two IEEE addresses for the device
- Supports active promiscuous mode

1.3.8 Packet buffering

The packet buffer is a 128-byte random access memory (RAM) dedicated to the storage of 802.15.4 packet contents for both transmit and receive sequences. For transmit sequences, software stores the contents of the packet buffer starting with the frame length byte at packet buffer address 0 followed by the packet contents at the subsequent packet buffer addresses. For receive sequences, the incoming packet's frame length is stored in a register external to the packet buffer. Software will read this register to determine the number of bytes of packet buffer to read. This facilitates DMA transfer through the SPI. For receive packets, an LQI byte is stored at the byte immediately following the last byte of the packet (frame length +1). Usage of the packet buffer for receive and transmit sequences is on a time-shared basis—that is, the receive packet data will overwrite the contents of the packet buffer. Software can inhibit receive-packet overwriting of the packet buffer contents by setting the PB_PROTECT bit. This will block receive packet overwriting, but will not inhibit transmit content loading of the packet buffer via the SPI.

1.3.8.1 Features

The features of the packet buffer are as follow:

- 128 byte buffer stores maximum length 802.15.4 packets
- Same buffer serves both transmit and receive sequences

- The entire packet buffer can be uploaded or downloaded in a single SPI burst
- Automatic address auto-incrementing for burst accesses
- Single-byte access mode supported
- Entire packet buffer can be accessed in hibernate mode
- Under-run error interrupt supported

1.4 Dual PAN ID

In the past, radio transceivers designed for 802.15.4 and ZigBee applications allowed a device to associate to one and only one Personal Area Network (PAN) at any given time. The MCR20A transceiver represents a high-performance radio that includes hardware support for a device to reside in two networks simultaneously. In optional dual PAN mode, the device alternates between the two PANs under hardware or software control. Hardware support for dual PAN operation consists of two sets of PAN and IEEE addresses for the device, two different channels (one for each PAN), and a programmable timer to automatically switch PANs (including on-the-fly channel changing) without software intervention. There are control bits to configure and enable dual PAN mode, and read only bits to monitor status in dual PAN mode. A device can be configured to be a PAN coordinator on either network, both networks, or neither network.

For the purpose of defining PAN in the context of dual PAN mode, two sets of network parameters are maintained; PAN0 and PAN1. PAN0 and PAN1 will be used to refer to the two PANs where each parameter set uniquely identifies a PAN for dual PAN mode. These parameters are described in Table 3.

Table 3. PAN0 and PAN1 descriptions

PAN0	PAN1
Channel0 (PHY_INT0, PHY_FRAC0)	Channel1 (PHY_INT1, PHY_FRAC1)
MacPANID0 (16-bit register)	MacPANID1 (16-bit register)
MacShortAddrs0 (16-bit register)	MacShortAddrs1 (16-bit register)
MacLongAddrs0 (64-bit registers)	MacLongAddrs1 (64-bit registers)
PANCORDNTR0 (1-bit register)	PANCORDNTR1 (1-bit register)

During device initialization when dual PAN mode is used, software will program both parameter sets to configure the hardware for operation on two networks.

1.4.1 Event Timer

The MCR20A transceiver features a 24-bit event timer that can be used in conjunction with the sequencer to provide protocol control as well as timing interrupts. The event timer consists of a continuously running counter and four separate 24-bit comparators.

The event timer functionality:

- The event timer counter runs at the 802.15.4 bit rate of 250 kHz (programmable).
- Each comparator has an individual interrupt request capability—the compare status is set when there is a match between the comparator and the timer counter. Each status can be enabled to generate an IRQ.
- A separate 16-bit T2PRIMECMP comparator is provided, which uses only the lower 16 bits of the event timer rather than requiring a full 24-bit compare.

For each timer compare enable, when the bit is set, a match on the respective 24-bit compare value to the event timer will cause the corresponding interrupt status bit to become set. If the compare enable is low, then the event timer matches prevent the corresponding interrupt status bit to become set.

2 System and power management

The MCR20A transceiver is a low power device that also supports extensive system control and power management modes to maximize battery life and provide system protection.

2.1 Modes of operation

The transceiver modes of operation include:

- Idle mode
- Doze mode
- Low power (LP) / hibernate mode
- Reset / powerdown mode
- Run mode

2.2 Power management

The MCR20A transceive's power management is controlled by programming the modes of operation. Different modes enable different levels of power-down and run operation. For the receiver, the programmable power modes available are:

- Preamble search
- Preamble search sniff
- Low power preamble search (LPPS)
- Fast antenna diversity (FAD) preamble search
- Packet decoding

3 Radio Peripherals

The MCR20A transceiver provides a set of I/O pins to supply a system clock to the MCU, to control the external RF modules and circuitry, and to control the GPIO.

3.1 Clock output (CLK_OUT)

The MCR20A transceiver integrates a programmable clock to source numerous frequencies for connection with various MCUs. Package pin 16 can be used to provide this clock source as required to enable the user to make adjustments per their application requirements.

Care must be taken that the clock output signal does not interfere with the reference oscillator or the radio. Additional functionality this feature supports is:

- XTAL domain can be completely gated off (hibernate mode)
- SPI communication allowed during hibernation

Table 4. CLK_OUT table

CLK_OUT_DIV [2:0]	CLK_OUT frequency
0	32 MHz[1]

Table continues on the next page...

Table 4. CLK_OUT table (continued)

CLK_OUT_DIV [2:0]	CLK_OUT frequency
1	16 MHz[1]
2	8 MHz[1]
3	4 MHz [2]
4	2 MHz
5	1 MHz
6	62.5 kHz
7	32.786 kHz [3]

1. May require high drive strength for proper signal integrity.
2. DEFAULT if GPIO5/BOPT = 0
3. DEFAULT if GPIO5/BOPT = 1

There is an enable/disable bit for CLK_OUT. When disabled, the clock output will optionally continue to run for 128 clock cycles after it is disabled. There is also one bit available to adjust the CLK_OUT I/O pad drive strength.

3.2 General-purpose input output (GPIO)

The MCR20A transceiver supports 8 GPIO pins. All I/O pins will have the same supply voltage and depending on the supply, can vary from 1.8 V up to 3.6 V. When the pin is configured as a general-purpose output or for peripheral use, there will be specific settings required per use case. Pin configuration will be executed by software to adjust input/output direction and drive strength capability. When the pin is configured as a general-purpose input or for peripheral use, software (see Table 5) can enable a pull-up or pull-down device. Immediately after reset, all pins are configured as high-impedance general-purpose inputs with internal pull-up devices enabled.

Features for these pins include:

- Programmable output drive strength
- Programmable output slew rate
- Hi-Z mode
- Programmable as outputs or inputs (default)

Table 5. Pin configuration summary

Pin function configuration	Details	Tolerance			Units
		Min.	Typ.	Max.	
I/O buffer full drive mode[1]	Source or sink	—	±10	—	mA
I/O buffer partial drive mode[1]	Source or sink	—	±2	—	mA
I/O buffer high impedance[2]	Off state	—	—	10	nA
No slew, full drive	Rise and fall time[3]	2	4	6	ns
No slew, partial drive	Rise and fall time	2	4	6	ns
Slew, full drive	Rise and fall time	6	12	24	ns
Slew, partial drive	Rise and fall time	6	12	24	ns
Propagation delay[4], no slew	Full drive[5]	—	—	11	ns
Propagation delay, no slew	Partial drive[6]	—	—	11	ns
Propagation delay, slew	Full drive	—	—	50	ns
Propagation delay, slew	Partial drive	—	—	50	ns

1. For this drive condition, the output voltage will not deviate more than 0.5 V from the rail reference VOH or VOL.
2. Leakage current applies for the full range of possible input voltage conditions.
3. Rise and fall time values in reference to 20% and 80%
4. Propagation Delay measured from/to 50% voltage point.
5. Full drive values provided are in reference to a 75 pF load.
6. Partial drive values provided are in reference to a 15 pF load.

3.2.1 Serial peripheral interface (SPI)

The MCR20A transceiver's SPI interface enables an MCU to communicate with the radio's register set and packet buffer. The SPI is a slave-only interface—that is, the MCU must drive R_SSEL_B, R_SCLK, and R_MOSI. Write and read access to both direct and indirect registers is supported, and transfer length can be single-byte or bursts of unlimited length. Write and read access to the packet buffer can also be single-byte or a burst mode of unlimited length.

The SPI interface is asynchronous to the rest of the MCR20A transceiver. No relationship between R_SCLK and the internal oscillator is assumed. And no relationship between R_SCLK and the CLK_OUT pin is assumed. All synchronization of the SPI interface to the MCR20A transceiver occurs within the SPI module. SPI synchronization occurs in both directions; register writes and register reads. The SPI is capable of operation in all power modes except Reset. Operation in hibernate mode enables most transceiver registers and the complete packet buffer to be accessed in the lowest-power operating state enabling minimal power consumption, especially during the register-initialization phase of the radio.

The SPI design features a compact, single-byte control word, reducing SPI access latency to a minimum. Most SPI access types require only a single-byte control word, with the address embedded in the control word. During control word transfer (the first byte of any SPI access), the contents of the IRQSTS1 register (the radio's highest-priority status register) are always shifted out so that the MCU obtains access to IRQSTS1, with the minimum possible latency, on every SPI access.

3.2.1.1 Features

The SPI interface features:

- 4-wire industry standard interface, supported by all MCUs
- SPI R_SCLK maximum frequency 16 MHz (for SPI write accesses)
- SPI R_SCLK maximum frequency 9 MHz (for SPI read accesses)
- Write and read access to all radio registers (direct and indirect)
- Write and read access to packet buffer
- SPI accesses can be single-byte or burst
- Automatic address auto-incrementing for burst accesses
- Asynchronous mode
    - Entire packet buffer can be uploaded or downloaded in a single SPI burst
    - Entire packet buffer and most registers can be accessed during hibernation mode
    - All GPIO-related registers are accessible in hibernation mode
- Built-in synchronization inside the SPI module to or from the rest of the radio
- R_MISO can be tristated when the SPI is inactive, enabling multi-slave configurations

3.2.2 Antenna diversity

To improve the reliability of RF connectivity to long range applications, the antenna diversity feature is supported without using the MCU through use of four dedicated control pins (package pins 23, 24, 25, and 26).

Fast antenna diversity (FAD) mode supports this radio feature and, when enabled, allows the selection between two antennas during the preamble phase. By continually monitoring the received signal, the FAD block will select the first antenna of which the received signal has a correlation factor above a predefined progammable threshold. The FAD accomplishes the antenna selection by sequentially switching between the two antennas testing for the presence of suitably strong s0 symbol where the first antenna to reach this condition is then selected for the reception of the packet. Note that the antenna with the strongest signal is not necessarily picked but the antenna that first meets the signal requirements.

Each of the antennas are monitored for a period of 28 µs. The antenna switching is continued until 1.5 valid s0 symbols are detected. The demodulator then continues with normal preamble search before declaring *Preamble Detect*.

3.2.3 RF Output Power Distribution

The following figure shows the linear region of the output and the typical power distribution of the radio as a function of PA_PWR [4:0] range. The PA_PWR [4:0] is the lower 5 bits of the PA_PWR 0x23 direct register and has a usable range of 3 to 31 decimal.

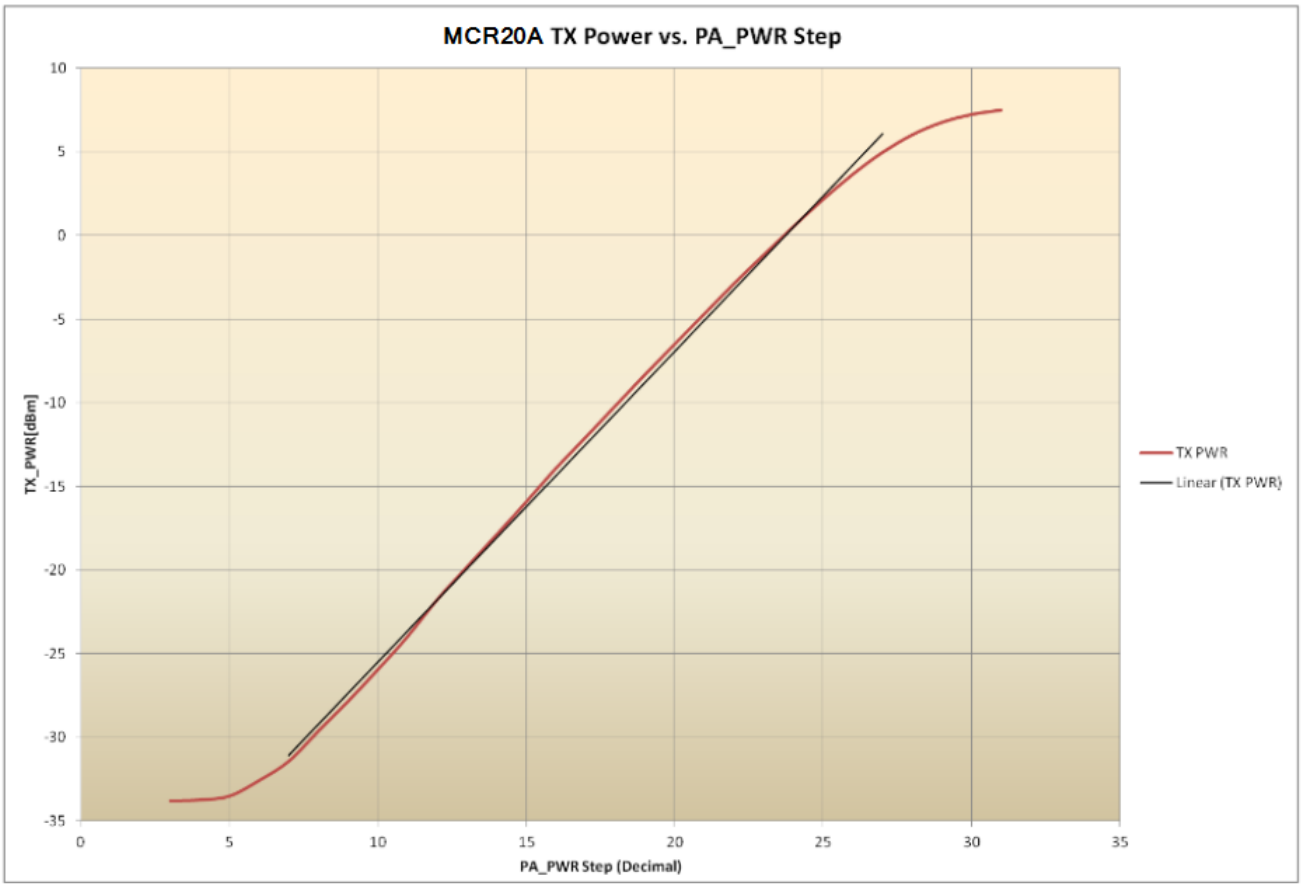


Figure 4. MCR20A transmit power vs. PA_PWR step

4 Serial peripheral interface (SPI)

The host microcontroller directs the MCR20A transceiver, checks its status, and reads/writes data to the device through the 4-wire SPI port. The transceiver operates as a SPI slave device only. A transaction between the host and the MCR20A transceiver occurs as multiple 8-bit bursts on the SPI. The SPI signals are:

- Slave select (R_SSEL_B)—A transaction on the SPI port is framed by the active low R_SSEL_B input signal.
- SPI clock (R_SCLK)—The host drives the SPICLK input to the MCR20A transceiver. Data is clocked into the master or slave on the leading (rising) edge of the return-to-zero SPICLK and data out changes state on the trailing (falling) edge of SPICLK.

NOTE

For Kinetis microcontrollers, the SPI clock format is the clock phase control bit CPHA=0 and the clock polarity control bit CPOL=0.

- Master out/slave in (MOSI)—Incoming data from the host is presented on the MOSI input.
- Master in/slave out (MISO)—The MCR20A transceiver presents data to the master on the MISO output.

The SPI interface is capable of operating with either the crystal oscillator ON (synchronous mode), or OFF (asynchronous mode; i.e., hibernate).

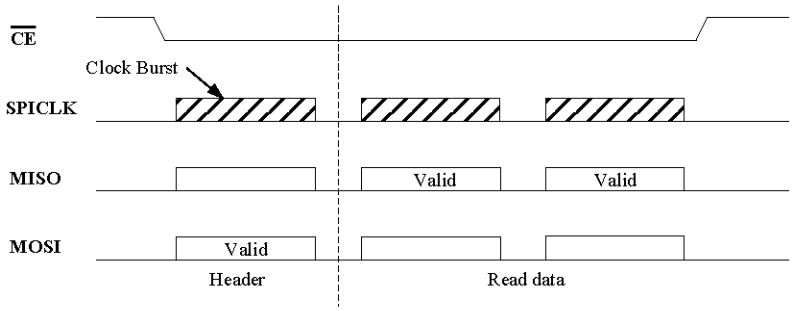


Figure 5. SPI read transaction diagram

4.1 SPI transfer protocol

The MCR20A transceiver's SPI is a slave-only interface, and follows a CPHA=0 and CPOL=0 protocol. Taken together, CPHA and CPOL determine the clock polarity and clock edge used to transfer data between the SPI master and slave, in both communication directions. CPHA=0 (clock phase) indicates that data is captured on the leading edge of SCK and changed on the following edge. CPOL=0 (clock polarity) indicates that the inactive state value of R_SCLK is low. All data is transferred MSB-first. The following diagram depicts the transfer protocol of the MCR20A transceiver's SPI.

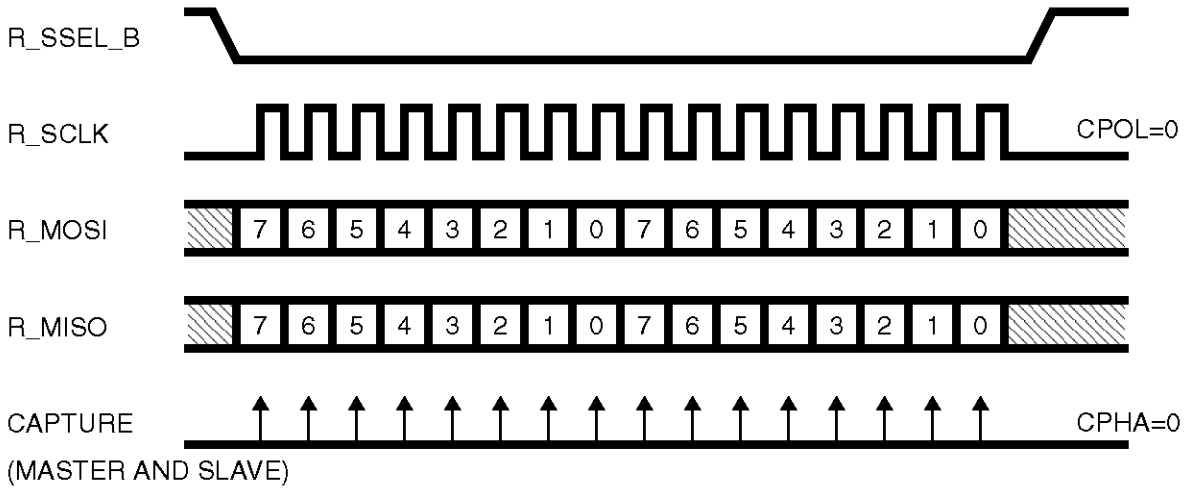


Figure 6. SPI Transfer Protocol

4.2 SPI control word

Every SPI transaction begins with one single-byte control word. The control word consists of the address, direction (write or read), transaction target (register or packet buffer), and for the packet buffer, the access mode (burst or byte). For most transactions, data transfer follows immediately after the control word. However, for indirect access register transactions, and for packet buffer byte-mode transactions, an additional address byte follows the control word, before data transfer begins. Bit 7 of the control word selects the transfer direction (1=READ, 0=WRITE). Bit 6 selects the transfer target (1=PACKET BUFFER, 0=REGISTER). For register accesses, the remaining bits select the register address. For packet buffer access, bit 5 selects the access mode (1=BYTE, 0=BURST). For packet buffer access, the remaining bits in the control word are reserved and ignored by the MCR20A transceiver. Details and examples of control word usage appear in the following sections. The following table depicts an overview of the control word.

Table 6. Control word overview

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access Mode	Access Type
1	0	Register address [5:0]						Register access	Read
0	0	Register address [5:0]							Write
1	1	0	Reserved					Packet buffer burst access	Read
0	1	0	Reserved						Write
1	1	1	Reserved					Packet bugger byte access	Read
0	1	1	Reserved						Write

5 MCR20A Operating Modes

The MCR20A transceiver has 6 primary operating modes:

- Reset or power down
- Low power (LP) or hibernate
- Doze (low power with reference oscillator active)
- Idle
- Receive
- Transmit

Table 7 lists and describes the transceiver's power modes and consumption.

Table 7. Transceiver power modes

Mode	Definition	Current consumption[1]
Reset / powerdown	All IC functions off, leakage only. $\overline{RST}$ asserted.	< 100 nA
Low power / hibernate	Crystal reference oscillator off (SPI is functional).	< 1 µA
Doze[2]	Crystal reference oscillator on with CLK_OUT output available only if selected.	500 µA (no CLK_OUT)
Idle	Crystal reference oscillator on with CLK_OUT output available only if selected.	700 µA[3] (no CLK_OUT)
Receive	Crystal reference oscillator on. Receiver on.	19 mA [3, 4] 15 mA, LPPS mode
Transmit	Crystal reference oscillator on. Transmitter on.	17 mA [3, 5]

1. Conditions: VBAT and VBAT_2 = 2.7 V, nominal process @ 25°C.
2. While in Doze mode, 4 MHz maximum frequency can be selected for CLK_OUT.
3. Typical.
4. Signal sensitivity = -102 dBm.
5. RF output = 0 dBm.

5.1 Transceiver Transmit Current Distribution

The following figure shows the relation between the transmit power generated by the radio and its current consumption.

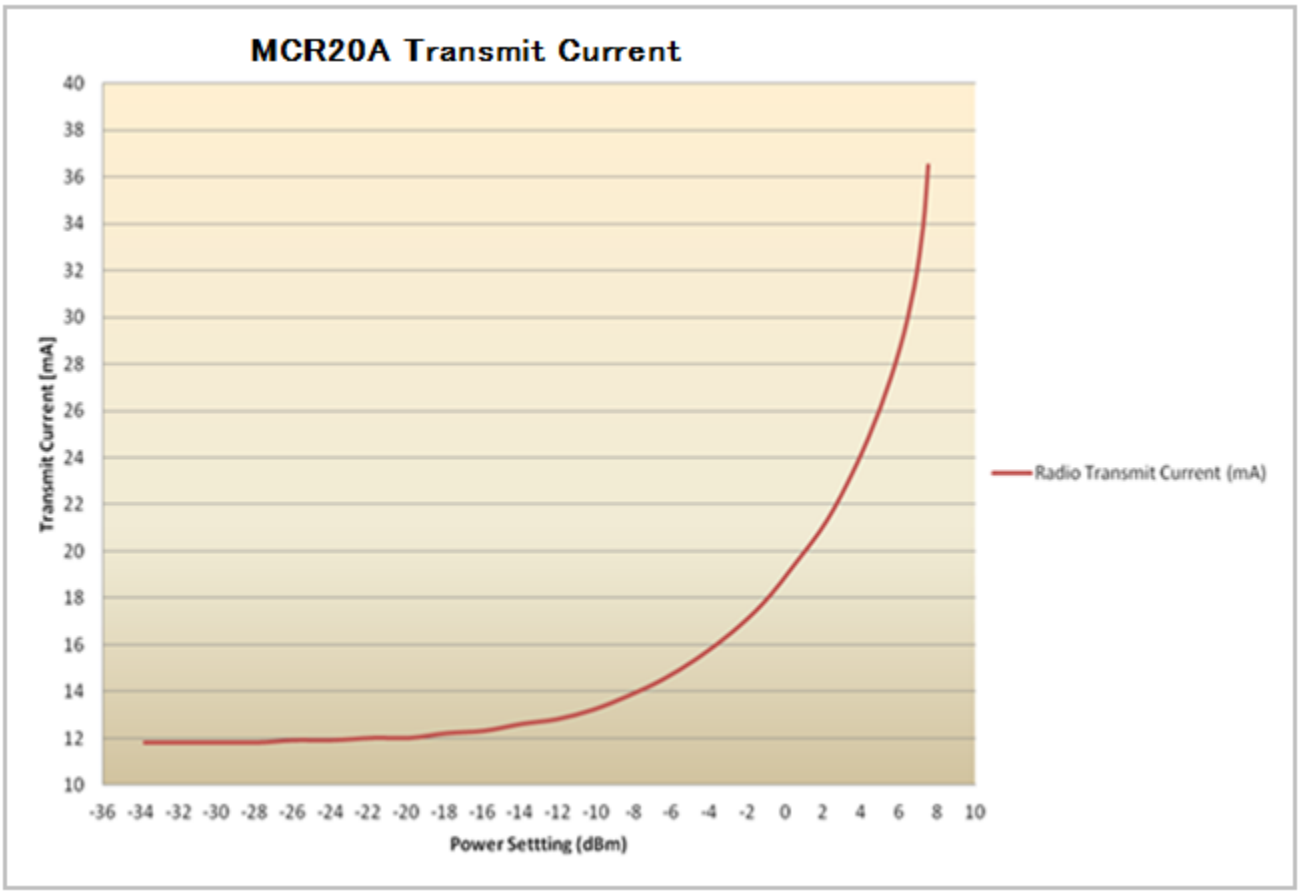


Figure 7. MCR20A transmit power vs transmit current

6 MCR20A Electrical Characteristics

6.1 Maximum ratings

Table 8. Maximum ratings

Requirement	Description	Symbol	Rating level	Unit
Power Supply Voltage		VBAT, VBAT2	-0.3 to 3.6	Vdc
Digital Input Voltage		Vin	-0.3 to (VDDINT[1] + 0.3)	Vdc
RF Input Power		Pmax	+10	dBm

Table continues on the next page...

Table 8. Maximum ratings (continued)

Requirement	Description	Symbol	Rating level	Unit
Note: Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics or recommended operating conditions tables.				
ESD[2]	Human Body Model	HBM	±2000	Vdc
	Machine Model	MM	±200	Vdc
	Charged Device Model	CDM	±750	Vdc
Junction Temperature		T_J	+125	°C
Storage Temperature Range		T_{stg}	-65 to +165	°C

1. Digital interface supply voltage (VDDINT). In this device it is required VBAT, VBAT2 are common and VBAT2 is equal to VDDINT and are supplied from a single un-regulated source.
2. Electrostatic discharge on all device pads meet this requirement

Note

Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics or recommended operating conditions tables.

6.2 Radio recommended operating conditions

Table 9. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BAT} = VDD_{INT})	V_{BAT}, VDD_{INT}	1.8	2.7	3.6	Vdc
Input Frequency	fin	2.360	—	2.480	GHz
Ambient Temperature Range	TA	-40	25	105	°C
Logic Input Voltage Low	VIL	0	—	30% VDDINT	V
Logic Input Voltage High	VIH	70% VDDINT	—	VDDINT	V
SPI Clock Rate	f_{SPI}	—	—	16.0	MHz
RF Input Power	Pmax	—	—	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	fref	32 MHz only			

6.3 Ratings

6.3.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.3.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.3.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

7 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

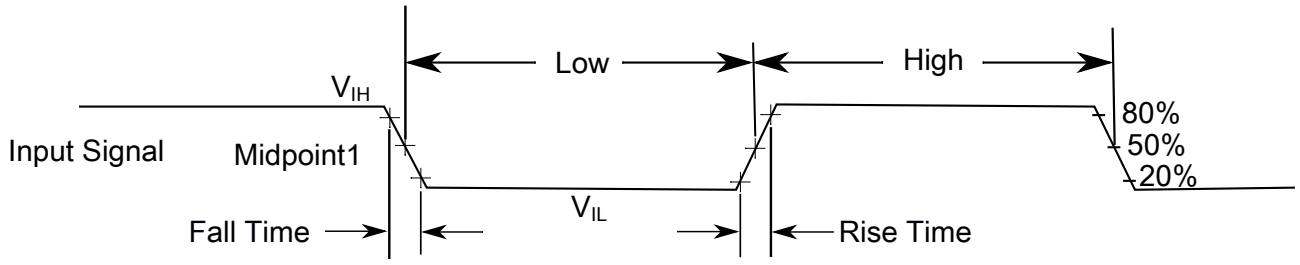


Figure 8. Input signal measurement reference

8 Nonswitching electrical specifications

8.1 EMC radiated emissions operating behaviors

Table 10. EMC radiated emissions operating behaviors 1

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	19	dBµV	2, 3
V_{RE2}	Radiated emissions voltage, band 2	50–150	21	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	19	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	11	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	L	—	3, 4

1. This data was collected on a MK20DN128VLH5 64pin LQFP device.
2. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
3. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 48 MHz, f_{BUS} = 48MHz
4. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

8.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to www.nxp.com.
- Perform a keyword search for “EMC design.”

8.3 Capacitance attributes

Table 11. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

9 Thermal specifications

9.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature[1]	–40	105	°C

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

10 Transceiver Electrical Characteristics

10.1 DC electrical characteristics

Table 13. DC electrical characteristics (V_{BAT}, V_{BAT2} = 2.7 V, T_A=25 °C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (VBAT + VBAT2)					
Reset / power down[1]	$I_{leakage}$	—	<60	<100	nA
Hibernate[1]	I_{CCH}	—	<1	—	µA
Doze (No CLK_OUT)	I_{CCD}	—	500	—	µA
Idle (No CLK_OUT)	I_{CCI}	—	700	—	µA
Transmit mode (0 dBm nominal output power)	I_{CCT}	—	17	18	mA
Receive mode (normal)	I_{CCR}	—	19	19.5	mA
Receive mode (power preamble search)			15 (LPPS)		
Input current (VIN = 0 V or VDDINT) (All digital inputs)	I_{IN}	—	—	±1	µA
Input low voltage (all digital inputs)	V_{IL}	0	—	30% V_{DDINT}	V
Input high voltage (all digital inputs)	V_{IH}	70% V_{DDINT}	—	V_{DDINT}	V
Output high voltage (IOH = -1 mA) (all digital outputs)	V_{OH}	80% V_{DDINT}	—	V_{DDINT}	V
Output low voltage (IOL = 1 mA) (all digital outputs)	V_{OL}	0	—	20% V_{DDINT}	V

1. To attain specified low power current, all GPIO and other digital IO must be handled properly.

10.2 AC electrical characteristics

Table 14. Receiver AC electrical characteristics (V_{BAT}, V_{DDINT} = 2.7 V, T_A=25 °C, f_{ref} = 32 MHz unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% packet error rate (PER) (–40 to +105 °C)[1]	SENSper	—	–99	–97	dBm
Sensitivity for 1% packet error rate (PER) (+25 °C)[1]	SENSper	—	–102	—	dBm
Saturation (maximum input level)	SENSmax	–10	—	—	dBm
Channel rejection for dual port mode (1% PER and desired signal –82 dBm)					
+5 MHz (adjacent channel)	—	—	39	—	dB

Table continues on the next page...

Table 14. Receiver AC electrical characteristics (V_{BAT}, V_{DDINT} = 2.7 V, T_A=25 °C, f_{ref} = 32 MHz unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
–5 MHz (adjacent channel)	—	—	33	—	dB
+10 MHz (alternate channel)	—	—	50	—	dB
–10 MHz (alternate channel)	—	—	50	—	dB
≥15 MHz	—	—	58	—	dB
Frequency error tolerance	—	—	—	200	kHz
Symbol rate error tolerance	—	80	—	—	ppm

1. Measurement is referenced to the package pin.

Table 15. Transmitter AC electrical characteristics (V_{BAT}, V_{DDINT} = 2.7 V, T_A=25 °C, f_{ref} = 32 MHz unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power spectral density, absolute limit from –40°C to +105°C	—	–30	—	—	dBm
Power spectral density, relative limit from –40°C to +105°C	—	–20	—	—	dB
Nominal output power[1]	Pout	–2	0	2	dBm
Maximum output power[1]	—	—	8	—	dBm
Error vector magnitude	EVM	—	8	13	%
Output power control range[2]	—	—	40	—	dB
Over the air data rate	—	—	250	—	kbps
2nd harmonic[3]	—	—	<–50	<–40	dBm
3rd harmonic[3]	—	—	<–50	<–40	dBm

1. Measurement is referenced to the package pin.
2. Measurement is referenced to the package pin on the output of the Tx/Rx switch. It does not degrade more than ±2 dB across temperature and an additional ±1 dB across all processes. Power adjustment will span nominally from –35 dBm to +8 dBm in 21 steps @ 2 dBm / step.
3. Measured with output power set to nominal (0 dBm) and temperature @ 25°C. Trap filter is needed.

Table 16. RF port impedance

Characteristic	Symbol	Typ	Unit
RFIN Pins for internal T/R switch configuration, TX mode	Zin	—	Ohm
2.360 GHz		14.7–j215	
2.420 GHz		13.7–j18.7	
2.480 GHz		13–j16.3	
RFIN Pins for internal or external T/R switch configuration, RX mode	Zin	—	Ohm
2.360 GHz		14–j9.5	
2.420 GHz		13–j7.6	
2.480 GHz		12.3–j5.6	

10.3 SPI timing: R_SSEL_B to R_SCLK

The following diagram describes timing constraints that must be guaranteed by the system designer.

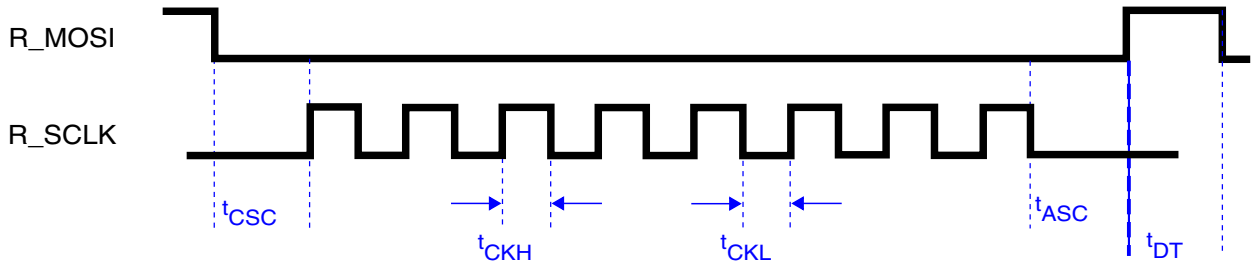


Figure 9. SPI timing: R_SSEL_B to R_SCLK

t_{CSC} (CS-to-SCK delay): 31.25 ns

t_{ASC} (After SCK delay): 31.25 ns

t_{DT} (Minimum CS idle time): 62.5 ns

t_{CKH} (Minimum R_SCLK high time): 31.25 ns (for SPI writes); 55.55 ns (for SPI reads)

t_{CKL} (Minimum R_SCLK low time): 31.25 ns (for SPI writes); 55.55 ns (for SPI reads)

Note

The SPI master device deasserts R_SSEL_B only on byte boundaries, and only after guaranteeing the t_{ASC} constraint shown above.

10.4 SPI timing: R_SCLK to R_MOSI and R_MISO

The following diagram describes timing constraints that must be guaranteed by the system designer. These constraints apply to the Master SPI (R_MOSI), and are guaranteed by the radio SPI (R_MISO).

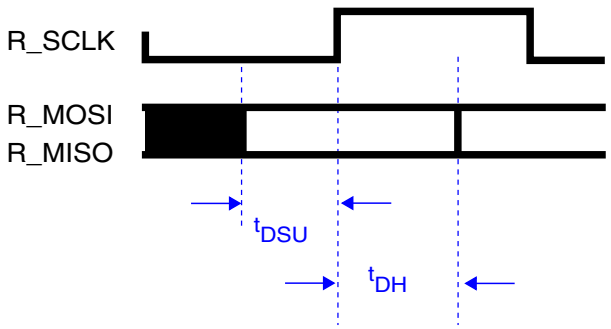


Figure 10. SPI timing: R_SCLK to R_MOSI and R_MISO

t_{DSU} (data-to-SCK setup): 10 ns

t_{DH} (SCK-to-data hold): 10 ns

11 Crystal oscillator reference frequency

This section provides application specific information regarding crystal oscillator reference design and recommended crystal usage.

11.1 Crystal oscillator design considerations

The IEEE 802.15.4 standard requires that frequency tolerance remain within ±40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will result in acceptable performance. The MCR20A transceiver provides on board crystal trim capacitors to assist in meeting this performance, while the bulk of the crystal load capacitance is external.

11.2 Crystal requirements

The suggested crystal specification for the MCR20A transceiver is shown in Table 17. A number of the stated parameters are related to the desired package, the desired temperature range and the use of crystal capacitive load trimming.

Table 17. MCR20A transceiver's crystal specifications

Parameter	Value	Unit	Condition
Frequency	32	MHz	
Frequency tolerance (cut tolerance)	±10	ppm	at 25°C

Table continues on the next page...

Table 17. MCR20A transceiver's crystal specifications (continued)

Parameter	Value	Unit	Condition
Frequency stability (temperature)	±25	ppm	Over desired temperature range
Aging[1]	±2	ppm	max
Equivalent series resistance	60	Ω	max
Load capacitance	5–9	pF	
Shunt capacitance	<2	pF	max
Mode of oscillation	—	—	fundamental

1. A wider aging tolerance may be acceptable when the application uses trimming at production final test.

12 Pin Diagrams and Pin Assignments

12.1 Pin assignments

This figure shows the MCR20A transceiver's package pin assignment.

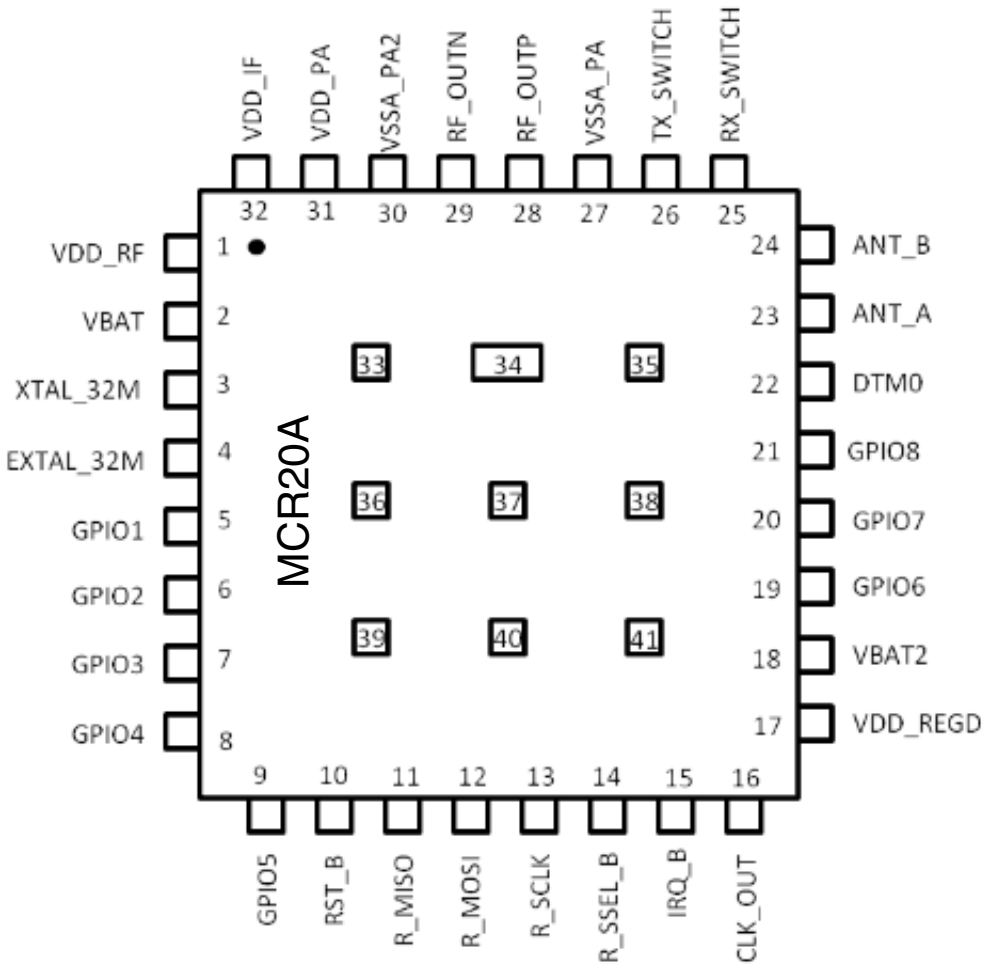


Figure 11. Pin assignment

12.2 Pin function table

Table 18. Pin function

Pin number	Pin name	Type	Function	Description
1	VDD_RF	Analog Power Output	Analog Voltage	Analog 1.8 Vdc
2	VBAT	Power Input	Battery Voltage	Connect to system VDD supply
3	XTAL_32M	Analog Output	RF	32 MHz reference oscillator output
4	EXTAL_32M	Analog Input	RF	32 MHz references oscillator input
5	GPIO1	Digital Input/Output	General-Purpose IO	GPIO
6	GPIO2	Digital Input/Output	General-Purpose IO	GPIO

Table continues on the next page...

Table 18. Pin function (continued)

Pin number	Pin name	Type	Function	Description
7	GPIO3	Digital Input/Output	General-Purpose IO	GPIO
8	GPIO4	Digital Input/Output	General-Purpose IO	GPIO
9	GPIO5	Digital Input/Output	General-Purpose IO	GPIO or CLK_OUT default state select
10	RST_B	Digital Input/Output	Digital	Device asynchronous hardware reset. Active low.
11	R_MISO	Digital Input/Output	Digital	SPI MISO
12	R_MOSI	Digital Input/Output	Digital	SPI MOSI
13	R_SCLK	Digital Input/Output	Digital	SPI clock
14	R_SSEL_B	Digital Input/Output	Digital	SPI slave select
15	IRQ_B	Digital Input/Output	Digital	Interrupt command signal
16	CLK_OUT	Digital Output	RF	Programmable clock source
17	VDD_REGD	Digital Power Ref	Digital Voltage	Digital 1.8 Vdc ref. Decouple to ground.
18	VBAT2	Power Input	Battery Voltage	Connect to system VDD supply.
19	GPIO6	Digital Input/Output	General-Purpose IO	GPIO
20	GPIO7	Digital Input/Output	General-Purpose IO	GPIO
21	GPIO8	Digital Input/Output	General-Purpose IO	GPIO
22	DTM0	—	Factory Test	Do not connect.
23	ANT_A	Digital Input/Output	Antenna Diversity	Programmable sink and source current output with selectable high impedance state.
24	ANT_B	Digital Input/Output	Antenna Diversity	Programmable sink and source current output with selectable high impedance state.
25	RX_SWITCH	Digital Input/Output	Control Switch	Programmable sink and source current output with selectable high impedance state.
26	TX_SWITCH	Digital Input/Output	Control Switch	Programmable sink and source current output with selectable high impedance state.
27	VSSA_PA	—	Gnd	RF ground
28	RF_OUTP	RFInput/Output	RF	Bidirectional RF input/output positive
29	RF_OUTN	RFInput/Output	RF	Bidirectional RF input/output negative
30	VSSA_PA2	—	Gnd	RFground
31	VDD_PA	Analog Power Input	Analog Voltage	Analog 1.8 Vdc input
32	VDD_IF	Analog Power Input	Analog Voltage	Analog 1.8 Vdc input
33	GND_RF	—	—	Connect to RF ground
34	GND_PA	—	—	Connect to RF ground

Table continues on the next page...

Table 18. Pin function (continued)

Pin number	Pin name	Type	Function	Description
35	GND_RF	—	—	Connect to RF ground
36	—	Factory test	Reserved	Do not connect
37	—	Factory test	Reserved	Do not connect
38	—	Factory test	Reserved	Do not connect
39	—	Factory test	Reserved	Do not connect
40	—	Factory test	Reserved	Do not connect
41	—	Factory test	Reserved	Do not connect

13 Dimensions

13.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
MLGA-32	98ASA00424D

14 Revision History

The following table provides a revision history for this document.

Table 19. Revision History

Rev. No.	Date	Substantial Changes
3.2	07/2016	Added section 5.1 "Transceiver Transmit Current Distribution".

How to Reach Us:

Home Page:
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Web Support:
nxp.com/support

Document Number MCR20AVHM
Revision 3.2, 07/2016