

74LVC8T595

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Rev. 1 — 9 May 2017

Product data sheet

1 General description

The 74LVC8T595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. Data is shifted on the positive-going transitions of the SHCP input. The data in the shift register is transferred to the storage register on a positive-going transition of the STCP input. If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

$V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 1.1 V and 5.5 V making the device suitable for translating between any of the voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins \overline{MR} , SHCP, STCP, \overline{OE} , DS and Q7S are referenced to $V_{CC(A)}$ and pins Qn are referenced to $V_{CC(B)}$.

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when $V_{CC(A)}$ is at GND level, the Qn outputs are in the high-impedance OFF-state.

2 Features and benefits

- Wide supply voltage range:
 - $V_{CC(A)}$: 1.1 V to 5.5 V
 - $V_{CC(B)}$: 1.1 V to 5.5 V
- High noise immunity
- Complies with JEDEC standards:
 - JESD8-12A (1.1 V to 1.3 V)
 - JESD8-11A (1.4 V to 1.6 V)
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (3.0 V to 3.6 V)
 - JESD12-6 (4.5 V to 5.5 V)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 4000V
 - CDM JESD22-C101E exceeds 1000 V
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- ± 24 mA output drive ($V_{CC(A)} = V_{CC(B)} = 3.0$ V)
- Inputs accept voltages up to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC8T595PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC8T595BQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm	SOT764-1

4 Functional diagram

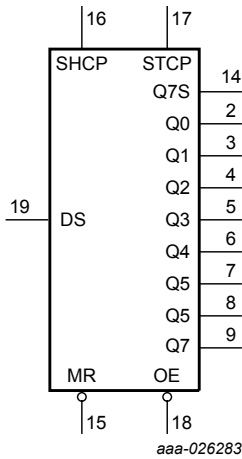


Figure 1. Logic symbol

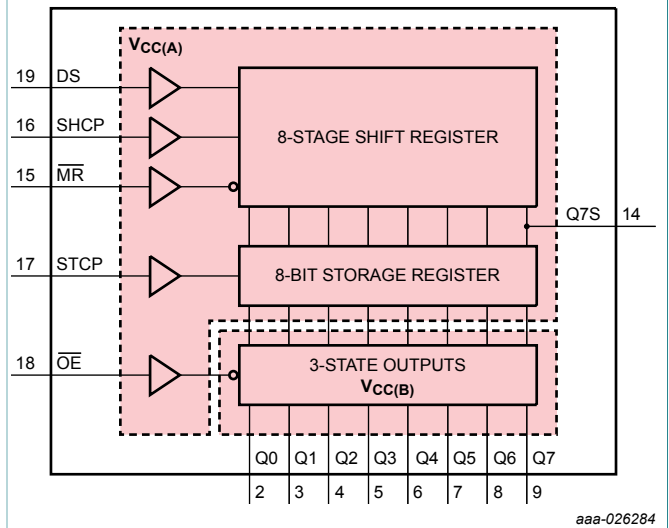
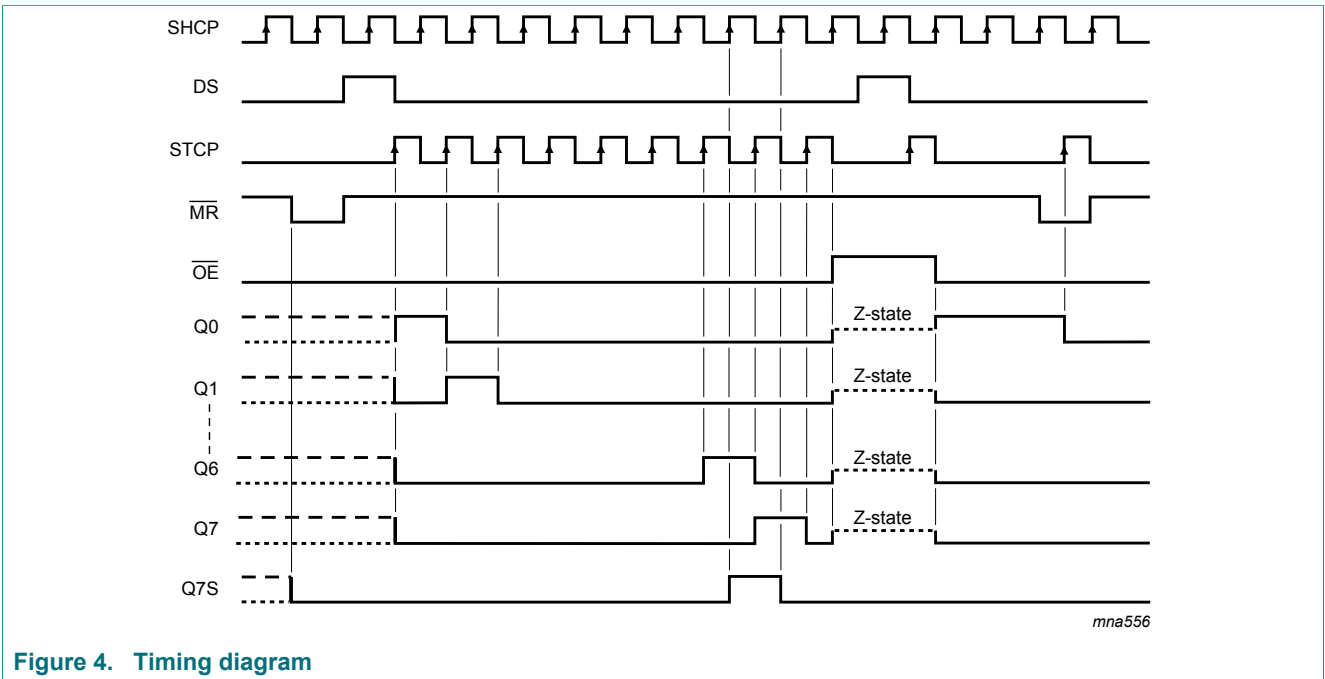
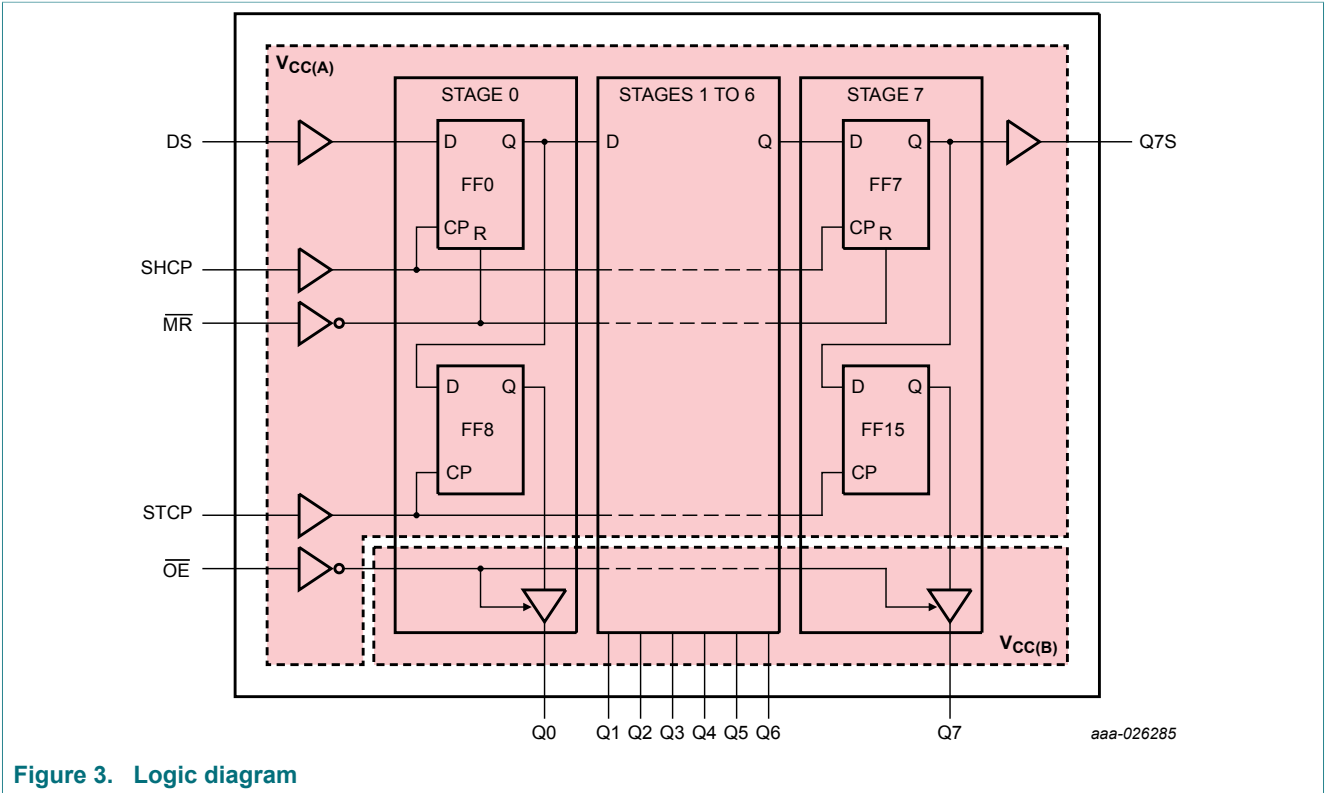
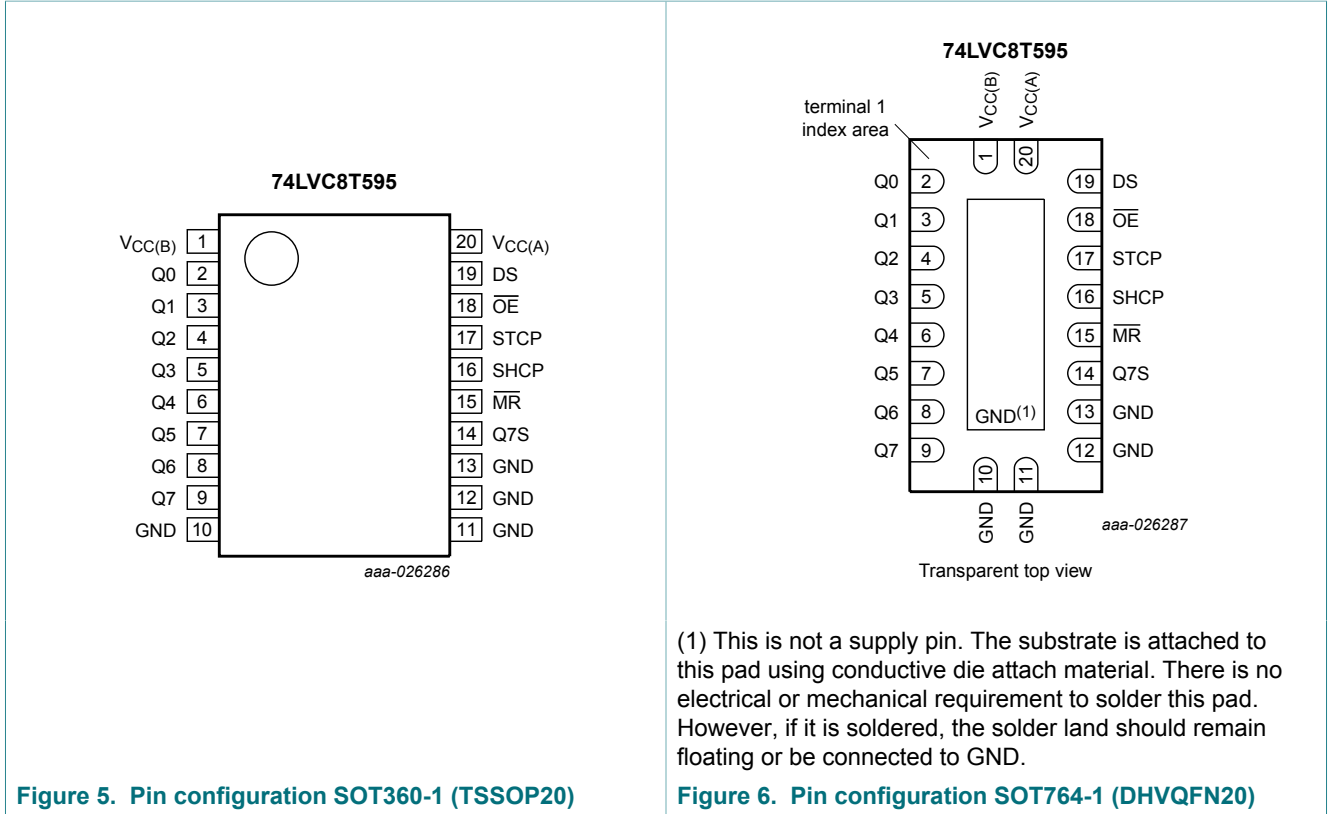


Figure 2. Functional diagram



5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V _{CC(B)}	1	supply voltage B (Q _n outputs)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 3, 4, 5, 6, 7, 8, 9	data output
GND	10, 11, 12, 13	ground (0 V)
Q7S	14	serial data output
$\overline{\text{MR}}$	15	master reset input (active LOW)
SHCP	16	shift register clock input
STCP	17	storage register clock input
$\overline{\text{OE}}$	18	output enable input (active LOW)
DS	19	serial data input
V _{CC(A)}	20	supply voltage A ($\overline{\text{MR}}$, SHCP, STCP, $\overline{\text{OE}}$, DS inputs and Q7S output)

6 Functional description

Table 3. Function table ^[1]

Supply voltage $V_{CC(A)}, V_{CC(B)}$	Input				Output			Function
	SHCP	STCP	OE	MR	DS	Q7S	Qn	
1.2 V to 5.5 V	X	X	L	L	X	L	NC	a LOW-state on \overline{MR} only affects the shift register
1.2 V to 5.5 V	X	↑	L	L	X	L	L	empty shift register loaded into storage register
1.2 V to 5.5 V	X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
1.2 V to 5.5 V	↑	X	L	H	H	Q6S	NC	logic HIGH-state shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
1.2 V to 5.5 V	X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
1.2 V to 5.5 V	↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages
GND ^[2]	X	X	X	X	X	X	Z	suspend mode

- [1] H = HIGH voltage state;
 L = LOW voltage state;
 ↑ = LOW-to-HIGH transition;
 X = don't care;
 NC = no change;
 Z = high-impedance OFF-state.

- [2] When $V_{CC(A)}$ is at GND level, the device goes into suspend mode.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode [1] [2] [3]	-0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode [1]	-0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CCO} [2]	-	± 50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

[3] $V_{CCO} + 0.5$ V should not exceed 6.5 V

[4] For TSSOP20 package: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN20 package: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.1	5.5	V
$V_{CC(B)}$	supply voltage B		1.1	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode [1]	0	V_{CCO}	V
		Suspend or 3-state mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)} = 1.1$ V to 1.3 V	-	20	ns/V
		$V_{CC(A)} = 1.4$ V to 1.95 V	-	20	ns/V
		$V_{CC(A)} = 2.3$ V to 2.7 V	-	20	ns/V
		$V_{CC(A)} = 3$ V to 3.6 V	-	10	ns/V
		$V_{CC(A)} = 4.5$ V to 5.5 V	-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output.

9 Static characteristics

Table 6. Typical static characteristics at $T_{amb} = 25\text{ °C}$

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = -3\text{ mA}$; $V_{CCO} = 1.2\text{ V}$	[1]	-	1.09	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 3\text{ mA}$; $V_{CCO} = 1.2\text{ V}$	[1]	-	0.07	-	V
I_I	input leakage current	\overline{MR} , SHCP, STCP, \overline{OE} and DS inputs; $V_I = 0\text{ V}$ to 5.5 V ; $V_{CC(A)} = 1.1\text{ V}$ to 5.5 V	-	-	± 1	μA	
I_{OZ}	OFF-state output current	Qn outputs; $V_O = 0\text{ V}$ or $V_{CC(B)}$					
		$V_{CC(B)} = 1.1\text{ V}$ to 5.5 V	-	-	± 1	μA	
		suspend mode; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 5.5\text{ V}$	-	-	± 1	μA	
I_{OFF}	power-off leakage current	inputs, Q7S output; V_I or $V_O = 0\text{ V}$ to 5.5 V ; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 1.1\text{ V}$ to 5.5 V	[1]	-	-	± 1	μA
		Qn outputs; V_I or $V_O = 0\text{ V}$ to 5.5 V ; $V_{CC(B)} = 0\text{ V}$; $V_{CC(A)} = 1.1\text{ V}$ to 5.5 V		-	-	± 1	μA
C_I	input capacitance	\overline{MR} , SHCP, STCP, \overline{OE} and DS inputs; $V_I = 0\text{ V}$ or 3.3 V ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	3	-	pF	

[1] V_{CCO} is the supply voltage associated with the output.

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC(A)} = 1.1 V to 1.3 V	0.65V _{CC(A)}	-	0.65V _{CC(A)}	-	V
		V _{CC(A)} = 1.4 V to 1.6 V	0.65V _{CC(A)}	-	0.65V _{CC(A)}	-	V
		V _{CC(A)} = 1.65 V to 1.95 V	0.65V _{CC(A)}	-	0.65V _{CC(A)}	-	V
		V _{CC(A)} = 2.3 V to 2.7 V	1.7	-	1.7	-	V
		V _{CC(A)} = 3.0 V to 3.6 V	2.0	-	2.0	-	V
		V _{CC(A)} = 4.5 V to 5.5 V	0.7V _{CC(A)}	-	0.7V _{CC(A)}	-	V
V _{IL}	LOW-level input voltage	V _{CC(A)} = 1.1 V to 1.3 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
		V _{CC(A)} = 1.4 V to 1.6 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
		V _{CC(A)} = 1.65 V to 1.95 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
		V _{CC(A)} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CC(A)} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		V _{CC(A)} = 4.5 V to 5.5 V	-	0.3V _{CC(A)}	-	0.3V _{CC(A)}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} [1]					
		I _O = -100 µA; V _{CCO} = 1.1 V to 4.5 V	V _{CCO} - 0.1	-	V _{CCO} - 0.1	-	V
		I _O = -2 mA; V _{CCO} = 1.1 V	0.825	-	0.825	-	V
		I _O = -6 mA; V _{CCO} = 1.4 V	1.0	-	1.0	-	V
		I _O = -8 mA; V _{CCO} = 1.65 V	1.2	-	1.2	-	V
		I _O = -12 mA; V _{CCO} = 2.3 V	1.9	-	1.9	-	V
		I _O = -24 mA; V _{CCO} = 3.0 V	2.4	-	2.4	-	V
		I _O = -24 mA; V _{CCO} = 4.5 V	3.85	-	3.85	-	V
		I _O = -32 mA; V _{CCO} = 4.5 V	3.8	-	3.8	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IL} [1]					
		I _O = 100 µA; V _{CCO} = 1.1 V to 4.5 V	-	0.1	-	0.1	V
		I _O = 2 mA; V _{CCO} = 1.1 V	-	0.275	-	0.275	V
		I _O = 6 mA; V _{CCO} = 1.4 V	-	0.3	-	0.3	V
		I _O = 8 mA; V _{CCO} = 1.65 V	-	0.45	-	0.45	V
		I _O = 12 mA; V _{CCO} = 2.3 V	-	0.3	-	0.3	V
		I _O = 24 mA; V _{CCO} = 3.0 V	-	0.55	-	0.55	V
		I _O = 24 mA; V _{CCO} = 4.5 V	-	0.50	-	0.50	V
I _O = 32 mA; V _{CCO} = 4.5 V	-	0.55	-	0.55	V		

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_I	input leakage current	$V_I = 0 \text{ V to } 5.5 \text{ V};$ $V_{CC(A)} = 1.1 \text{ V to } 5.5 \text{ V}$	-	± 2	-	± 10	μA
I_{OZ}	OFF-state output current	Qn outputs; $V_O = 0 \text{ V or } V_{CC(B)}$					
		$V_{CC(B)} = 1.1 \text{ V to } 5.5 \text{ V}$	-	± 2	-	± 10	μA
		suspend mode; $V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 5.5 \text{ V}$	-	± 2	-	± 10	μA
I_{OFF}	power-off leakage current	inputs, Q7S output; $V_I \text{ or } V_O = 0 \text{ V to } 5.5 \text{ V};$ $V_{CC(A)} = 0 \text{ V};$ $V_{CC(B)} = 1.1 \text{ V to } 5.5 \text{ V}$	-	± 2	-	± 10	μA
		Qn outputs; $V_I \text{ or } V_O = 0 \text{ V to } 5.5 \text{ V};$ $V_{CC(B)} = 0 \text{ V};$ $V_{CC(A)} = 1.1 \text{ V to } 5.5 \text{ V}$	-	± 2	-	± 10	μA
I_{CC}	supply current	$V_{CC(A)}$ domain; $V_I = 0 \text{ V or } V_{CC(A)}; I_O = 0 \text{ A}$					
		$V_{CC(A)}, V_{CC(B)} = 1.1 \text{ V to } 5.5 \text{ V}$	-	2	-	5	μA
		$V_{CC(A)} = 5.5 \text{ V}; V_{CC(B)} = 0 \text{ V}$	-	2	-	5	μA
		$V_{CC(A)} = 0 \text{ V}; V_{CC(B)} = 5.5 \text{ V}$	-1	-	-2	-	μA
		$V_{CC(B)}$ domain; $V_I = 0 \text{ V or } V_{CC(A)}; I_O = 0 \text{ A}$					
		$V_{CC(A)}, V_{CC(B)} = 1.1 \text{ V to } 5.5 \text{ V}$	-	9	-	24	μA
		$V_{CC(B)} = 5.5 \text{ V}; V_{CC(A)} = 0 \text{ V}$	-	9	-	24	μA
$V_{CC(B)} = 0 \text{ V}; V_{CC(A)} = 5.5 \text{ V}$	-1	-	-2	-	μA		
ΔI_{CC}	additional supply current	per input; $V_{CC(A)}, V_{CC(B)} = 3.0 \text{ V to } 5.5 \text{ V}$					
		MR, SHCP, STCP, \overline{OE} inputs; one input at $V_{CC(A)} - 0.6 \text{ V};$ DS input at $V_{CC(A)}$ or GND; Qn = open	-	50	-	75	μA
		DS input at $V_{CC(A)} - 0.6 \text{ V};$ Qn = open	-	50	-	75	μA

[1] V_{CC0} is the supply voltage associated with the output.

10 Dynamic characteristics

Table 8. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ °C}$ [1] [2]

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$						Unit
			1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	
C_{PD}	power dissipation capacitance	inputs	31	31	32	33	36	43	pF
		outputs	105	104	103	101	99	98	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i = 10\text{ MHz}$; $V_i = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\ \Omega$.

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#); for waveforms see [Figure 7](#) up to [Figure 12](#).

Symbol	Parameter	Conditions	$V_{CC(A)}$									Unit
			1.2 V \pm 0.1 V			1.5 V \pm 0.1 V			1.8 V \pm 0.15 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$T_{amb} = +25\text{ °C}$; $V_{CC(B)} = 1.1\text{ V to } 5.5\text{ V}$												
t_{pd}	propagation delay	SHCP to Q7S [1]	5.8	21.3	38.9	4.5	14.2	20.9	3.7	10.9	16.7	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{\text{MR}}$ to Q7S	5.9	22.7	42.1	4.5	14.8	18.9	3.7	11.2	14.7	ns
t_W	pulse width	SHCP, STCP HIGH or LOW	6.9	1.9	-	3.5	1.4	-	2.6	1.1	-	ns
		$\overline{\text{MR}}$ LOW	12.4	3.5	-	5.6	2.1	-	3.9	1.5	-	ns
t_{su}	set-up time	DS to SHCP	3.0	1.1	-	2.6	0.5	-	2.3	0.3	-	ns
		$\overline{\text{MR}}$ to STCP	15.5	7.2	-	7.9	4.0	-	5.5	2.8	-	ns
		SHCP to STCP	13.5	5.4	-	6.5	3.0	-	4.9	2.1	-	ns
t_h	hold time	DS to SHCP	3.0	± 0.4	-	2.0	± 0.2	-	1.5	± 0.1	-	ns
t_{rec}	recovery time	$\overline{\text{MR}}$ to SHCP	2.0	-0.4	-	1.5	-0.2	-	1.3	-0.2	-	ns
f_{max}	maximum frequency	SHCP	45	73	-	75	99	-	90	120	-	MHz

[1] t_{pd} is the same as t_{PHL} , t_{PLH} .

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Table 10. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13; for waveforms see Figure 7 up to Figure 12.

Symbol	Parameter	Conditions	$V_{CC(A)}$									Unit
			2.5 V ± 0.2 V			3.3 V ± 0.3 V			5.0 V ± 0.5 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$T_{amb} = +25\text{ °C}; V_{CC(B)} = 1.1\text{ V to }5.5\text{ V}$												
t_{pd}	propagation delay	SHCP to Q7S ^[1]	2.7	7.3	11.5	2.3	5.6	9.1	1.9	4.1	6.6	ns
t_{PHL}	HIGH to LOW propagation delay	\overline{MR} to Q7S	2.9	7.4	10.0	2.4	5.7	7.9	2.1	4.4	6.1	ns
t_W	pulse width	SHCP, STCP HIGH or LOW	1.6	0.7	-	1.4	0.6	-	1.0	0.5	-	ns
		\overline{MR} LOW	2.5	1.0	-	1.6	0.8	-	1.4	0.6	-	ns
t_{su}	set-up time	DS to SHCP	1.9	0.2	-	1.5	0.1	-	1.1	0.1	-	ns
		\overline{MR} to STCP	3.2	1.7	-	2.4	1.3	-	2.2	1.1	-	ns
		SHCP to STCP	2.8	1.2	-	1.9	0.9	-	1.4	0.6	-	ns
t_h	hold time	DS to SHCP	1.5	±0.1	-	1.0	±0.1	-	1.0	±0.1	-	ns
t_{rec}	recovery time	\overline{MR} to SHCP	1.0	-0.1	-	1.0	-0.1	-	1.0	-0.1	-	ns
f_{max}	maximum frequency	SHCP	135	160	-	175	194	-	195	250	-	MHz

[1] t_{pd} is the same as t_{PHL} , t_{PLH} .

Table 11. Dynamic characteristics for temperature +25 °C ^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13; for waveforms see Figure 7 up to Figure 12.

Symbol	Parameter	Conditions	$V_{CC(B)}$									Unit
			1.2 V ± 0.1 V			1.5 V ± 0.1 V			1.8 V ± 0.15 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{CC(A)} = 1.2\text{ V} \pm 0.1\text{ V}$												
t_{pd}	propagation delay	STCP to Qn	6.2	23.7	46.4	5.3	19.1	35.4	4.8	16.9	31.6	ns
t_{dis}	disable time	\overline{OE} to Qn	3.6	12.7	25.1	3.0	9.7	15.6	3.1	9.0	14.4	ns
t_{en}	enable time	\overline{OE} to Qn	5.8	20.9	40.0	4.6	15.1	26.2	3.9	12.6	21.7	ns
f_{max}	maximum frequency	STCP	35	69	-	45	88	-	45	110	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	-	3.0	-	-	2.3	-	-	1.9	ns

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Symbol	Parameter	Conditions	$V_{CC(B)}$									Unit
			1.2 V ± 0.1 V			1.5 V ± 0.1 V			1.8 V ± 0.15 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{CC(A)} = 1.5 \text{ V} \pm 0.1 \text{ V}$												
t_{pd}	propagation delay	STCP to Qn	5.7	20.2	32.1	4.9	15.5	23.3	4.3	13.3	20.0	ns
t_{dis}	disable time	\overline{OE} to Qn	3.4	11.4	20.1	2.8	8.3	13.2	2.8	7.6	11.7	ns
t_{en}	enable time	\overline{OE} to Qn	5.5	19.9	38.7	4.2	13.9	24.1	3.6	11.3	19.3	ns
f_{max}	maximum frequency	STCP	45	73	-	70	95	-	90	120	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	-	2.7	-	-	2.0	-	-	1.7	ns
$V_{CC(A)} = 1.8 \text{ V} \pm 0.15 \text{ V}$												
t_{pd}	propagation delay	STCP to Qn	5.4	18.7	30.3	4.5	14.0	21.4	4	11.8	18.3	ns
t_{dis}	disable time	\overline{OE} to Qn	3.2	10.8	19.4	2.6	7.8	12.6	2.6	7.0	11.0	ns
t_{en}	enable time	\overline{OE} to Qn	5.4	19.4	38.1	4.1	13.4	23.7	3.5	10.7	18.7	ns
f_{max}	maximum frequency	STCP	45	75	-	70	98	-	90	125	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	-	2.7	-	-	2.0	-	-	1.6	ns
$V_{CC(A)} = 2.5 \text{ V} \pm 0.2 \text{ V}$												
t_{pd}	propagation delay	STCP to Qn	5.1	17.3	28.3	4.2	12.6	19.5	3.6	10.4	16.3	ns
t_{dis}	disable time	\overline{OE} to Qn	3.0	10.3	18.8	2.4	7.2	11.9	2.4	6.4	10.3	ns
t_{en}	enable time	\overline{OE} to Qn	5.3	18.9	37.7	4.1	13.0	23.3	3.4	10.2	18.1	ns
f_{max}	maximum frequency	STCP	45	76	-	70	100	-	90	128	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	-	2.6	-	-	2.0	-	-	1.6	ns
$V_{CC(A)} = 3.3 \text{ V} \pm 0.3 \text{ V}$												
t_{pd}	propagation delay	STCP to Qn	4.9	16.7	27.6	4.0	12.0	18.7	3.4	9.8	15.4	ns
t_{dis}	disable time	\overline{OE} to Qn	3.0	10.0	18.4	2.3	6.9	11.4	2.3	6.1	10.0	ns
t_{en}	enable time	\overline{OE} to Qn	5.3	18.8	37.6	4.1	12.9	23.0	3.4	10.1	18.0	ns
f_{max}	maximum frequency	STCP	45	76	-	70	101	-	90	130	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	-	2.6	-	-	2.0	-	-	1.6	ns
$V_{CC(A)} = 5.0 \text{ V} \pm 0.5 \text{ V}$												
t_{pd}	propagation delay	STCP to Qn	4.8	16.1	27.5	3.9	11.4	18.0	3.3	9.2	14.8	ns
t_{dis}	disable time	\overline{OE} to Qn	2.8	9.6	19.4	2.2	6.6	11.3	2.3	5.9	9.6	ns
t_{en}	enable time	\overline{OE} to Qn	5.4	18.7	38.3	4.1	12.8	23.1	3.4	10.1	18.3	ns
f_{max}	maximum frequency	STCP	45	77	-	70	102	-	90	132	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	-	2.7	-	-	2.0	-	-	1.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Table 12. Dynamic characteristics for temperature +25 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13; for waveforms see Figure 7 up to Figure 12.

Symbol	Parameter	Conditions	V _{CC(B)}									Unit
			2.5 V ± 0.2 V			3.3 V ± 0.3 V			5.0 V ± 0.5 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{CC(A)} = 1.2 V ± 0.1 V												
t _{pd}	propagation delay	STCP to Qn	4.2	14.5	27.9	3.8	13.4	26.3	3.5	12.4	24.9	ns
t _{dis}	disable time	\overline{OE} to Qn	2.6	7.4	12.0	2.9	7.7	12.4	2.4	6.6	11.3	ns
t _{en}	enable time	\overline{OE} to Qn	3.3	10.1	16.8	2.9	9.2	15.8	2.7	8.9	15.9	ns
f _{max}	maximum frequency	STCP	45	131	-	45	139	-	45	144	-	MHz
t _{sk(o)}	output skew time	Q0 to Q7 [2]	-	-	1.4	-	-	1.2	-	-	1.0	ns
V _{CC(A)} = 1.5 V ± 0.1 V												
t _{pd}	propagation delay	STCP to Qn	3.7	10.9	16.2	3.3	9.7	14.5	3.0	8.7	13.0	ns
t _{dis}	disable time	\overline{OE} to Qn	2.2	6.0	9.2	2.6	6.2	9.4	2.1	5.0	8.1	ns
t _{en}	enable time	\overline{OE} to Qn	2.9	8.6	14.1	2.6	7.5	12.1	2.4	6.7	10.6	ns
f _{max}	maximum frequency	STCP	130	144	-	130	187	-	130	224	-	MHz
t _{sk(o)}	output skew time	Q0 to Q7 [2]	-	-	1.2	-	-	1.0	-	-	0.7	ns
V _{CC(A)} = 1.8 V ± 0.15 V												
t _{pd}	propagation delay	STCP to Qn	3.4	9.4	14.4	3.0	8.2	12.6	2.7	7.2	10.9	ns
t _{dis}	disable time	\overline{OE} to Qn	2.0	5.3	8.3	2.4	5.5	8.5	1.9	4.3	7.2	ns
t _{en}	enable time	\overline{OE} to Qn	2.7	8.0	13.3	2.4	6.7	11.1	2.2	5.8	9.4	ns
f _{max}	maximum frequency	STCP	130	151	-	165	197	-	205	237	-	MHz
t _{sk(o)}	output skew time	Q0 to Q7 [2]	-	-	1.2	-	-	0.9	-	-	0.7	ns
V _{CC(A)} = 2.5 V ± 0.2 V												
t _{pd}	propagation delay	STCP to Qn	3.0	7.9	12.4	2.6	6.7	10.5	2.3	5.7	8.8	ns
t _{dis}	disable time	\overline{OE} to Qn	1.9	4.6	7.5	2.2	4.8	7.5	1.7	3.5	6.0	ns
t _{en}	enable time	\overline{OE} to Qn	2.7	7.4	12.6	2.3	6.0	10.2	2.0	4.9	8.2	ns
f _{max}	maximum frequency	STCP	130	156	-	165	210	-	215	252	-	MHz
t _{sk(o)}	output skew time	Q0 to Q7 [2]	-	-	1.2	-	-	0.9	-	-	0.7	ns
V _{CC(A)} = 3.3 V ± 0.3 V												
t _{pd}	propagation delay	STCP to Qn	2.8	7.3	11.5	2.4	6.1	9.6	2.1	5.0	7.9	ns
t _{dis}	disable time	\overline{OE} to Qn	1.8	4.4	7.1	2.1	4.5	7.1	1.6	3.2	5.5	ns
t _{en}	enable time	\overline{OE} to Qn	2.6	7.2	12.3	2.3	5.8	10.0	2.0	4.6	7.8	ns
f _{max}	maximum frequency	STCP	130	159	-	165	213	-	215	255	-	MHz
t _{sk(o)}	output skew time	Q0 to Q7 [2]	-	-	1.2	-	-	0.9	-	-	0.7	ns

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Symbol	Parameter	Conditions	$V_{CC(B)}$									Unit
			2.5 V \pm 0.2 V			3.3 V \pm 0.3 V			5.0 V \pm 0.5 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{CC(A)} = 5.0 \text{ V} \pm 0.5 \text{ V}$												
t_{pd}	propagation delay	STCP to Qn	2.7	6.8	10.9	2.3	5.5	8.9	1.8	4.4	7.2	ns
t_{dis}	disable time	\overline{OE} to Qn	1.7	4.1	6.8	2.0	4.3	6.7	1.4	2.9	5.1	ns
t_{en}	enable time	\overline{OE} to Qn	2.7	7.2	12.4	2.3	5.8	10.0	2.0	4.6	7.7	ns
f_{max}	maximum frequency	STCP	130	159	-	165	213	-	215	254	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	-	1.1	-	-	0.9	-	-	0.7	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Table 13. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#); for waveforms see [Figure 7](#) up to [Figure 12](#).

Symbol	Parameter	Conditions	$V_{CC(A)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$T_{amb} = -40\text{ °C to }+85\text{ °C}; V_{CC(B)} = 1.1\text{ V to }5.5\text{ V}$															
t_{pd}	propagation delay	SHCP to Q7S ^[1]	3.4	42.1	2.7	22.1	2.1	17.7	1.5	12.4	1.3	9.8	1.0	7.2	ns
t_{PHL}	HIGH to LOW propagation delay	\overline{MR} to Q7S	3.6	43.6	2.7	20.2	2.2	16.0	1.7	11.0	1.4	8.7	1.3	6.6	ns
t_w	pulse width	SHCP, STCP HIGH or LOW	7.8	-	4.8	-	3.3	-	2.0	-	1.7	-	1.3	-	ns
		\overline{MR} LOW	12.8	-	6.2	-	4.4	-	2.8	-	2.3	-	1.4	-	ns
t_{su}	set-up time	DS to SHCP	4.5	-	3.0	-	2.6	-	2.3	-	1.9	-	1.5	-	ns
		\overline{MR} to STCP	16.5	-	9.1	-	6.1	-	3.6	-	2.9	-	2.3	-	ns
		SHCP to STCP	13.5	-	7.7	-	5.4	-	3.2	-	2.3	-	1.8	-	ns
t_h	hold time	DS to SHCP	3.0	-	2.0	-	1.5	-	1.5	-	1.0	-	1.0	-	ns
t_{rec}	recovery time	\overline{MR} to SHCP	2.2	-	1.7	-	1.5	-	1.2	-	1.2	-	1.2	-	ns
f_{max}	maximum frequency	SHCP	40	-	70	-	90	-	130	-	160	-	175	-	MHz

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Symbol	Parameter	Conditions	$V_{CC(A)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$T_{amb} = -40\text{ °C to }+125\text{ °C}; V_{CC(B)} = 1.1\text{ V to }5.5\text{ V}$															
t_{pd}	propagation delay	SHCP to Q7S ^[1]	3.4	42.1	2.7	22.7	2.1	18.3	1.5	12.9	1.3	10.3	1.0	7.6	ns
t_{PHL}	HIGH to LOW propagation delay	\overline{MR} to Q7S	3.6	44.3	2.7	21.0	2.2	16.7	1.7	11.5	1.4	9.1	1.3	7.0	ns
t_W	pulse width	SHCP, STCP HIGH or LOW	8.4	-	5.3	-	3.8	-	2.5	-	1.9	-	1.4	-	ns
		\overline{MR} LOW	13.3	-	6.9	-	5.2	-	3.1	-	2.4	-	1.6	-	ns
t_{su}	set-up time	DS to SHCP	4.5	-	3.0	-	2.6	-	2.3	-	1.9	-	1.5	-	ns
		\overline{MR} to STCP	16.5	-	9.5	-	6.8	-	4.2	-	3.1	-	2.4	-	ns
		SHCP to STCP	14.2	-	8.0	-	6.2	-	3.6	-	2.3	-	1.8	-	ns
t_h	hold time	DS to SHCP	3.5	-	2.5	-	2.0	-	2.0	-	1.5	-	1.2	-	ns
t_{rec}	recovery time	\overline{MR} to SHCP	2.4	-	1.9	-	1.7	-	1.4	-	1.4	-	1.4	-	ns
f_{max}	maximum frequency	SHCP	40	-	70	-	85	-	120	-	150	-	170	-	MHz

[1] t_{pd} is the same as t_{PHL} , t_{PLH} .

Table 14. Dynamic characteristics for temperature range -40 °C to +85 °C ^[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#); for waveforms see [Figure 7](#) up to [Figure 12](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 1.2 V \pm 0.1 V$															
t_{pd}	propagation delay	STCP to Qn	3.8	48.3	3.2	36.7	2.8	33.0	2.4	29.2	2.2	27.7	2.0	26.0	ns
t_{dis}	disable time	\overline{OE} to Qn	2.1	26.6	1.8	17.2	1.8	15.8	1.5	13.1	1.8	13.4	1.4	12.3	ns
t_{en}	enable time	\overline{OE} to Qn	3.5	42.1	2.7	27.0	2.2	22.6	1.9	18.0	1.7	17.0	1.6	17.2	ns
f_{max}	maximum frequency	STCP	30	-	40	-	40	-	40	-	40	-	40	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.5	-	2.5	-	2.0	-	1.5	-	1.2	-	1.0	ns
$V_{CC(A)} = 1.5 V \pm 0.1 V$															
t_{pd}	propagation delay	STCP to Qn	3.5	34.2	2.9	25.6	2.5	22.4	2.1	18.5	1.9	16.8	1.7	15.1	ns
t_{dis}	disable time	\overline{OE} to Qn	2.0	21.6	1.7	14.8	1.7	13.1	1.3	10.3	1.6	10.4	1.3	9.0	ns
t_{en}	enable time	\overline{OE} to Qn	3.3	38.9	2.6	25.0	2.1	20.3	1.7	15.1	1.5	13.2	1.4	11.7	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	105	-	105	-	105	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.1	-	2.2	-	1.8	-	1.3	-	1.0	-	0.8	ns
$V_{CC(A)} = 1.8 V \pm 0.15 V$															
t_{pd}	propagation delay	STCP to Qn	3.3	31.8	2.7	23.4	2.3	20.4	1.9	16.4	1.7	14.5	1.5	12.8	ns
t_{dis}	disable time	\overline{OE} to Qn	1.9	20.9	1.5	14.2	1.6	12.4	1.2	9.4	1.4	9.4	1.1	8.0	ns
t_{en}	enable time	\overline{OE} to Qn	3.3	38.6	2.4	24.5	2.0	19.7	1.6	14.4	1.4	12.1	1.3	10.5	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	120	-	145	-	155	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.1	-	2.2	-	1.8	-	1.2	-	1.0	-	0.8	ns

Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Symbol	Parameter	Conditions	$V_{CC(B)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 2.5 V \pm 0.2 V$															
t_{pd}	propagation delay	STCP to Qn	3.1	29.6	2.5	21.2	2.1	18.1	1.7	14.0	1.5	12.1	1.3	10.2	ns
t_{dis}	disable time	\overline{OE} to Qn	1.8	20.2	1.4	13.2	1.4	11.6	1.1	8.5	1.3	8.3	1.0	6.6	ns
t_{en}	enable time	\overline{OE} to Qn	3.2	37.7	2.4	24.0	2.0	19.1	1.5	13.5	1.3	11.1	1.2	9.0	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	120	-	145	-	180	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.1	-	2.2	-	1.8	-	1.2	-	1.0	-	0.7	ns
$V_{CC(A)} = 3.3 V \pm 0.3 V$															
t_{pd}	propagation delay	STCP to Qn	3.0	29.1	2.4	20.3	2.0	17.2	1.6	13.0	1.4	11.0	1.2	9.1	ns
t_{dis}	disable time	\overline{OE} to Qn	1.7	19.7	1.3	13.0	1.4	11.2	1.0	8.1	1.3	7.9	0.9	6.0	ns
t_{en}	enable time	\overline{OE} to Qn	3.2	38.1	2.4	23.7	2.0	19.0	1.5	13.3	1.3	10.7	1.2	8.5	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	120	-	145	-	190	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.0	-	2.2	-	1.8	-	1.2	-	1.0	-	0.7	ns
$V_{CC(A)} = 5.0 V \pm 0.5 V$															
t_{pd}	propagation delay	STCP to Qn	2.9	29.1	2.3	19.6	1.9	16.3	1.5	12.2	1.3	10.2	1.1	8.2	ns
t_{dis}	disable time	\overline{OE} to Qn	1.6	20.6	1.3	12.6	1.3	10.9	0.9	7.7	1.2	7.5	0.8	5.6	ns
t_{en}	enable time	\overline{OE} to Qn	3.3	38.9	2.5	23.8	2.0	19.1	1.6	13.3	1.4	10.6	1.2	8.3	ns
f_{max}	maximum frequency	STCP	40	-	65	-	80	-	120	-	145	-	190	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.0	-	2.2	-	1.7	-	1.2	-	0.9	-	0.7	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Table 15. Dynamic characteristics for temperature range -40 °C to +125 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13; for waveforms see Figure 7 up to Figure 12.

Symbol	Parameter	Conditions	$V_{CC(B)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 1.1 \text{ V to } 1.3 \text{ V}$															
t_{pd}	propagation delay	STCP to Qn	3.8	48.3	3.2	37.4	2.8	34.0	2.4	30.4	2.2	28.6	2.0	27.0	ns
t_{dis}	disable time	\overline{OE} to Qn	2.1	27.6	1.8	18.0	1.8	16.5	1.5	13.7	1.8	14.1	1.4	12.8	ns
t_{en}	enable time	\overline{OE} to Qn	3.5	42.1	2.7	27.6	2.2	23.2	1.9	18.6	1.7	17.8	1.6	18.0	ns
f_{max}	maximum frequency	STCP	30	-	40	-	40	-	40	-	40	-	40	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [2]	-	3.6	-	2.6	-	2.1	-	1.5	-	1.3	-	1.0	ns
$V_{CC(A)} = 1.4 \text{ V to } 1.6 \text{ V}$															
t_{pd}	propagation delay	STCP to Qn	3.5	34.4	2.9	26.3	2.5	23.3	2.1	19.6	1.9	17.7	1.7	16.1	ns
t_{dis}	disable time	\overline{OE} to Qn	2.0	22.7	1.7	15.7	1.7	14.0	1.3	11.0	1.6	11.0	1.3	9.5	ns
t_{en}	enable time	\overline{OE} to Qn	3.3	38.9	2.6	25.5	2.1	20.8	1.7	15.8	1.5	13.8	1.4	12.3	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	95	-	95	-	95	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [2]	-	3.1	-	2.2	-	1.8	-	1.3	-	1.0	-	0.8	ns
$V_{CC(A)} = 1.65 \text{ V to } 1.95 \text{ V}$															
t_{pd}	propagation delay	STCP to Qn	3.3	32.1	2.7	24.1	2.3	21.1	1.9	17.3	1.7	15.3	1.5	13.6	ns
t_{dis}	disable time	\overline{OE} to Qn	1.9	21.9	1.5	14.9	1.6	13.2	1.2	10.1	1.4	10.0	1.1	8.4	ns
t_{en}	enable time	\overline{OE} to Qn	3.3	38.6	2.4	24.8	2.0	20.3	1.6	14.9	1.4	12.7	1.3	11.0	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	105	-	140	-	140	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 [2]	-	3.1	-	2.2	-	1.8	-	1.2	-	1.0	-	0.8	ns

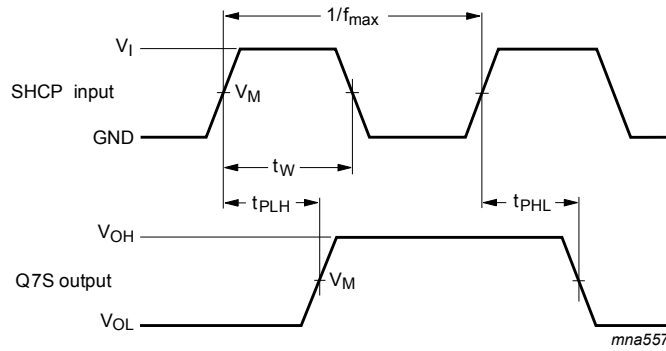
Dual supply 8-bit serial-in/serial-out or parallel-out shift register; 3-state

Symbol	Parameter	Conditions	$V_{CC(B)}$												Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)} = 2.3 \text{ V to } 2.7 \text{ V}$															
t_{pd}	propagation delay	STCP to Qn	3.1	29.7	2.5	21.8	2.1	18.8	1.7	14.7	1.5	12.7	1.3	10.8	ns
t_{dis}	disable time	\overline{OE} to Qn	1.8	21.2	1.4	14.2	1.4	12.4	1.1	9.1	1.3	8.8	1.0	7.0	ns
t_{en}	enable time	\overline{OE} to Qn	3.2	37.7	2.4	24.4	2.0	19.7	1.5	14.1	1.3	11.6	1.2	9.4	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	105	-	140	-	175	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.1	-	2.2	-	1.8	-	1.2	-	1.0	-	0.7	ns
$V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}$															
t_{pd}	propagation delay	STCP to Qn	3.0	29.1	2.4	20.8	2.0	17.7	1.6	13.5	1.4	11.6	1.2	9.6	ns
t_{dis}	disable time	\overline{OE} to Qn	1.7	20.9	1.3	13.8	1.4	12.1	1.0	8.7	1.3	8.3	0.9	6.4	ns
t_{en}	enable time	\overline{OE} to Qn	3.2	38.1	2.4	24.3	2.0	19.5	1.5	13.7	1.3	11.2	1.2	8.9	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	105	-	140	-	175	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.0	-	2.2	-	1.8	-	1.2	-	1.0	-	0.7	ns
$V_{CC(A)} = 4.5 \text{ V to } 5.5 \text{ V}$															
t_{pd}	propagation delay	STCP to Qn	2.9	29.1	2.3	20.0	1.9	16.7	1.5	12.7	1.3	10.6	1.1	9.0	ns
t_{dis}	disable time	\overline{OE} to Qn	1.6	21.7	1.3	13.6	1.3	11.7	0.9	8.3	1.2	7.9	0.8	6.0	ns
t_{en}	enable time	\overline{OE} to Qn	3.3	38.9	2.5	24.3	2.0	19.5	1.6	13.8	1.4	11.0	1.2	8.6	ns
f_{max}	maximum frequency	STCP	40	-	65	-	75	-	105	-	140	-	175	-	MHz
$t_{sk(o)}$	output skew time	Q0 to Q7 ^[2]	-	3.0	-	2.2	-	1.7	-	1.2	-	0.9	-	0.7	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

[2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

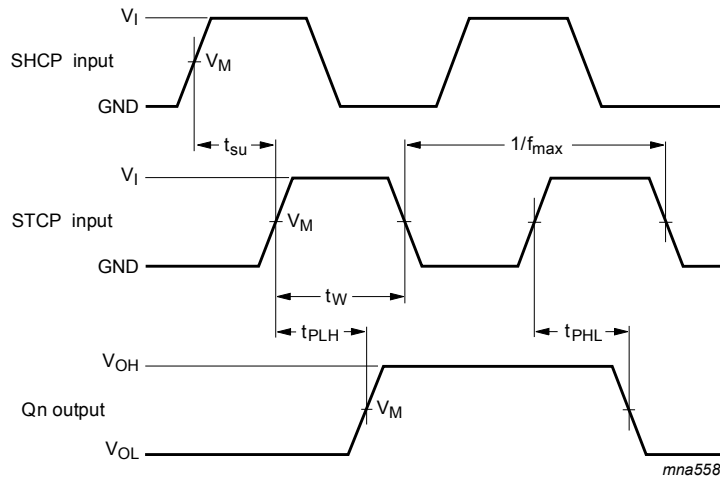
10.1 Waveforms and test circuit



Measurement points are given in [Table 16](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

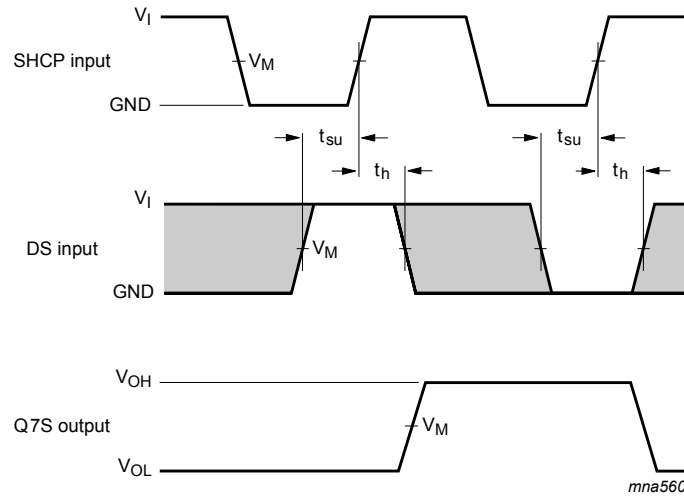
Figure 7. The shift clock (SHCP) to serial data output (Q7S) propagation delays, the shift clock pulse width and maximum shift clock frequency



Measurement points are given in [Table 16](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

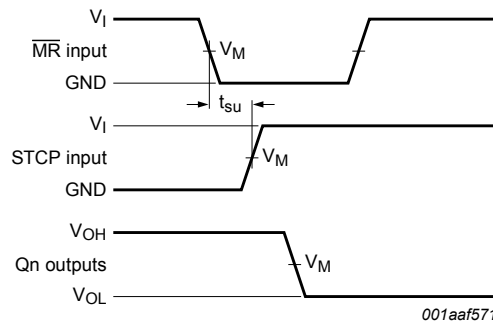
Figure 8. The storage clock (STCP) to parallel data output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time



Measurement points are given in [Table 16](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 9. The data set-up and hold times for the serial data input (DS)



Measurement points are given in [Table 16](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 10. The master reset (\overline{MR}) to storage clock (STCP) set-up time

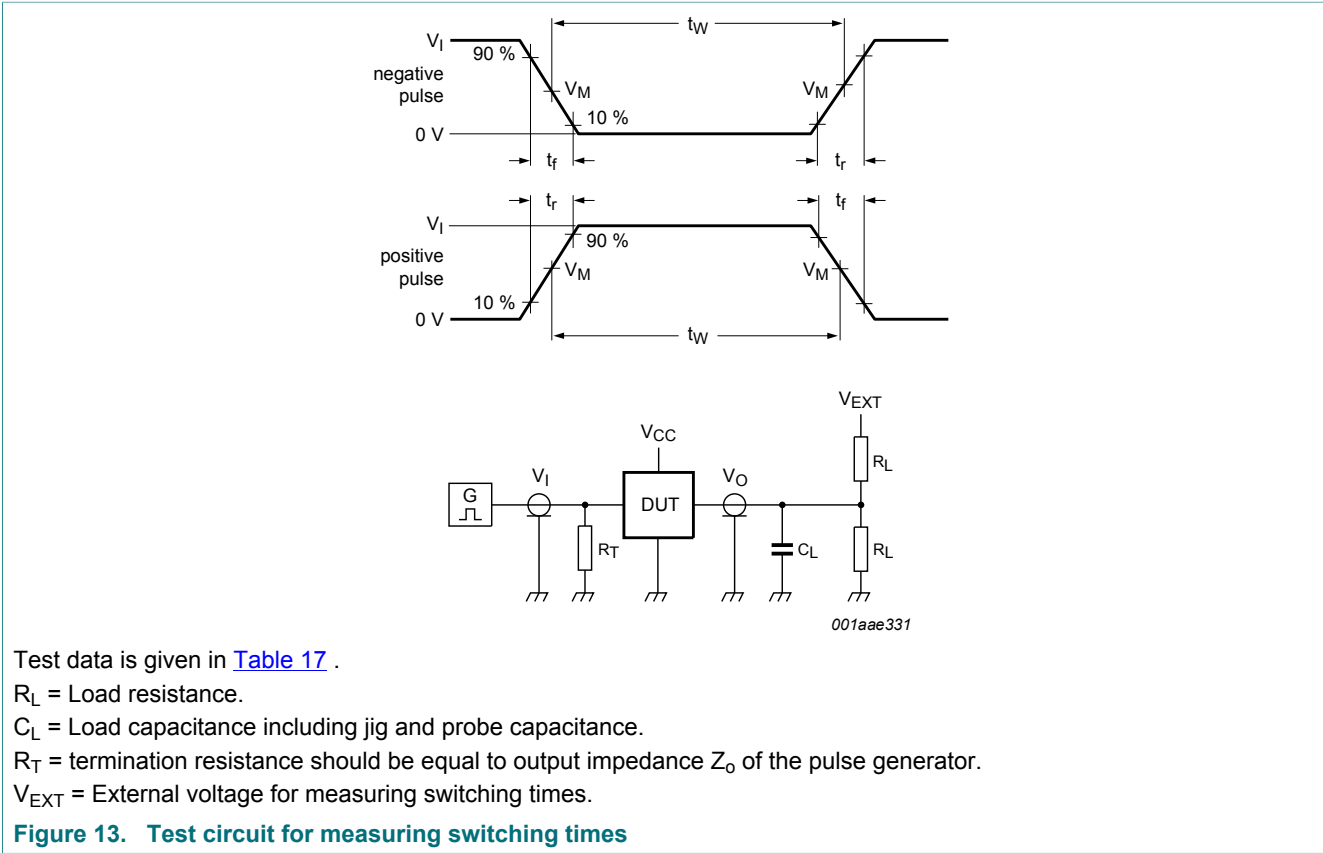
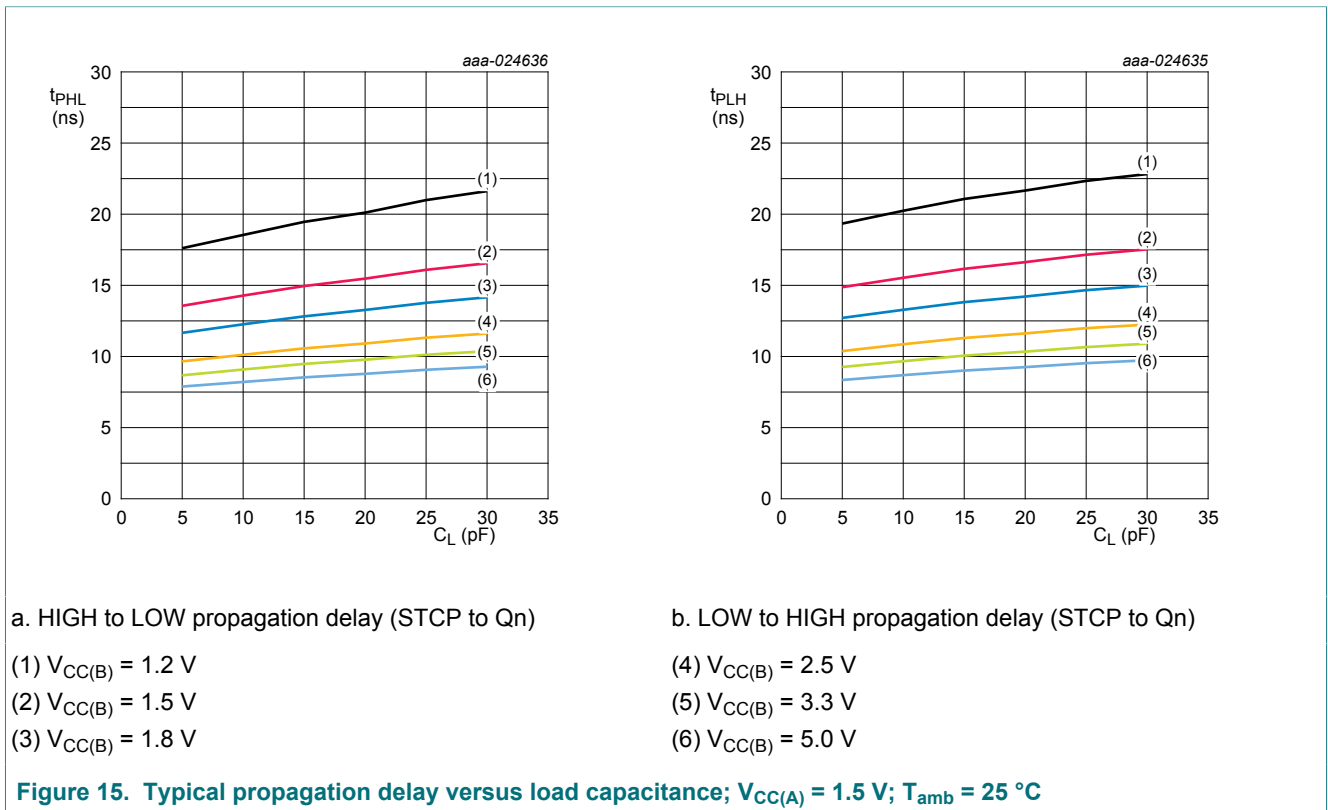
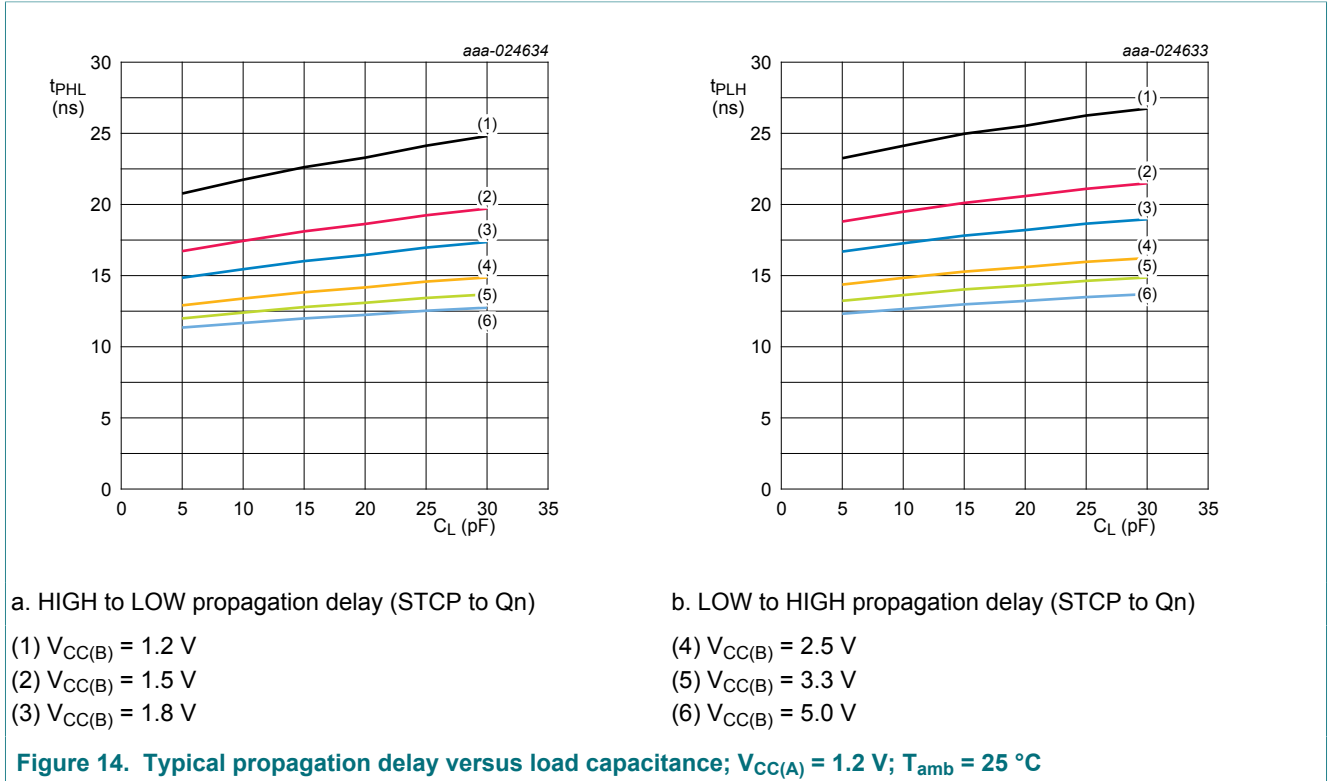


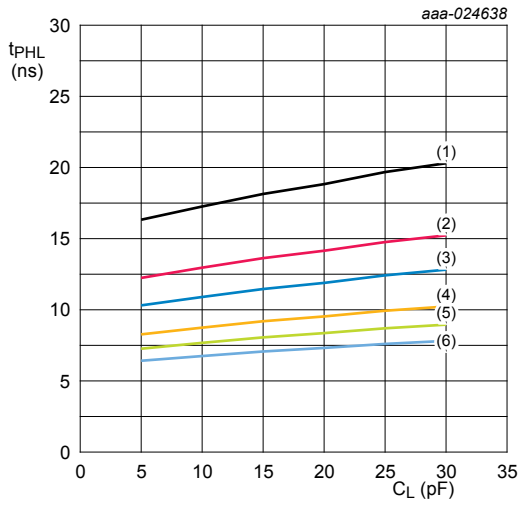
Table 17. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	V_I	$\Delta t/\Delta V$ [1]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.1 V to 5.5 V	$V_{CC(A)}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CC(B)}$

[1] $dV/dt \geq 1.0 \text{ V/ns}$

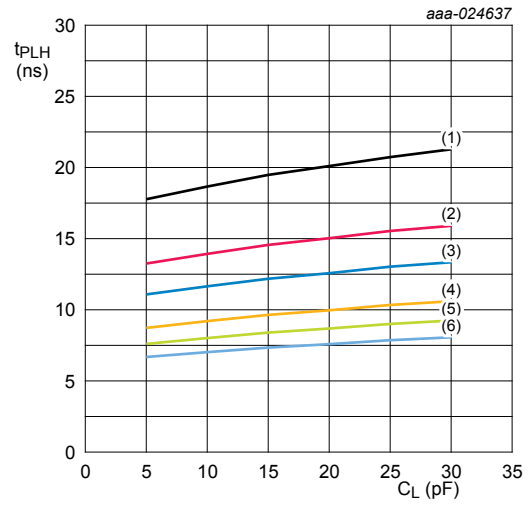
10.2 Typical propagation delay characteristics





a. HIGH to LOW propagation delay (STCP to Qn)

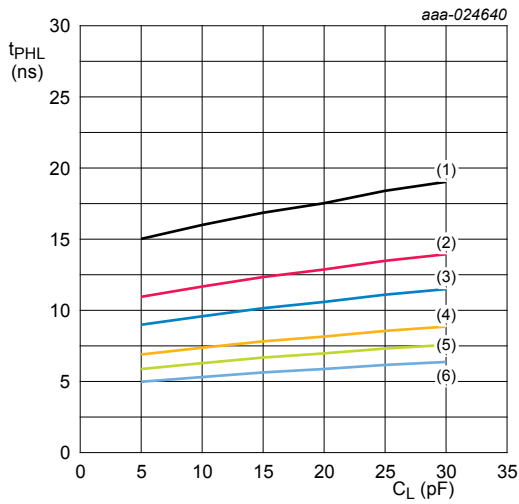
- (1) $V_{CC(B)} = 1.2\text{ V}$
- (2) $V_{CC(B)} = 1.5\text{ V}$
- (3) $V_{CC(B)} = 1.8\text{ V}$



b. LOW to HIGH propagation delay (STCP to Qn)

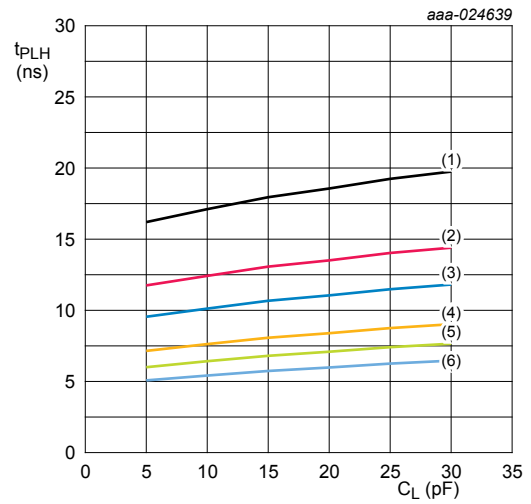
- (4) $V_{CC(B)} = 2.5\text{ V}$
- (5) $V_{CC(B)} = 3.3\text{ V}$
- (6) $V_{CC(B)} = 5.0\text{ V}$

Figure 16. Typical propagation delay versus load capacitance; $V_{CC(A)} = 1.8\text{ V}$; $T_{amb} = 25\text{ °C}$



a. HIGH to LOW propagation delay (STCP to Qn)

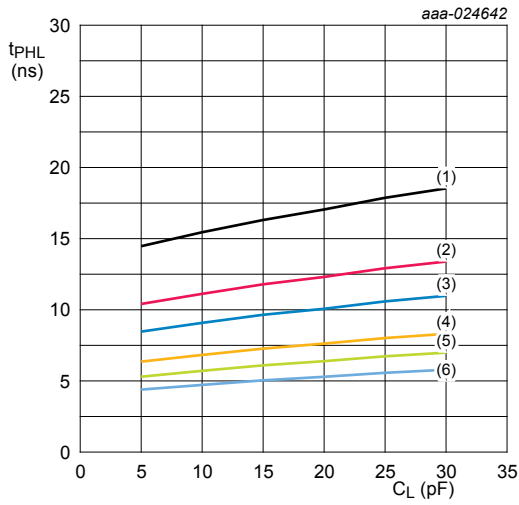
- (1) $V_{CC(B)} = 1.2\text{ V}$
- (2) $V_{CC(B)} = 1.5\text{ V}$
- (3) $V_{CC(B)} = 1.8\text{ V}$



b. LOW to HIGH propagation delay (STCP to Qn)

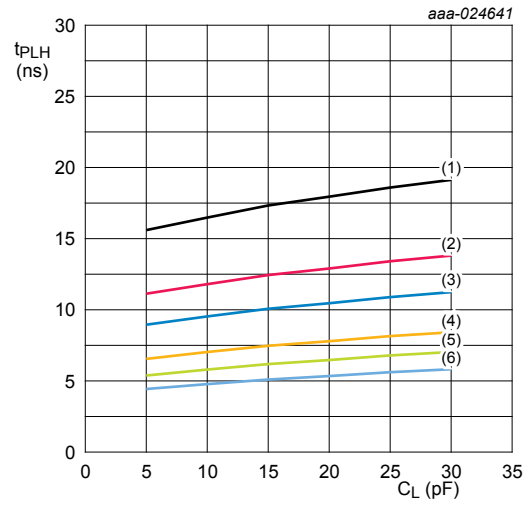
- (4) $V_{CC(B)} = 2.5\text{ V}$
- (5) $V_{CC(B)} = 3.3\text{ V}$
- (6) $V_{CC(B)} = 5.0\text{ V}$

Figure 17. Typical propagation delay versus load capacitance; $V_{CC(A)} = 2.5\text{ V}$; $T_{amb} = 25\text{ °C}$



a. HIGH to LOW propagation delay (STCP to Qn)

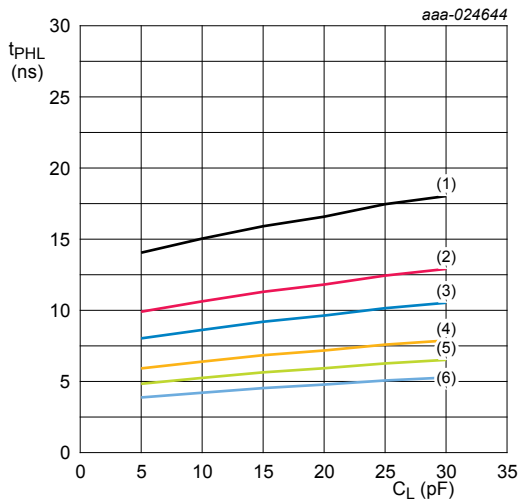
- (1) $V_{CC(B)} = 1.2\text{ V}$
- (2) $V_{CC(B)} = 1.5\text{ V}$
- (3) $V_{CC(B)} = 1.8\text{ V}$



b. LOW to HIGH propagation delay (STCP to Qn)

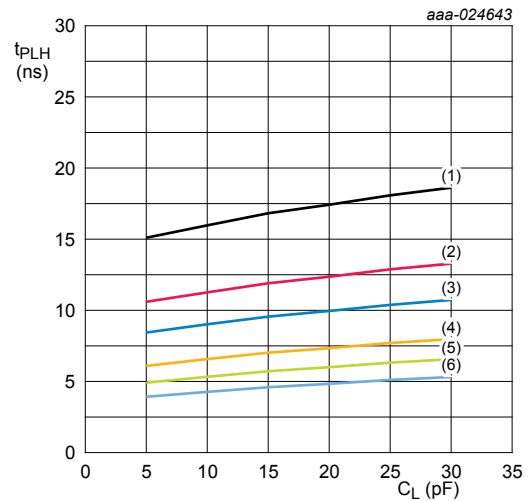
- (4) $V_{CC(B)} = 2.5\text{ V}$
- (5) $V_{CC(B)} = 3.3\text{ V}$
- (6) $V_{CC(B)} = 5.0\text{ V}$

Figure 18. Typical propagation delay versus load capacitance; $V_{CC(A)} = 3.3\text{ V}$; $T_{amb} = 25\text{ °C}$



a. HIGH to LOW propagation delay (STCP to Qn)

- (1) $V_{CC(B)} = 1.2\text{ V}$
- (2) $V_{CC(B)} = 1.5\text{ V}$
- (3) $V_{CC(B)} = 1.8\text{ V}$



b. LOW to HIGH propagation delay (STCP to Qn)

- (4) $V_{CC(B)} = 2.5\text{ V}$
- (5) $V_{CC(B)} = 3.3\text{ V}$
- (6) $V_{CC(B)} = 5.0\text{ V}$

Figure 19. Typical propagation delay versus load capacitance; $V_{CC(A)} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$

11 Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

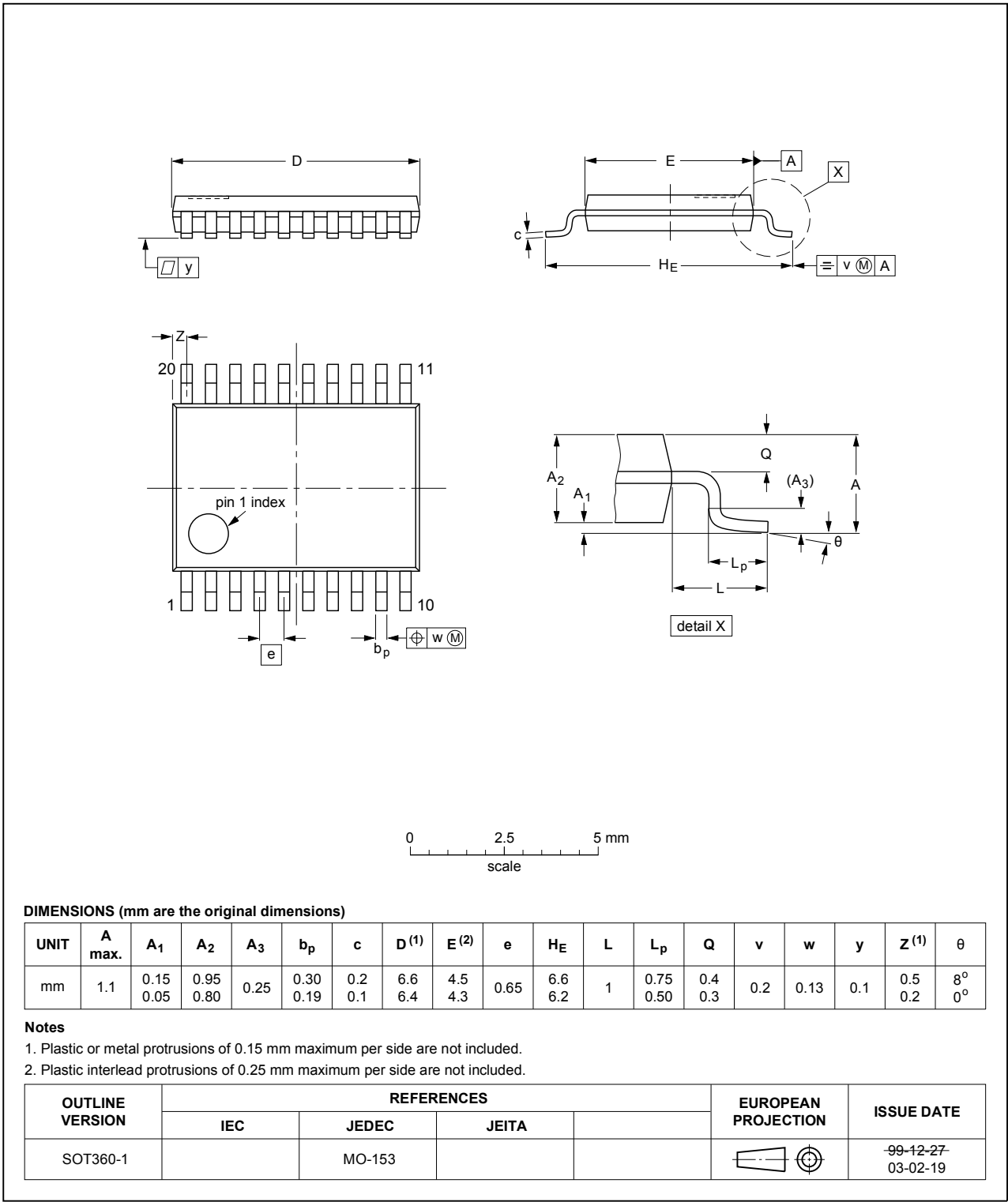
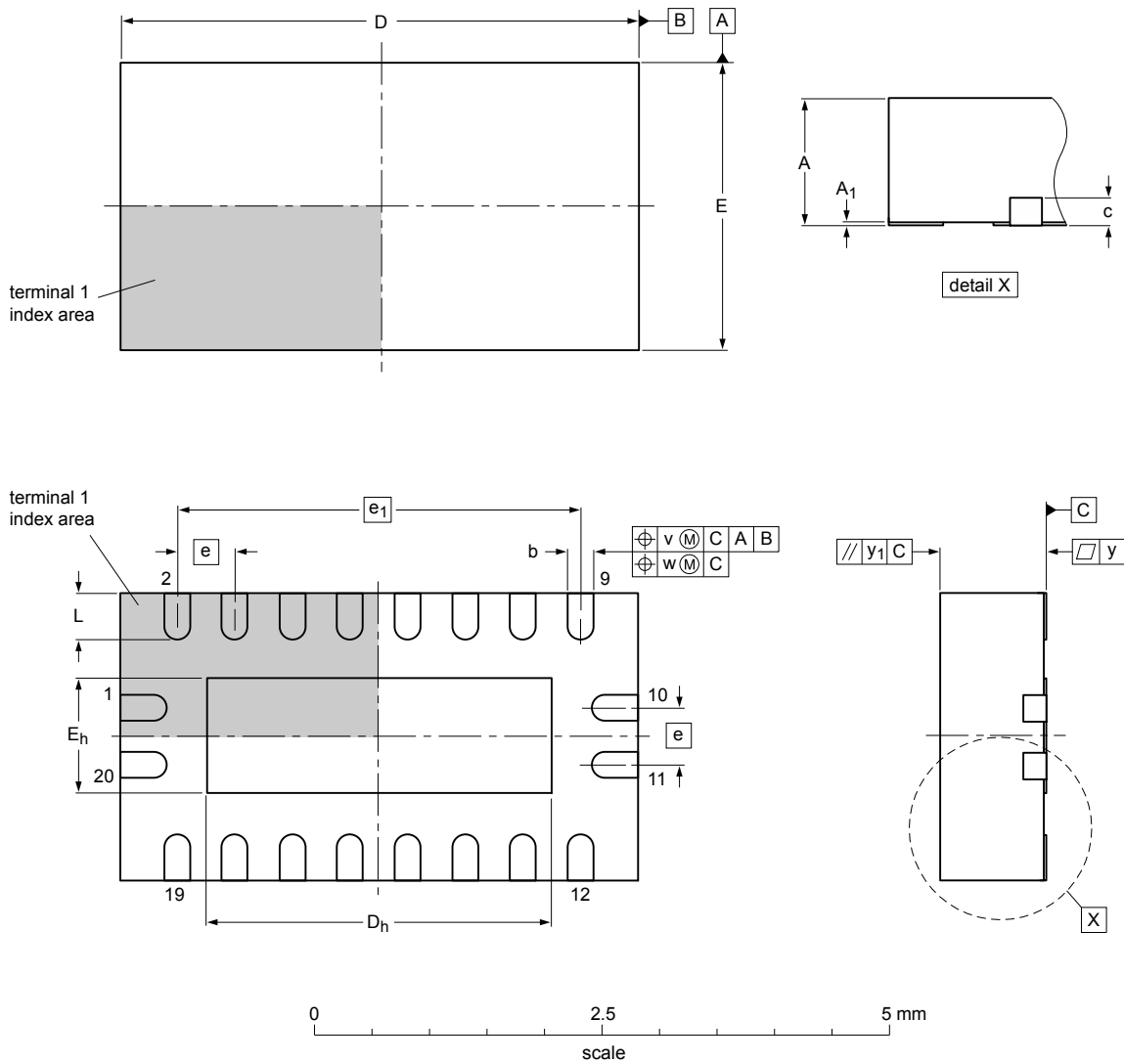


Figure 20. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Dimensions (mm are the original dimensions)

Unit	A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	---	MO-241	---			03-01-27 14-12-12

Figure 21. Package outline SOT764-1 (DHVQFN20)

12 Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13 Revision history

Table 19. Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC8T595 v.1	20170509	Product data sheet	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

14.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia. In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical

systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer

design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
7	Limiting values	6
8	Recommended operating conditions	6
9	Static characteristics	7
10	Dynamic characteristics	10
10.1	Waveforms and test circuit	21
10.2	Typical propagation delay characteristics	25
11	Package outline	28
12	Abbreviations	30
13	Revision history	30
14	Legal information	31

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© Nexperia B.V. 2017.

All rights reserved.

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 9 May 2017
Document identifier: 74LVC8T595