GV8601 Adaptive Cable Equalizer

Key Features

- HDcctv 1.0, HD-SDI (ST 292), 3G-SDI (ST 424) and SD-SDI (ST 259) compliant
- Automatic cable equalization
- Multi-standard operation from 143Mb/s to 2.97Gb/s
- Small footprint (4mm x 4mm)
- Pb-free and RoHS compliant
- Manual bypass (useful for low data rates with slow rise/fall times)
- Performance optimized for 1.485Gb/s (HDcctv/HD-SDI) and 2.970Gb/s
- Differential outputs support DC coupling to 3.3V and 2.5V CML logic
- Typical equalized length of Belden 1694A cable: 140m at 2.97Gb/s
- Typical equalized length of Belden 543945 HDcctv 1.1 reference cable: 150m at 1.485Gb/s
- Typical equalized length of Belden 543945 HDcctv 1.1 reference cable: 330m at 270Mb/s (HD-VLC™)
- 50Ω differential output (internal 50Ω pull-ups)
- Single 3.3V power supply operation
- Operating temperature range: -20°C to +85°C

Applications

- Digital video recorders (DVR)
- Video capture cards
- Video monitors and displays
- Video mixers and switchers
- Video servers
- Camcorders
- Distribution amplifiers
- Repeaters

Description

The GV8601 is a high-speed BiCMOS integrated circuit designed to equalize and restore signals received over 75Ω coaxial cable.

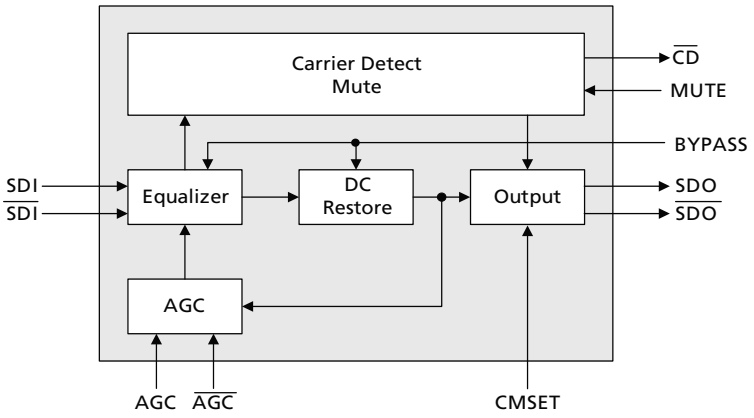
The GV8601 is designed to support HDcctv 1.0, ST 292 and ST 424, and is optimized for performance at 1.485Gb/s and 2.97Gb/s serial data.

The GV8601 features DC restoration to compensate for the DC content of HDcctv 1.1 pathological test patterns.

The differential outputs can be DC-coupled to industry-standard 3.3V and 2.5V CML logic using the CMSET pin.

Power consumption is typically 195mW using a 3.3V power supply. The GV8601 is lead-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogenous subcomponents are RoHs compliant.



GV8601 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
1	010001	–	November 2012	Changed Moisture Sensitivity Level to 1 in Section 6.2.
0	158552	–	September 2012	New document.

Contents

1. Pin Out

1.1 GV8601 Pin Assignment

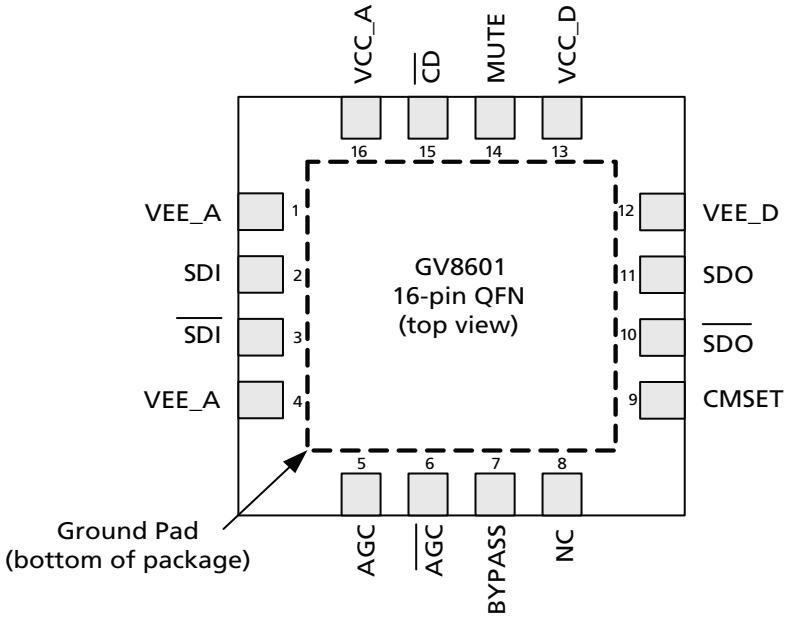


Figure 1-1: GV8601 Pin Out

1.2 GV8601 Pin Descriptions

Table 1-1: GV8601 Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	VEE_A	Analog	Power	Most negative power supply for analog circuitry. Connect to GND.
2, 3	SDI, $\overline{\text{SDI}}$	Analog	Input	Serial digital differential input.
4	VEE_A	Analog	Power	Most negative power supply for analog circuitry. Connect to GND.
5, 6	AGC, $\overline{\text{AGC}}$	Analog	–	External AGC capacitor. Connect pin 5 and pin 6 together as shown in the Typical Application Circuit on page 12.
7	BYPASS	Not Synchronous	Input	Forces the Equalizing and DC RESTORE stages into bypass mode when HIGH. No equalization occurs in this mode. (Internal pull-down).
8	NC	–	–	No connect.
9	CMSET	Not Synchronous	Input	CONTROL SIGNAL INPUT levels are LVCMOS/LVTTL compatible. (3.3V Tolerant) Controls output common mode level. (Internal pull-down). See Section 4.5.

Table 1-1: GV8601 Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
10, 11	$\overline{SDO}$, SDO	Analog	Output	Equalized serial digital differential output.
12	VEE_D	Analog	Power	Most negative power supply for the digital circuitry and output buffer. Connect to GND.
13	VCC_D	Analog	Power	Most positive power supply for the digital I/O pins of the device. Connect to +3.3V DC.
14	MUTE	Not Synchronous	Input	CONTROL SIGNAL INPUT levels are LVCMOS/LVTTL compatible. (3.3V Tolerant) Controls output behaviour on SDO and $\overline{SDO}$. (Internal pull-down). See Section 4.4.
15	$\overline{CD}$	Not Synchronous	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence of an input signal. See Section 4.4.
16	VCC_A	Analog	Power	Most positive power supply for the analog circuitry of the device. Connect to +3.3V DC.
–	Center Pad	–	Power	Internally bonded to VEE_A.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to +3.6V DC
Input ESD Voltage (HBM)	5kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	-20°C to +85°C
Functional Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V	–
Power Consumption	P_D	T_A = 25°C	–	195	250	mW	–
Supply Current	I_s	T_A = 25°C	–	59	–	mA	–
Output Common Mode Voltage	V_{CMOUT}	T_A = 25°C	–	V_{CMSET} - ΔV_{SDO}/2	–	V	1
Input Common Mode Voltage	V_{CMIN}	T_A = 25°C	–	1.8	–	V	–
$\overline{CD}$ Output Voltage	$V_{\overline{CD}(OH)}$	Carrier not present	2.4	–	–	V	–
	$V_{\overline{CD}(OL)}$	Carrier present	–	–	0.4	V	–
Mute Input Voltage Required to Force Outputs to Mute	V_{Mute}	Min to Mute	2.0	–	–	V	–
Mute Input Voltage Required to Force Outputs Active	V_{Mute}	Max to Activate	–	–	0.8	V	–

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	143	–	2970	Mb/s	–
Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential, 270Mb/s and 1.485Gb/s	720	800	950	mV_{p-p}	1
		T_A =25°C, differential, 2.97Gb/s	720	800	880	mV_{p-p}	1
Output Voltage Swing	ΔV_{SDO}	100Ω load, T_A =25°C, differential	680	800	900	mV_{p-p}	–
Output Jitter of Various Cable Lengths and Data Rates	–	2.97Gb/s Belden 1694A: 0-120m	–	–	0.25	UI	2, 5
	–	2.97Gb/s Belden 1694A: 120-140m	–	0.3	–	UI	3, 5
	–	1.485Gb/s Belden 1694A: 0-160m	–	–	0.25	UI	2, 5
	–	1.485Gb/s Belden 1694A: 160-200m	–	0.2	–	UI	3, 5
	–	270Mb/s Belden 1694A: 0-400m	–	–	0.2	UI	2, 5
Output Rise/Fall time	–	2.97Gb/s & 1.485Gb/s 20% - 80%	35	65	90	ps	–
Mismatch in rise/fall time	–	–	–	–	30	ps	–
Duty cycle distortion	–	–	–	–	30	ps	–
Overshoot	–	–	–	–	10	%	–
Input Return Loss	–	–	15	21	–	dB	4
Input Resistance	–	single ended	–	1.9	–	kΩ	–
Input Capacitance	–	single ended	–	1.3	–	pF	–
Output Resistance	–	single ended	–	50	–	Ω	–

NOTES:

1. 0m cable length.
2. All parts are production tested. In order to guarantee jitter over the full range of specification (V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, and 720-880mV launch swing from the SDI cable driver) the recommended applications circuit must be used.
3. Based on characterization data using the recommended applications circuit, at V_{CC} = 3.3V, T_A = 25°C and 800mV launch swing from the SDI cable driver.
4. Tested on a Semtech evaluation board from 5MHz to 3GHz.

3. Input/Output Circuits

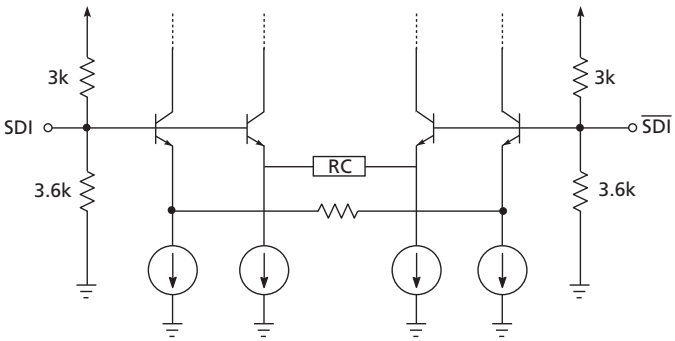


Figure 3-1: Input Equivalent Circuit

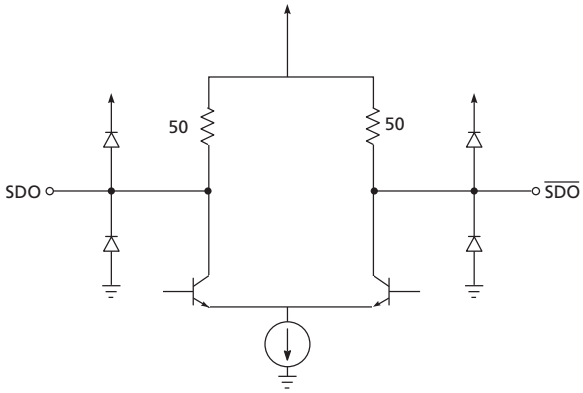


Figure 3-2: Output Circuit

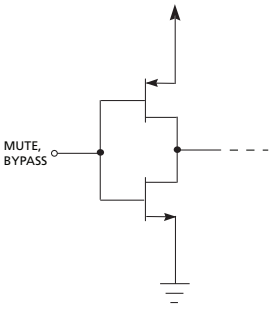


Figure 3-3: MUTE and BYPASS Circuits

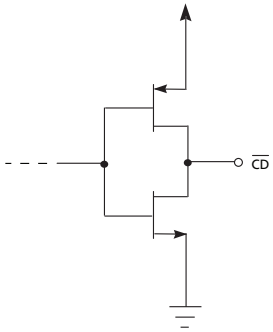


Figure 3-4: $\overline{CD}$ Circuit

4. Detailed Description

The GV8601 is a high-speed BiCMOS IC designed to equalize serial digital video signals.

The GV8601 can equalize 3Gb/s, HDcctv/HD-SDI and SD-SDI serial digital signals, and will typically equalize 150m of Belden 543945 HDcctv 1.1 reference cable at 1.485Gb/s and 140m of Belden 1694A cable at 2.970Gb/s. When used for HD-VLC™ applications at 270Mb/s, the GV8601 will typically equalize signals over 330m of Belden 543945. The GV8601 is powered from a single +3.3V power supply and consumes approximately 195mW of power.

4.1 Serial Digital Inputs

The Serial Data Signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

4.2 Cable Equalization

The input signal passes through a variable gain equalizing stage, whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling.

4.3 Serial Digital Outputs

The digital output signals have a nominal voltage of 800mV$_{pp}$ differential, or 400mV$_{pp}$ single-ended when terminated with 50Ω as shown in Figure 4-1.

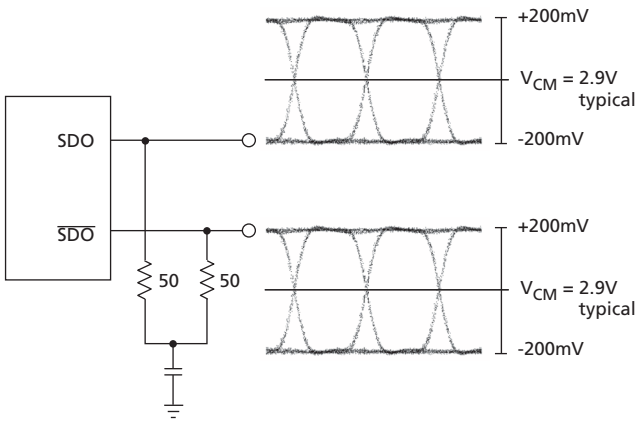


Figure 4-1: Typical Output Voltage Levels (for 3.3V Common Mode)

4.4 Mute and Carrier Detect

The GV8601 includes a MUTE input pin that allows the application interface to mute the Serial Digital Output at any time. Set the MUTE pin HIGH to mute SDO and $\overline{\text{SDO}}$. In this case, the outputs will mute regardless of the setting of the BYPASS pin.

A Carrier Detect output pin ($\overline{\text{CD}}$) indicates the presence of a valid signal at the input of the GV8601. When $\overline{\text{CD}}$ is LOW, the device has detected a valid input on SDI and $\overline{\text{SDI}}$. When $\overline{\text{CD}}$ is HIGH, the device has not detected a valid input.

NOTE 1: $\overline{\text{CD}}$ will only detect loss of carrier for data rates greater than 19Mb/s. The $\overline{\text{CD}}$ output pin may be connected directly to the MUTE input pin to enable automatic muting of the GV8601 when no valid input signal has been detected.

Table 4-1: Mute Input Table

Mute	Function
0	SDO and $\overline{\text{SDO}}$ operate normally
1	SDO and $\overline{\text{SDO}}$ are forced to a steady state (either high or low)

Table 4-2: $\overline{\text{CD}}$ Output Table

$\overline{\text{CD}}$	Input Status
0	Valid Input on SDI, $\overline{\text{SDI}}$ pins
1	Input is not valid

4.5 CMSET Operation

The GV8601 has a selectable output common mode level. This is useful when interfacing to chips that can accept 2.5V input common mode levels. In these cases, AC coupling can be avoided by selecting the correct output common mode.

Table 4-3: CMSET Output Table

CMSET	Output Common Mode Voltage Level
0	The output common mode will be compatible with 3.3V CML
1	The output common mode will be compatible with 2.5V CML

NOTE 1: See Section 2.2 for Output Common Mode Voltage specification.

NOTE 2: When the GV8601 is used in a GV8501 design, the CMSET pin will be tied to ground (VEE_D on GV8501). Therefore, the output common mode will be permanently set to 3.3V.

5. Application Information

5.1 High Gain Adaptive Cable Equalizers

In order to continue to extend the cable length that an equalizer will remain operational over, it is necessary to have high gain in the equalizer.

A video cable equalizer must provide wide band gain over a range of frequencies in order to accommodate the range of data rates and signal patterns that are present in a HDcctv and SMPTE compliant serial video streams.

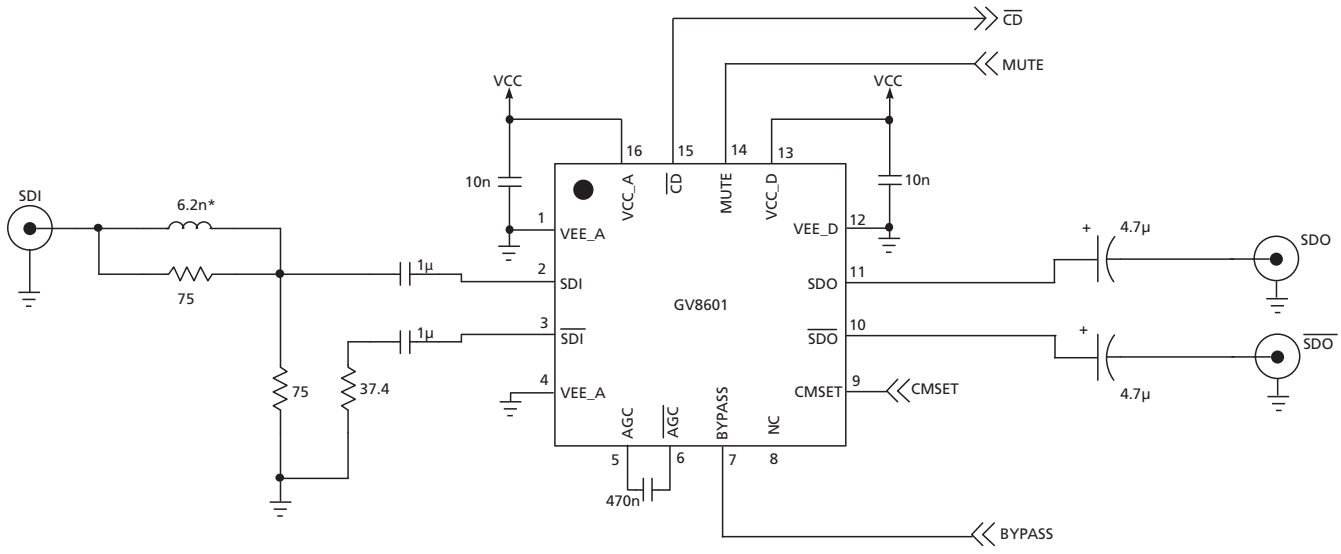
The GV8601 has an increase in gain over the GV8501 at critical 1.5Gb/s and 3Gb/s frequencies. Small levels of signal or noise present at the input pins of the Equalizer may cause chatter at the output. In order to prevent this from happening, particular attention must be paid to board layout.

5.2 PCB Layout

Special attention must be paid to component layout when designing High-Speed Serial Digital Interfaces. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for 3Gb/s rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- The PCB ground plane is removed under the GV8601 input components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GV8601 output components to minimize parasitic capacitance.
- High speed traces are curved to minimize impedance changes.

5.3 Typical Application Circuit

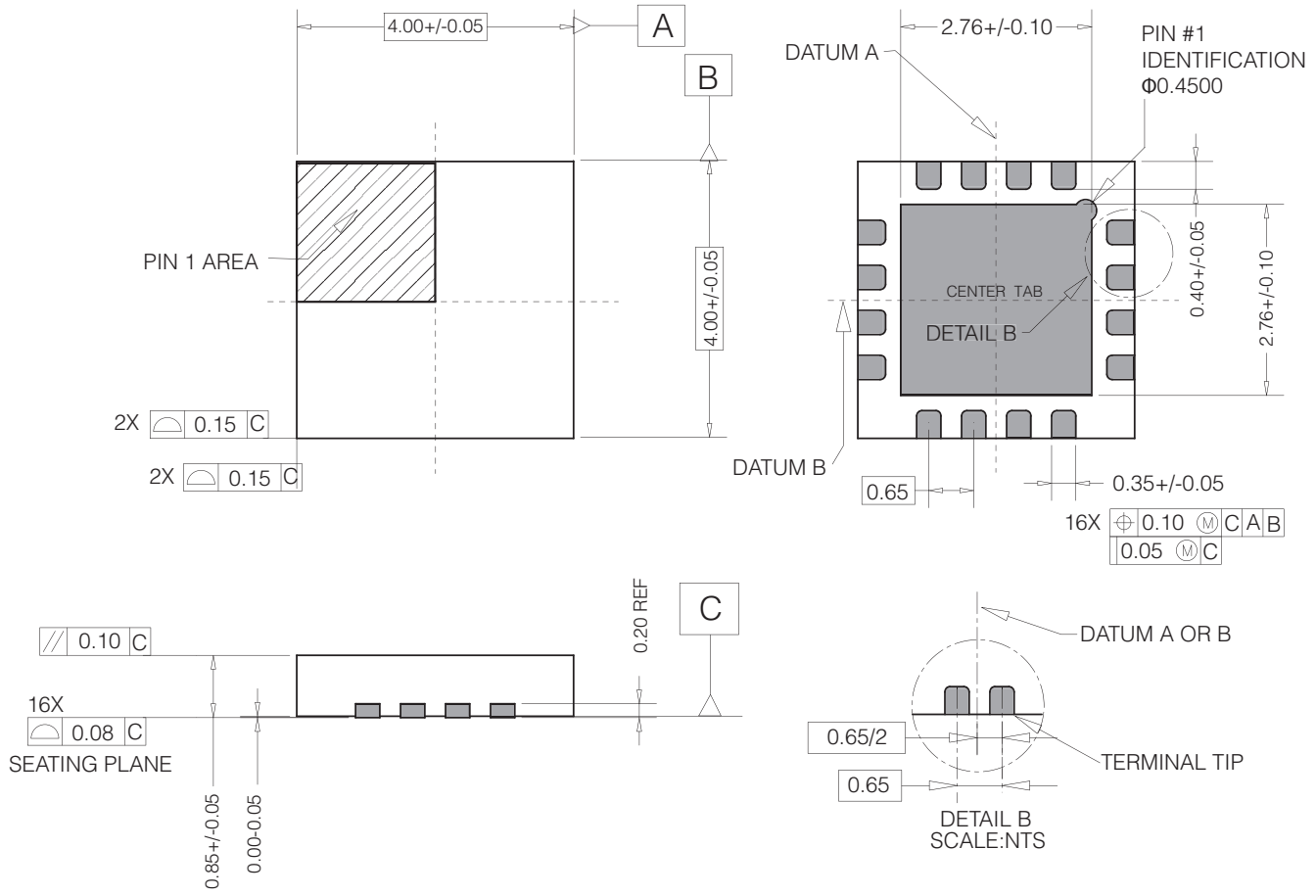


NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.
* Value dependent on layout

Figure 5-1: GV8601 Typical Application Circuit

6. Package & Ordering Information

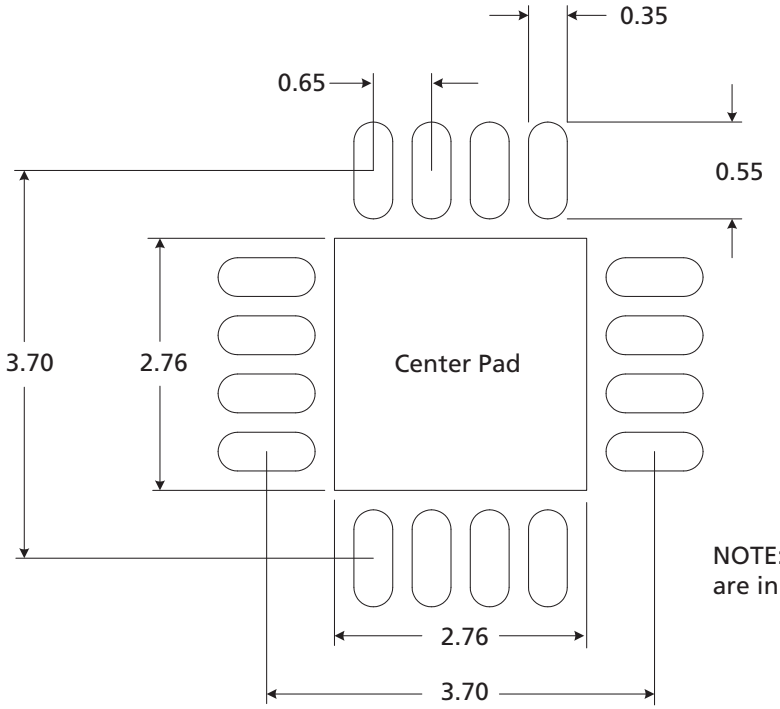
6.1 Package Dimensions



6.2 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

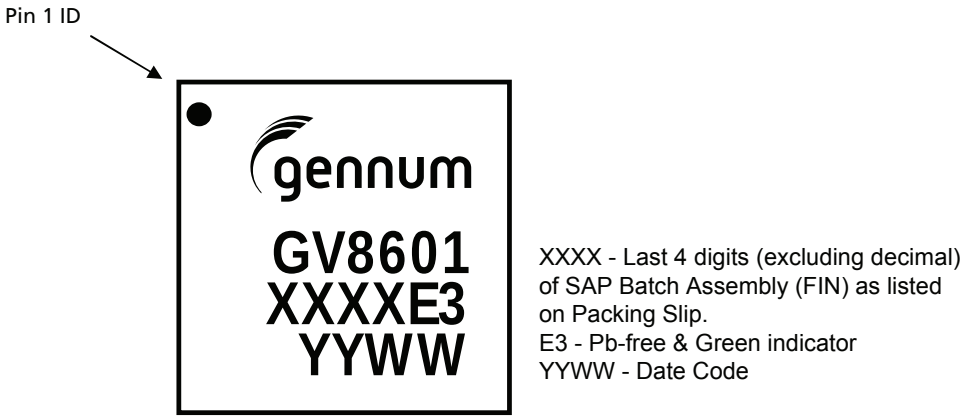
6.3 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE_A) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.4 Marking Diagram



6.5 Solder Reflow Profiles

The GV8601 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-1.

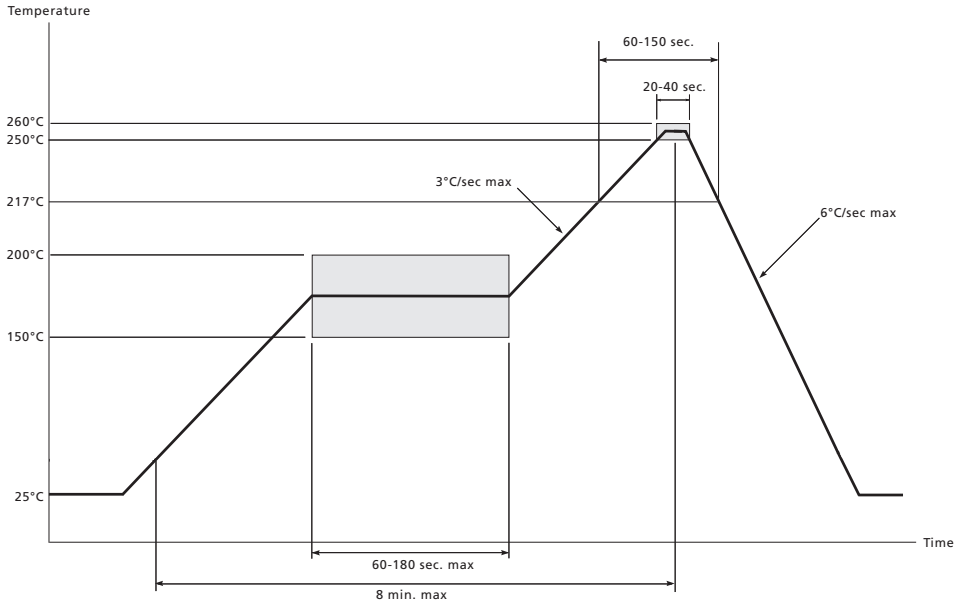


Figure 6-1: Maximum Pb-free Solder Reflow Profile

6.6 Ordering Information

	Part Number	Package	Temperature Range
GV8601	GV8601-INE3	16-pin QFN	-40°C to 85°C

DOCUMENT IDENTIFICATION
FINAL DATA SHEET

Information relating to this product and the application or design described herein is believed to be reliable, however such information is provided as a guide only and Semtech assumes no liability for any errors in this document, or for the application or design described herein. Semtech reserves the right to make changes to the product or this document at any time without notice.

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

Contact Information

Semtech Corporation
Gennum Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com