LC717A30UJ

Capacitance-Digital-Converter LSI for Electrostatic Capacitive Touch Sensors

The LC717A30UJ is a high performance, low cost, and highly usable capacitance converter for electrostatic capacitive touch and proximity sensors.
8 capacitance-sensing input channels ideal for use in any end products that needs an array of switches. The LC717A30J facilitates a short system development time through its automatic calibration function and minimal external components. The detection result (ON/OFF) for each sensor is read out by the serial interface (I^2C or SPI).

Features

- Differential capacitive detection using mutual capacitance.
- Operates with small to large capacitance sensor input pads.
- Capacitance detection down to femto-Farad level.
- Measurement time 16 ms for 8 sensors.
- Minimal external components.
- Selectable interface : I²C or SPI.
- Current consumption : 0.8 mA (V_{DD} = 5.5 V)
- Supply voltage : 2.6 V to 5.5 V
- AEC-Q100 qualified and PPAP capable.

Typical Applications

- Automotive : Smart key, Control switches, Car audio, Proximity
- Consumer : Home Appliance, White goods, Induction Cooking
- Industrial : Security lock
- Computing : PC Peripherals, Audio Visual equipment
- Lighting : Remote control switches

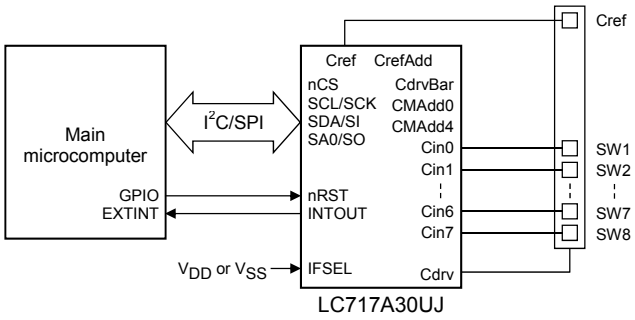
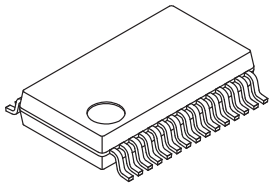


Figure 1. Application Schematic 1

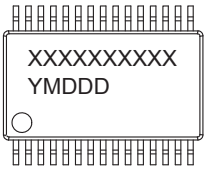
ON Semiconductor®

www.onsemi.com



SSOP30 (225mil)
8.0 x 6.4 x 1.6 mm

MARKING DIAGRAM



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

Ordering Code:
LC717A30UJ-AH

Package:
SSOP30 (225mil)
(Pb-Free / Halogen Free)

Shipping (Qty / Packing):
1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

8 small capacitance sensors channels and 4-wire SPI interface.

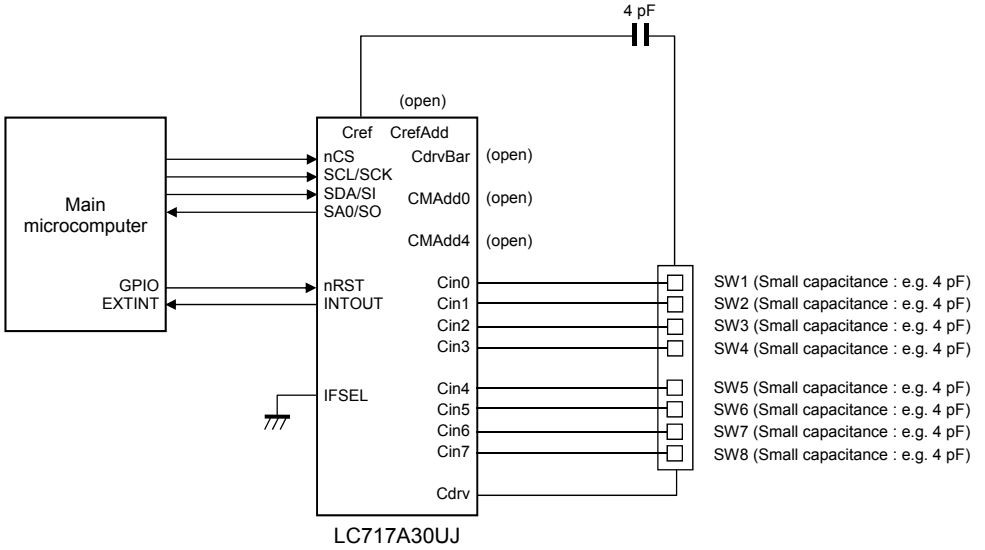


Figure 2. Application Schematic 2

8 Large capacitance sensors and I^2C interface.

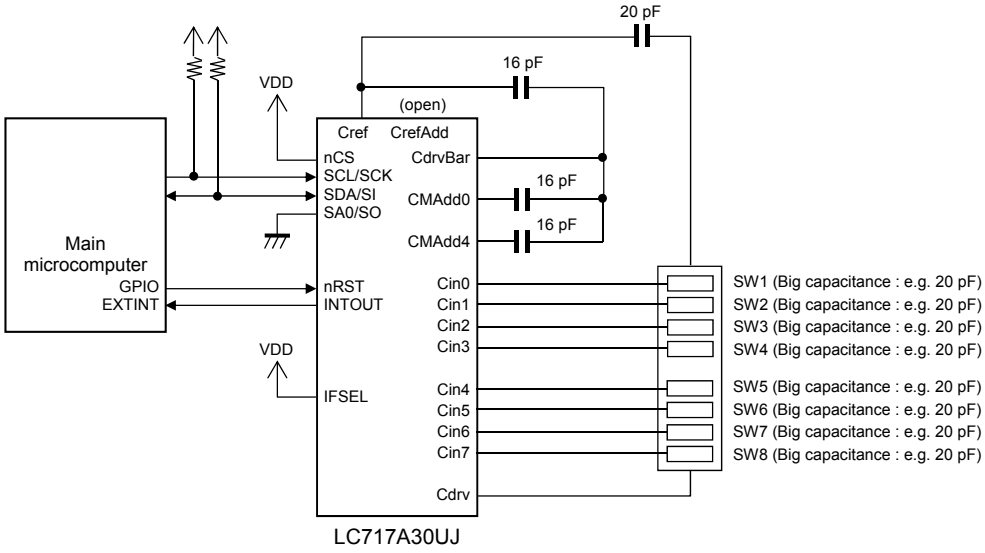


Figure 3. Application Schematic 3

BLOCK DIAGRAM

The LC717A30UJ is a capacitance-digital converter LSI that can detect capacitance at the femto farad level. It consists a multiplexer that selects the input channels, a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values, an A/D converter, a system clock, a power-on reset circuit, control logic and interface, I^2C bus or SPI.

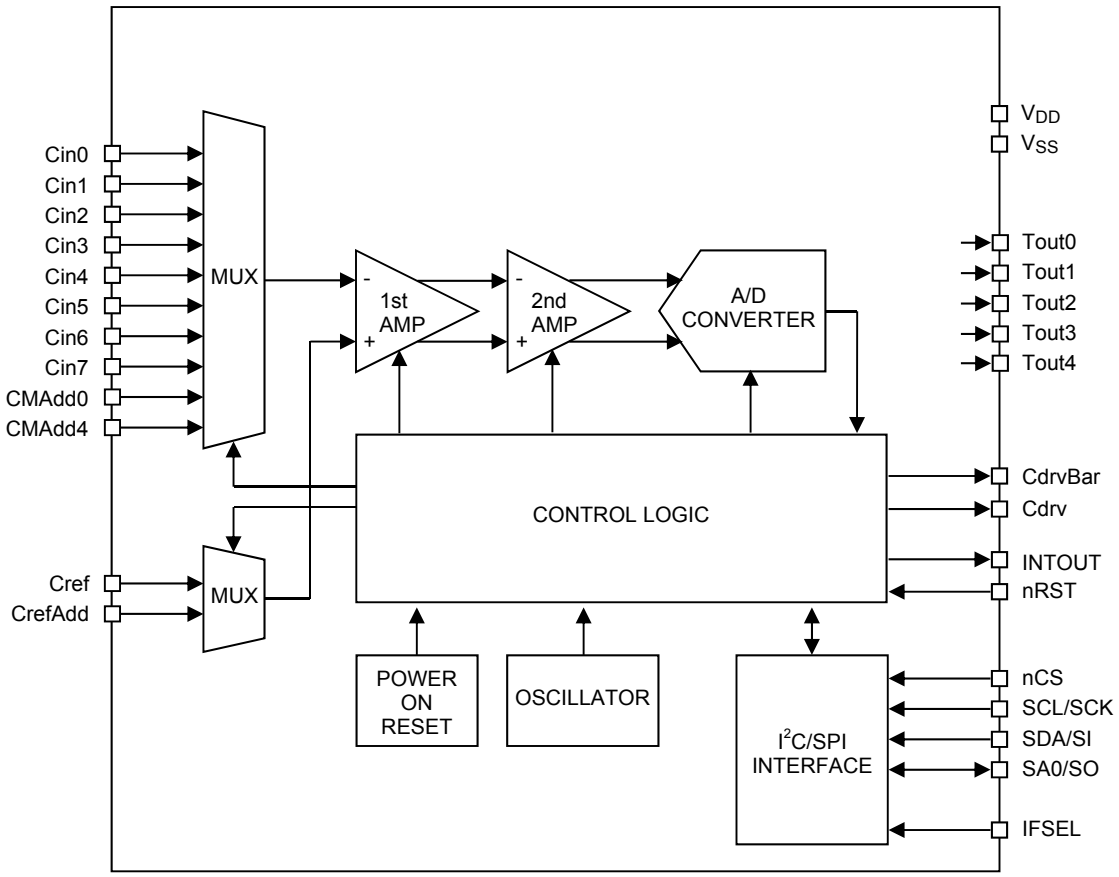


Figure 4. Simplified Block Diagram

Pin Assignment

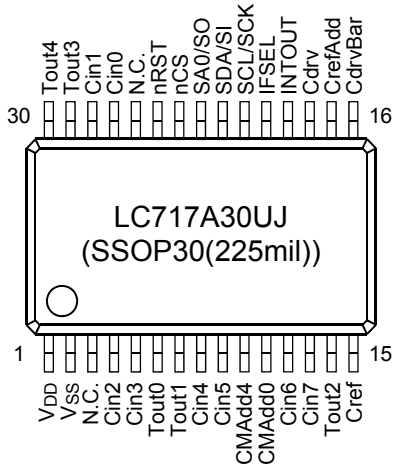


Figure 5. Pin Assignment (Top View)

PIN DISCRIPTION

Pin No.	Pin Name	I/O	Description
1	V_{DD}	Power	Power supply (+2.6 V to +5.5 V) (Note 1)
2	V_{SS}	Power	Ground (Note 1, 2)
3	Non Connect	-	Connect to Ground
27	Cin0	I/O	Sensor inputs. Cin0 to Cin7 are connected to the inverting input of the 1st amplifier through the multiplexer. All unused input pins must remain open. Cdrv and Cin printed circuit board patterns should be close to each other as they are capacitively coupled.
28	Cin1	I/O	
4	Cin2	I/O	
5	Cin3	I/O	
8	Cin4	I/O	
9	Cin5	I/O	
12	Cin6	I/O	
13	Cin7	I/O	
6	Tout0	O	Test pin, must remain open.
7	Tout1	O	Test pin, must remain open.
10	CMAdd4	I/O	Offset capacitance input pin for the sensor inputs 4 to 7. When using large sensor pads with high capacitance, additional capacitance is added between CMAdd4 and CdrvBar. See figure 3. Remain open if not in use.
11	CMAdd0	I/O	Offset capacitance input pin for the sensor inputs 0 to 3. When using large sensor pads with high capacitance, additional capacitance is added between CMAdd4 and CdrvBar. See figure 3. Remain open if not in use.
14	Tout2	O	Test pin, must remain open.
15	Cref	I/O	Reference capacitance input pins. See Figure 2 and 3. When using large sensor pads with high capacitance, additional capacitance maybe added for Cref. See Figure 3. Remain open if not in use.
17	CrefAdd	I/O	

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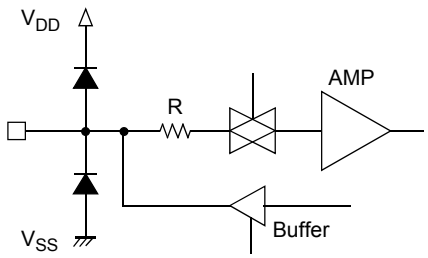
Pin No.	Pin Name	I/O	Descriptions
16	CdrvBar	O	Capacitance sensors drive signal inversion output When using large sensor pads with high capacitance, additional capacitance is added between CMAdd0 and CMAdd4 and CdrvBar. See figure 3. Remain open if not in use.
18	Cdrv	O	Capacitance sensors drive output. Cdrv and Cin printed circuit board patterns should be close to each other as they are capacitively coupled.
19	INTOUT	O	Interrupt output pin. (Active high). Remain open if not in use.
20	IFSEL	I	Interface Select. IFSEL = "Low"(V_{SS}) : SPI mode IFSEL = "High"(V_{DD}) : I^2C mode
21	SCL/SCK	I	I^2C = SCL clock input SPI = SCK clock input
22	SDA/SI	I/O	I^2C = SDA data input/output SPI = SI data input
23	SA0/SO	I/O	I^2C = SA0 slave address selection input. SPI = SO data output
24	nCS	I	I^2C = "High"(V_{DD}). SPI = nCS chip select inversion input.
25	nRST	I	Reset signal inversion input pin. nRST = "Low"(V_{SS}), in reset state. Cin0 to Cin7, CMAdd0, CMAdd4, Cref, CrefAdd, CdrvBar and Tout0 to Tout4 are "Hi-Z"
26	Non Connect	-	Connect to Ground.
29	Tout3	O	Test pin, must remain open.
30	Tout4	O	Test pin, must remain open.

Note 1 : For noise de-coupling place a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS}. The small-valued capacitor, at least 0.1 μF, should be mounted near the LSI.

Note 2 : When V_{SS} terminal is not grounded, in battery-powered mobile equipment, detection sensitivity may be degraded.

PIN FUNCTIONS

Pin No.	Pin Name	I/O	Pin Functions	Pin Type
1	V_{DD}	Power	Power supply (+2.6 V to +5.5 V)	
2	V_{SS}	Power	Ground	
27	Cin0	I/O	Capacitance sensor input 0	
28	Cin1	I/O	Capacitance sensor input 1	
4	Cin2	I/O	Capacitance sensor input 2	
5	Cin3	I/O	Capacitance sensor input 3	
8	Cin4	I/O	Capacitance sensor input 4	
9	Cin5	I/O	Capacitance sensor input 5	
12	Cin6	I/O	Capacitance sensor input 6	
13	Cin7	I/O	Capacitance sensor input 7	
10	CMAdd4	I/O	Additional offset capacitance input pin for the sensor inputs 4 to 7.	
11	CMAdd0	I/O	Additional offset capacitance input pin for the sensor inputs 0 to 3.	
15	Cref	I/O	Reference capacitance input	
17	CrefAdd	I/O	Additional Reference capacitance input	

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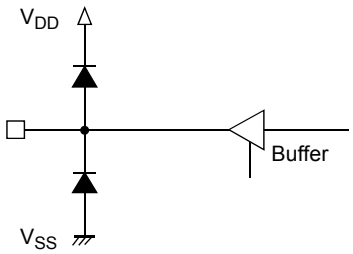
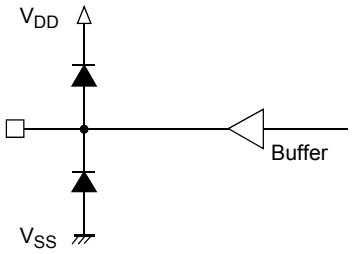
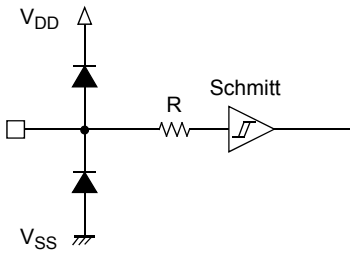
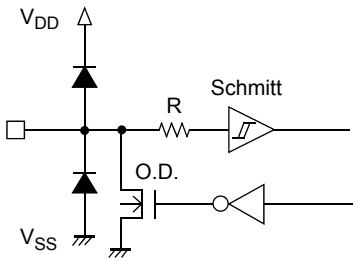
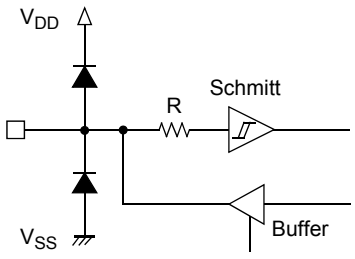
Pin No.	Pin Name	I/O	Pin Functions	Pin Type
6	Tout0	O	Output for tests	
7	Tout1	O	Output for tests	
14	Tout2	O	Output for tests	
29	Tout3	O	Output for tests	
30	Tout4	O	Output for tests	
16	CdrvBar	O	Capacitance sensors drive signal inversion output	
18	Cdrv	O	Capacitance sensors drive output	
19	INTOUT	O	Interrupt output	
20	IFSEL	I	Switching control input of the serial data communication interface	
21	SCL/SCK	I	SCL clock input (I^2C)	
		I	SCK clock input (SPI)	
24	nCS	I	nCS chip select inversion input (SPI)	
25	nRST	I	External reset signal inversion input	
22	SDA/SI	I/O	SDA data input/output (I^2C)	
		I	SI data input (SPI)	
23	SA0/SO	I	SA0 slave address selection input (I^2C)	
		O	SO data output (SPI)	

MAXIMUM RATINGS at V_{SS} = 0 V, T_A = +25°C (Note 3)

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{DD}	−0.3 to +6.5	V
Input Voltage Range (Note 4)	V_{IN}	−0.3 to V_{DD}+0.3	V
Output Voltage Range (Note 5)	V_{OUT}	−0.3 to V_{DD}+0.3	V
Peak Output Current Range (Notes 5, 6)	I_{OP}	−8.0 to +8.0	mA
Total Outputs Current Range (Note 7)	I_{OA}	−40 to +40	mA
Maximum Power Dissipation (Note 8)	P_{dmax}	160	mW

Note 3 : Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
4 : Apply to Cin0 to Cin7, CMAdd0, CMAdd4, Cref, CrefAdd ,SCL/SCK ,SDA/SI ,SA0, nCS, nRST, IFSEL.
5 : Apply to Cdrv, CdrvBar, SDA, SO, INTOUT, Tout0 to Tout4.
6 : Total value with duty cycle under 25%.
7 : Limited to one pin, with duty cycle under 50%.
8 : T_A = 105°C, Single-layer glass epoxy board (76.1 x 114.3 x 1.6 mm)

RECOMMENDED OPERATING RANGES at V_{SS} = 0 V (Note 9)

Parameter	Symbol	Min	Max	Unit
Operating Supply Voltage Range (Note 10)	V_{DD}	2.6	5.5	V
Input High-level Voltage Range (Note 11)	V_{IH}	0.8V_{DD}	V_{DD}	V
Input Low-level Voltage Range (Note 11)	V_{IL}	0	0.2V_{DD}	V
Ambient Temperature Range	T_A	−40	105	°C

Note 9 : Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
10 : For noise de-coupling place a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS}. The small-valued capacitor, at least 0.1 μF, should be mounted near the LSI. In addition, it is recommended that the power supply ripple + noise is less than ±40 mV.
11 : Apply to SCL/SCK ,SDA/SI ,SA0, nCS, nRST, IFSEL.

ELECTRICAL CHARACTERICALS at V_{DD} = 2.6 to 5.5 V, V_{SS} = 0 V, T_A = −40 to + 105°C, (Note 12)
Unless otherwise specified, the Cdrv drive frequency is f_{CDRV} = 121 kHz.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Common						
Output High-level Voltage (Note 13)	I_O = −1.5 mA, V_{DD} = 2.6 to 3.6 V	V_{OH1}	0.8V_{DD}			V
	I_O = −3.0 mA, V_{DD} = 3.6 to 5.5 V	V_{OH2}	0.8V_{DD}			V
Output Low-level Voltage (Note 13)	I_O = +1.5 mA, V_{DD} = 2.6 to 3.6 V	V_{OL1}			0.2V_{DD}	V
	I_O = +3.0 mA, V_{DD} = 3.6 to 5.5 V	V_{OL2}			0.2V_{DD}	V
Tout0 to Tout4 pins Output Low-level Voltage	I_O = +1.5 mA	V_{OL3}			0.2V_{DD}	V
SDA pin Output Low-level Voltage	I_O = +3.0 mA	V_{OL4}			0.4	V
Input High-level Current (Note 14)	V_I = V_{DD}	I_{IH}			1.0	μA
Input Low-level Current (Note 14)	V_I = V_{SS}	I_{IL}	−1.0			μA
Output Off Leakage Current (Note 15)	V_I = V_{DD} or V_I = V_{SS}	I_{OFF}	−1.0		1.0	μA
Current Consumption	Initial setting, Long interval operation, Sensor pins are open (Note 16), V_{DD} = 5.5 V	I_{DD1}		0.8	2.2	mA
	Initial setting, Short interval operation, Sensor pins are open (Note 16), V_{DD} = 5.5 V	I_{DD2}		3.25	6.5	mA
	Sleep mode (Sleep period) Sensor pins are open (Note 16)	I_{STBY}		0.1	70	μA
Capacitance Sensor Function						
Cin Detection Sensitivity	Measurements conducted using the test mode in the LSI, Minimum gain setting	Cin_{SENSE}	0.0476	0.068	0.0884	LSB/fF
Sensor Pin Leakage Current (Note 17)	V_I = V_{DD} or V_I = V_{SS}	I_{Cin}		±25	±500	nA
Cdrv Drive Frequency	With 121 kHz setting	f_{CDRV}	84.85	121.21	157.57	kHz
Power-on Reset Function						
nRST Minimum Pulse Width		t_{NRST}	1.0			μs
Power-on Reset Time		t_{POR}			20	ms
Power-on Reset Operation Condition: Hold Time		t_{POROP}	10			ms
Power-on Reset Operation Condition: Input Voltage		V_{POROP}			0.1	V
Power-on Reset Operation Condition: Power Supply Rise Rate	0 V to V_{DD}	t_{VDD}	1.0			V/ms
Interval Operation Timing						
Long Interval Time	V_{DD} = 2.6 to 4.5 V, Long interval mode (Long interval time is set to 101 ms)	T_{LIVAL1}	35	101	145	ms
	V_{DD} = 4.5 to 5.5 V, Long interval mode (Long interval time is set to 101 ms)	T_{LIVAL2}	40	101	125	ms
Short Interval Time	V_{DD} = 2.6 to 4.5 V, Short interval mode (Short interval time is set to 5 ms)	T_{SIVAL1}	1.7	5	7.3	ms
	V_{DD} = 4.5 to 5.5 V, Short interval mode (Short interval time is set to 5 ms)	T_{SIVAL2}	1.9	5	6.3	ms

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ELECTRICAL CHARACTERICALS (CONTINUED) at V_{DD} = 2.6 to 5.5 V, V_{SS} = 0 V, T_A = −40 to + 105°C, (Note 12)
Unless otherwise specified, the Cdrv drive frequency is f_{CDRV} = 121 kHz.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
I^2C Compatible Bus Interface Timing						
SCL Clock Frequency	SCL	f_{SCL}			400	kHz
START Condition Hold Time	SCL, SDA	$t_{HD; STA}$	0.6			μs
SCL Clock Low Period	SCL	t_{LOW}	1.3			μs
SCL Clock High Period	SCL	t_{HIGH}	0.6			μs
Repeated START Condition Setup Time	SCL, SDA	$t_{SU; STA}$	0.6			μs
Data Hold Time	SCL, SDA	$t_{HD; DAT}$	0		0.9	μs
Data Setup Time	SCL, SDA	$t_{SU; DAT}$	0.5			μs
SDA, SCL Rise/Fall Time	SCL, SDA	t_r/t_f			0.3	μs
STOP Condition Setup Time	SCL, SDA	$t_{SU; STO}$	0.6			μs
STOP-to-START Bus Release Time	SCL, SDA	t_{BUF}	2.5			μs
SPI Interface Timing						
SCK Clock Frequency	SCK	f_{SCK}			5.0	MHz
SCK Clock Low Time	SCK	t_{LOW}	100			ns
SCK Clock High Time	SCK	t_{HIGH}	100			ns
Input Signal Rise/Fall Time	nCS, SCK, SI	t_r/t_f			300	ns
nCS Setup Time	nCS, SCK	$t_{SU; NCS}$	200			ns
SCK Clock Setup Time	nCS, SCK	$t_{SU; SCK}$	100			ns
Data Setup Time	SCK, SI	$t_{SU; SI}$	100			ns
Data Hold Time	SCK, SI	$t_{HD; SI}$	100			ns
nCS Hold Time	nCS, SCK	$t_{HD; NCS}$	200			ns
SCK Clock Hold Time	nCS, SCK	$t_{HD;SCK}$	700			ns
nCS Standby Pulse Width	nCS	t_{CPH}	300			ns
Output High Impedance Time from nCS	nCS, SO	t_{CHZ}			100	ns
Output Data Determination Time	SCK, SO	t_V			100	ns
Output Data Hold Time	SCK, SO	$t_{HD; SO}$	0			ns
Output Low Impedance Time from SCK Clock	SCK, SO	t_{CLZ}	100			ns

Note 12 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
13 : Apply to Cdrv, CdrvBar, SO, INTOUT.
14 : Apply to SCL/SCK, SDA/SI, SA0, nCS, nRST, IFSEL.
15 : Apply to Cdrv, CdrvBar, SDA, SO.
16 : Sensor pins (Cin0 to Cin7, CMAdd0, CMAdd4, Cref, CrefAdd) are open condition.
17 : Apply to Cin0 to Cin7, CMAdd0, CMAdd4, Cref, CrefAdd.

FUNCTIONAL DESCRIPTION

Power-on Reset (POR)

When power is turned on, power-on reset is enabled, it is released after power-on reset time, t_{POR}. Power-on reset operation condition; Power supply rise rate t_{VDD} must be at least 1.0 V/ms.

.

Since INTOUT pin changes from “High” to “Low” at the same time as reset release, it is possible to verify the timing of release of reset externally. During power-on reset, Cin0 to Cin7, CMAdd0, CMAdd4, Cref, CrefAdd, and CdrvBar are unknown.

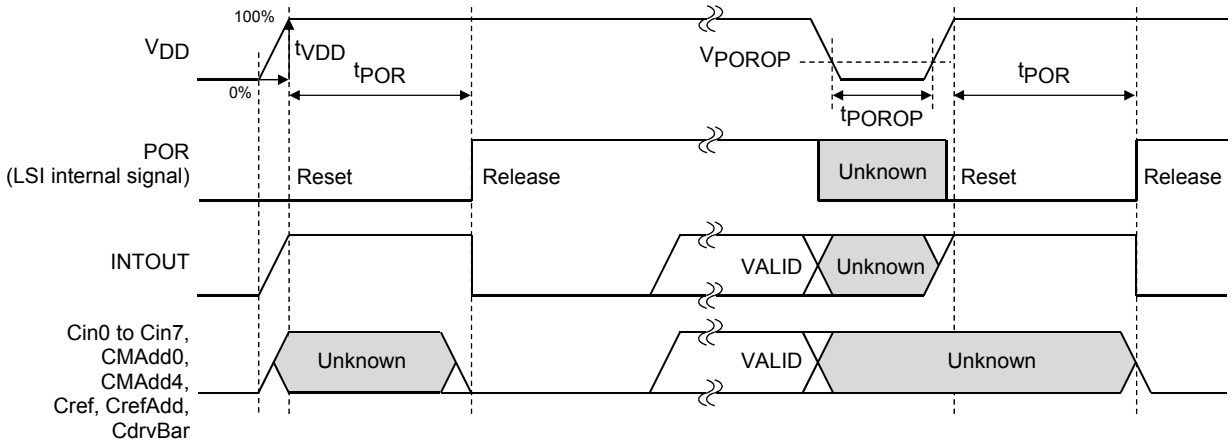


Figure 6. Power-on Sequence by the Power-on Reset

External Reset (nRST)

Reset State nRST = “Low”. Pins Cin0 to Cin7, CMAdd0, CMAdd4, Cref, CrefAdd and CdrvBar, are “Hi-Z” during reset state. The reset state is released after t_{POR}.

Since INTOUT pin changes from “High” to “Low” at the same time as the released of reset, it is possible to verify the timing of release of reset externally.

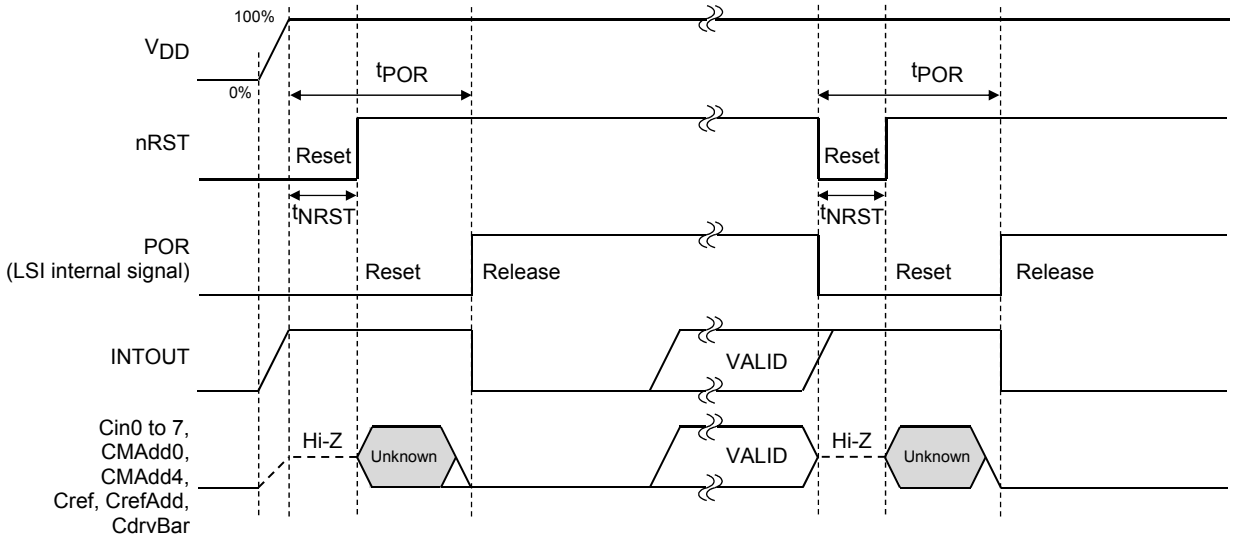


Figure 7. Power-on Sequence by the External Reset

I²C Data Timing

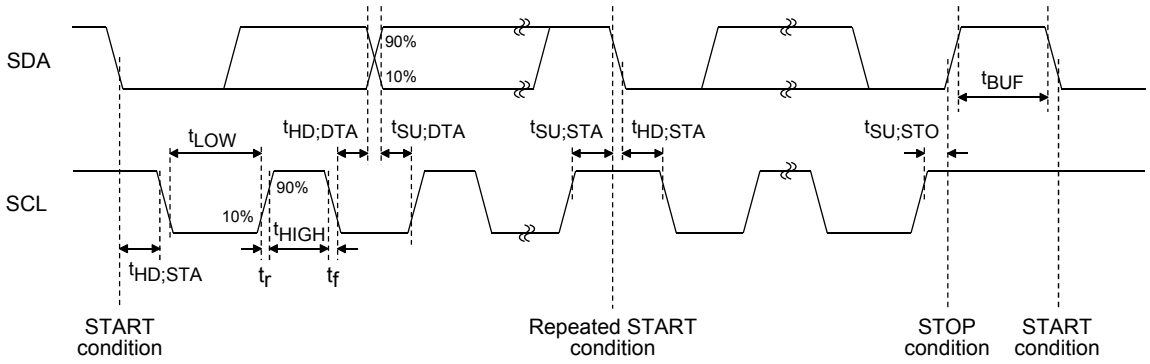


Figure 8. I²C Data Timing

I²C Communication Formats

Write Format

When using the Write format of I²C the data can be written into sequentially incremented addresses.

Figure 9. I²C Write Format

Read Format

When using the Read format of I²C the data can be read from sequentially incremented addresses.

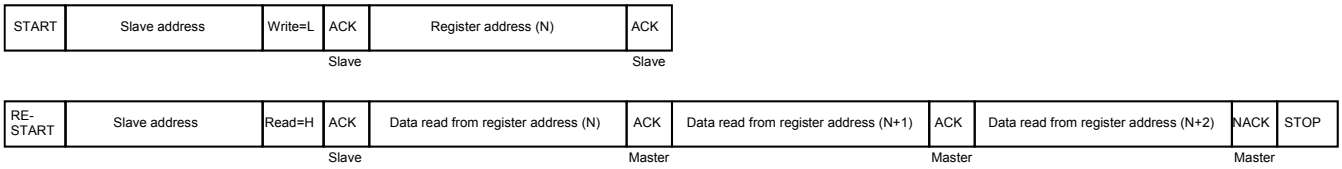


Figure 10. I²C Read Format

I²C Slave Address

SA0 pin is used to select the slave address

Table 1. I²C Slave Address

SA0 pin input	7 bit slave address	Binary notation	8 bit slave address
Low	0x16	00101100b (Write)	0x2C
		00101101b (Read)	0x2D
High	0x17	00101110b (Write)	0x2E
		00101111b (Read)	0x2F

SPI Data Timing (Mode 0 / Mode 3)

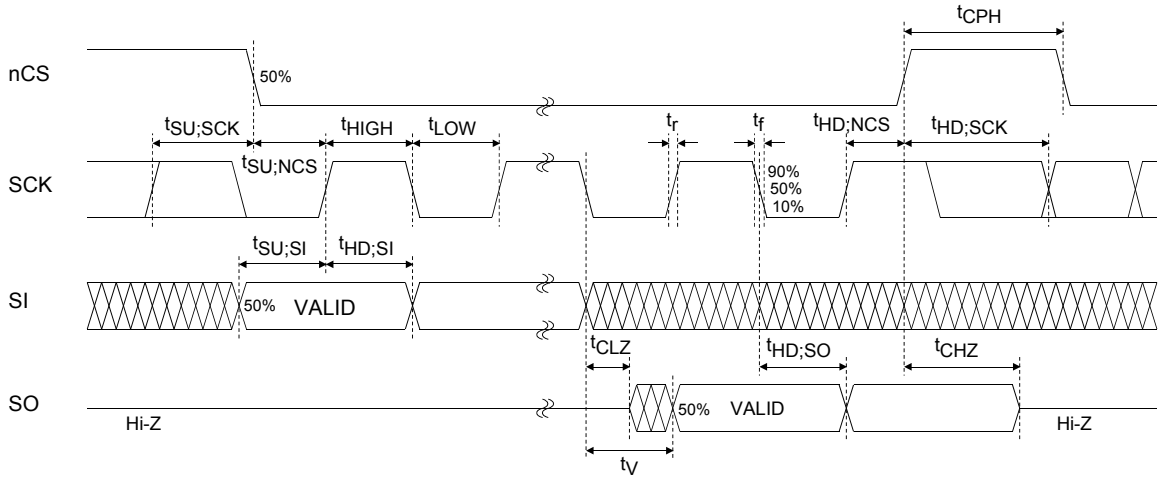


Figure 11. SPI Data Timing

SPI write Format (Example of Mode 0)

When using the SPI Write format the data can be written into sequentially incremented addresses with preserving nCS = "L".

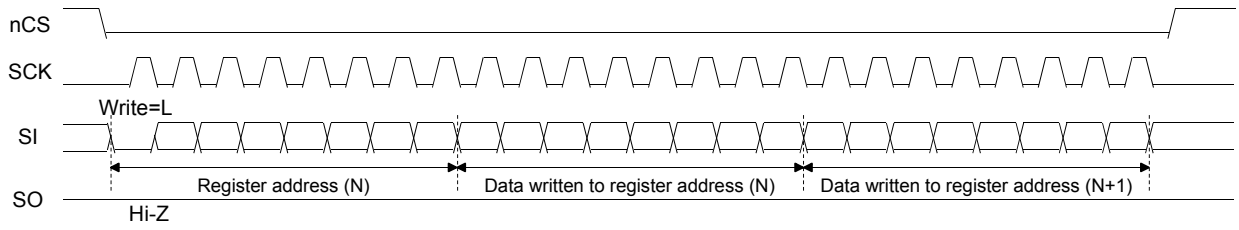


Figure 12. SPI Write Format

SPI Read Format

When using the SPI Read format the data can be read from sequentially incremented addresses with preserving nCS = "L".

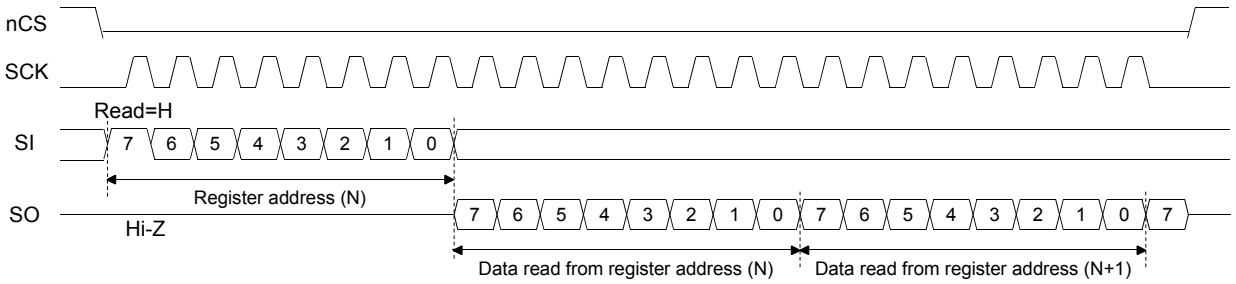
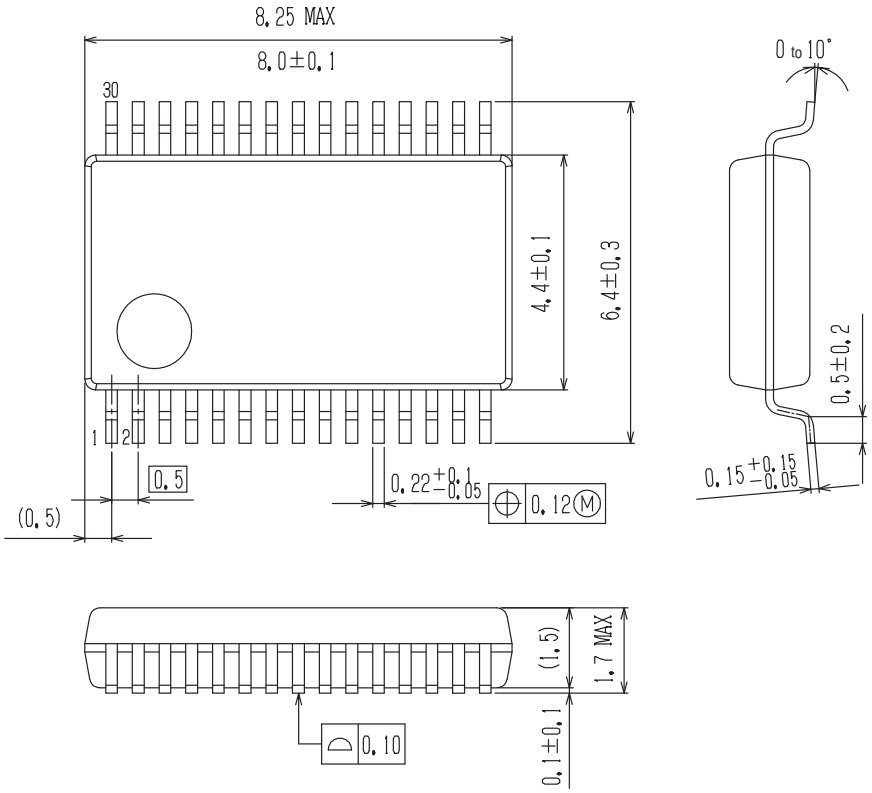


Figure 13. SPI Read Format

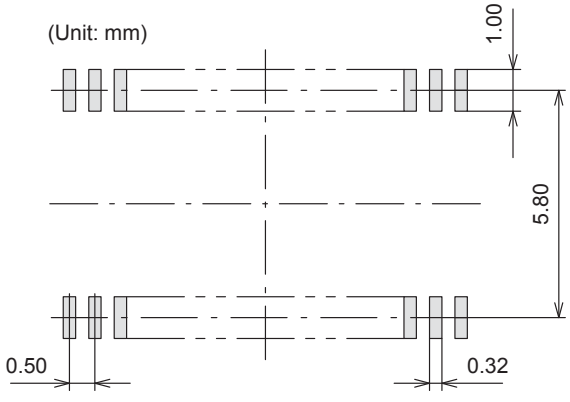
PACKAGE DIMENSIONS

unit : mm

SSOP30 (225 mil)
CASE 565AZ
ISSUE A



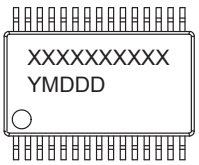
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

* I^2C Bus is a trademark of Philips Corporation.