

Preliminary Data

HiPerFET™ Power MOSFET

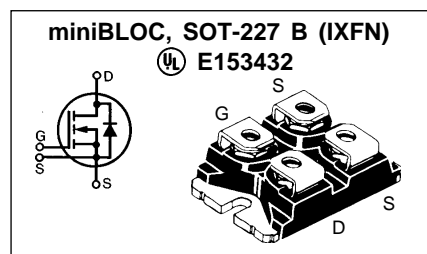
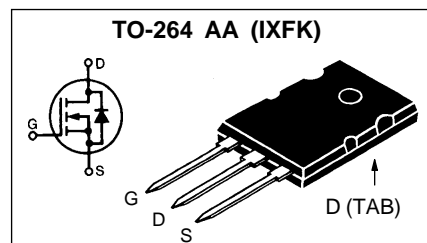
N-Channel Enhancement Mode

Avalanche Rated, High dv/dt, Low t_{rr}

	V_{DSS}	I_{D25}	$R_{DS(on)}$	t_{rr}
IXFK/FN 36N60	600V	36A	0.18Ω	250ns
IXFK/FN 32N60	600V	32A	0.25Ω	250ns

Symbol	Test Conditions	Maximum Ratings			
		IXFK	IXFN		
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	600	600		V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1\text{ M}\Omega$	600	600		V
V_{GS}	Continuous	±20	±20		V
V_{GSM}	Transient	±30	±30		V
I_{D25}	$T_C = 25^\circ\text{C}$, Chip capability	32N60	32	32	A
		36N60	36	36	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	32N60	128	128	A
		36N60	144	144	A
I_{AR}	$T_C = 25^\circ\text{C}$	20	20		A
E_{AR}	$T_C = 25^\circ\text{C}$	30	30		mJ
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$ $T_J \leq 150^\circ\text{C}$, $R_G = 2\ \Omega$	5	5		V/ns
P_D	$T_C = 25^\circ\text{C}$	500	520		W
T_J		-55 ...	+150		$^\circ\text{C}$
T_{JM}			150		$^\circ\text{C}$
T_{stg}		-55 ...	+150		$^\circ\text{C}$
T_L	1.6 mm (0.063 in) from case for 10 s	300	-		$^\circ\text{C}$
V_{ISOL}	50/60 Hz, RMSt = 1 min $I_{ISOL} \leq 1\text{ mA}$ at 1 s	-	2500		V~
		-	3000		V~
M_d	Mounting torque	0.9/6	1.5/13		Nm/lb.in.
	Terminal connection torque	-	1.5/13		Nm/lb.in.
Weight		10	30		g

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		Min.	Typ.	Max.
V_{DSS}	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600		V
$V_{GH(th)}$	$V_{DS} = V_{GS}$, $I_D = 8\text{ mA}$	2		4.5 V
I_{GSS}	$V_{GS} = \pm 20\text{ V}_{DC}$, $V_{DS} = 0$			±200 nA
I_{DSS}	$V_{DS} = 0.8\text{ V}_{DSS}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$			400 μA
				2 mA
$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 0.5\text{ I}_{D25}$ Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$	36N60		0.18 Ω
		32N60		0.25 Ω



G = Gate D = Drain
S = Source TAB = Drain
Either Source terminal at miniBLOC
can be used as Main or Kelvin Source

Features

- International standard packages
- JEDEC TO-264 AA, epoxy meet UL 94 V-0, flammability classification
- miniBLOC with Aluminium nitride isolation
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls
- Low voltage relays

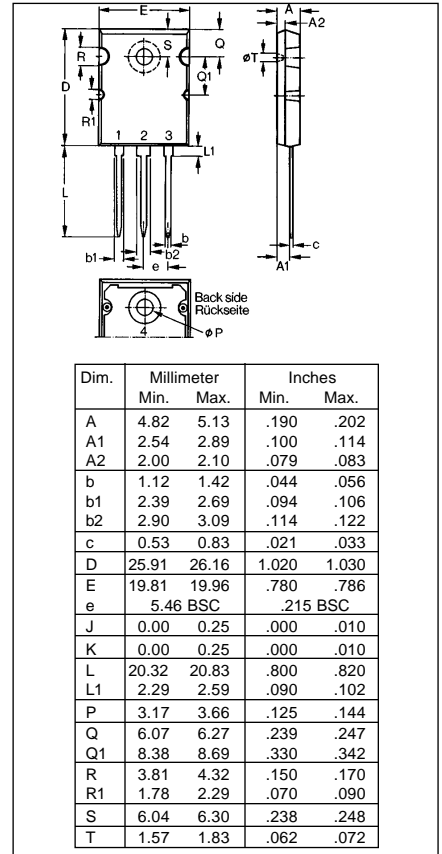
Advantages

- Easy to mount
- Space savings
- High power density

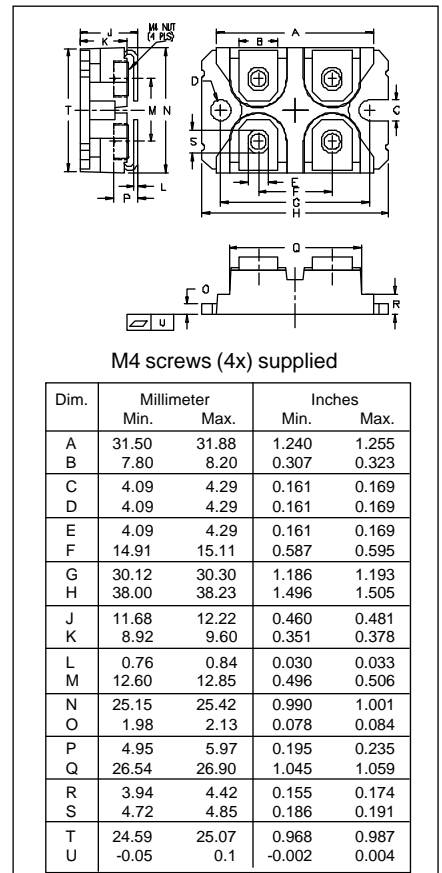
Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	V _{DS} = 10 V; I _D = 0.5 I _{D25} ; pulse test		36	S
C_{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		9000	pF
C_{oss}			840	pF
C_{rss}			280	pF
t_{d(on)}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} ; I _D = 0.5 I _{D25} R _G = 1 Ω (External),		30	ns
t_r			45	ns
t_{d(off)}			100	ns
t_f			60	ns
Q_{g(on)}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} ; I _D = 0.5 I _{D25}		325	nC
Q_{gs}			60	nC
Q_{gd}			120	nC
R_{thJC}	TO-264 AA		0.25	K/W
R_{thCK}	TO-264 AA		0.15	K/W
R_{thJC}	miniBLOC, SOT-227 B		0.24	K/W
R_{thCK}	miniBLOC, SOT-227 B		0.05	K/W

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C, unless otherwise specified)		
		Min.	Typ.	Max.
I_S	V _{GS} = 0	36N60		36 A
I_S	V _{GS} = 0	32N60		32 A
I_{SM}	Repetitive; pulse width limited by T _{JM}	36N60		144 A
		32N60		128 A
V_{SD}	I _F = I _S A, V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			1.5 V
t_{rr}	I _F = I _S , -di/dt = 100 A/μs, V _R = 100 V		20	ns
I_{RM}				

TO-264 AA Outline



miniBLOC, SOT-227 B



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715
4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025

Fig.1. Output Characteristics

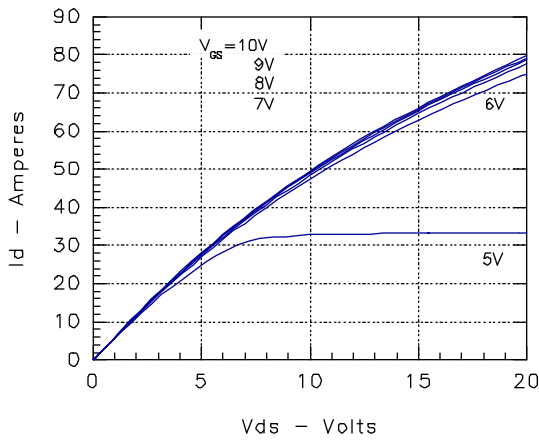


Fig. 2. Input Admittance

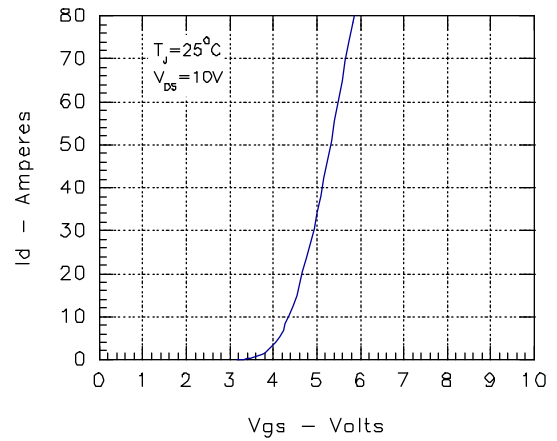


Fig. 3. Rds(on) vs. Drain Current

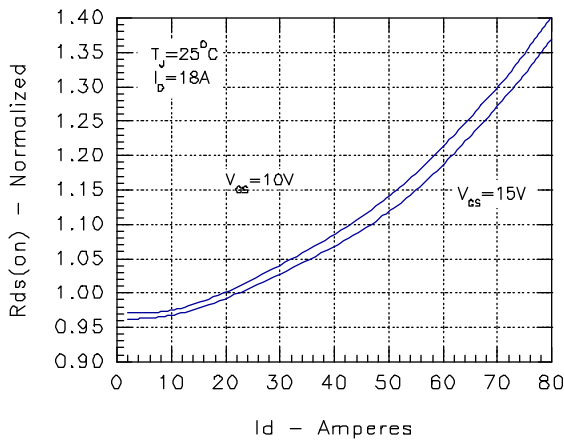


Fig. 4. Temperature Dependence of Drain to Source Resistance

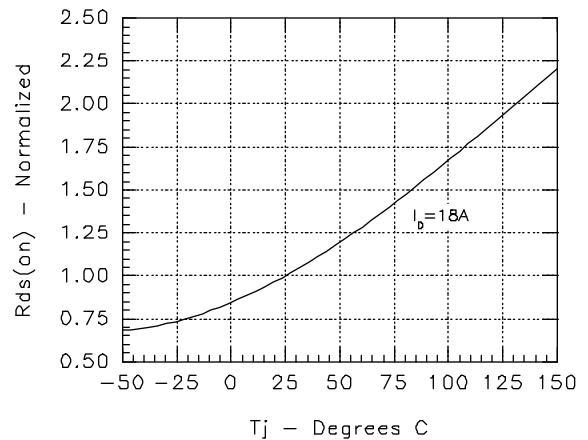


Fig. 5. Drain Current vs. Case Temperature

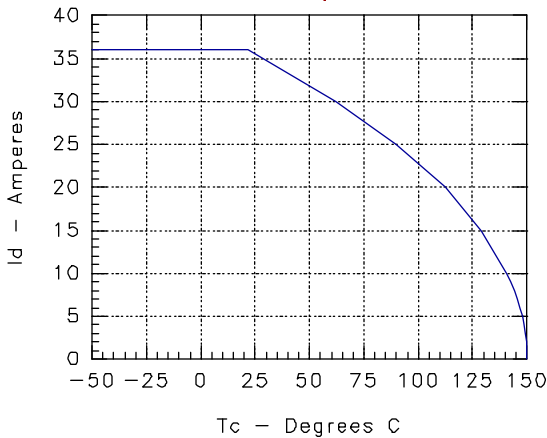
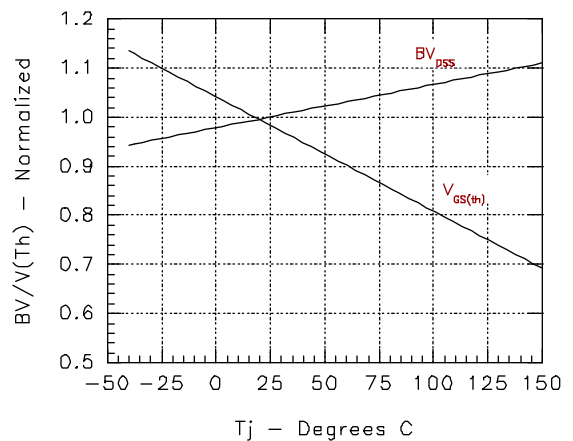


Fig. 6. Temperature Dependence of Breakdown Voltage and Threshold Voltage



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Fig. 7. Gate Charge

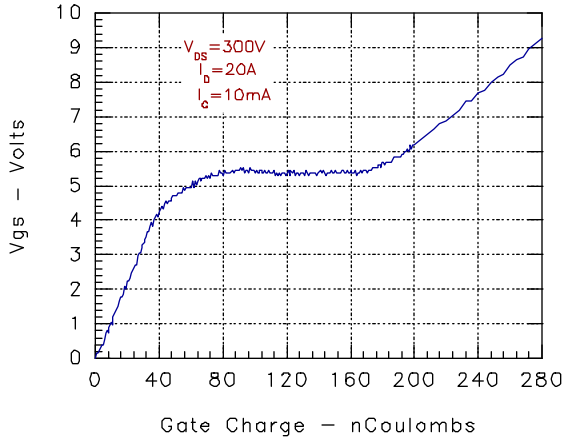


Fig. 8. Capacitance Curves

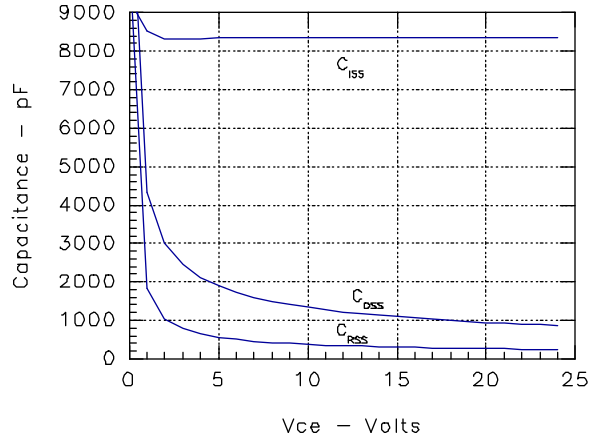


Fig. 9. Source Current vs. Source to Drain Voltage

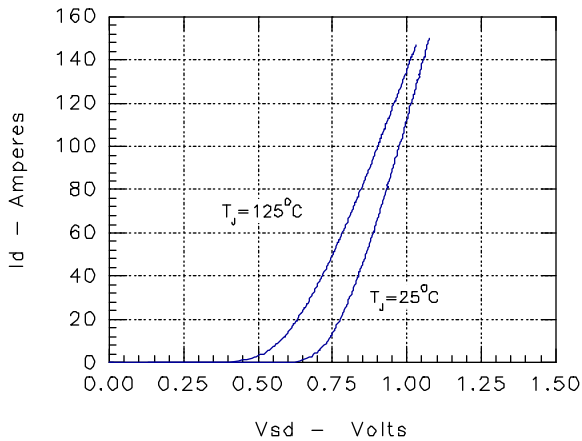
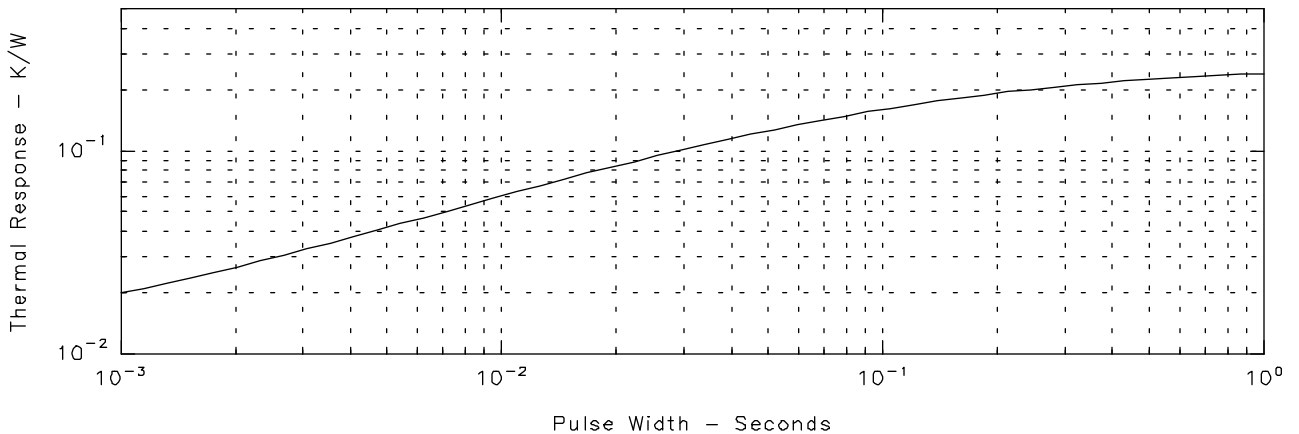


Fig. 10. Transient Thermal Impedance



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