

FEATURES

- 8.0 GHz bandwidth**
- 3.2 V to 3.6 V power supply**
- Separate charge pump supply (V_P) allows extended tuning voltage in 3.3 V systems**
- Programmable, dual-modulus prescaler**
8/9, 16/17, 32/33, or 64/65
- Programmable charge pump currents**
- Programmable antibacklash pulse width**
- 3-wire serial interface**
- Analog and digital lock detect**
- Hardware and software power-down mode**
- Loop filter design possible with ADIsimPLL**
- 4 mm × 4 mm, 20-lead chip scale package**

APPLICATIONS

- Broadband wireless access**
- Satellite systems**
- Instrumentation**
- Wireless LANs**
- Base stations for wireless radio**

GENERAL DESCRIPTION

The ADF4108 frequency synthesizer can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler ($P/P + 1$). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler ($P/P + 1$), implement an N divider ($N = BP + A$). In addition, the 14-bit reference counter (R counter), allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). Its very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

FUNCTIONAL BLOCK DIAGRAM

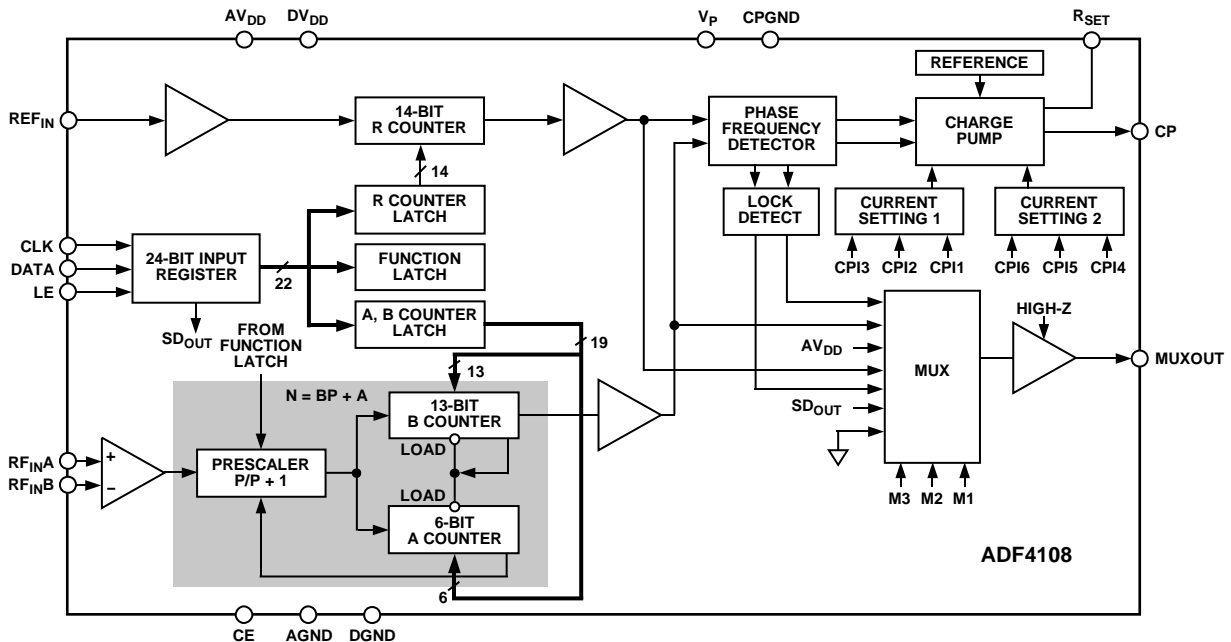


Figure 1.

06015-001

Rev. E

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF4108 Evaluation Board

DOCUMENTATION

Application Notes

- AN-30: Ask the Applications Engineer - PLL Synthesizers
- AN-349: Keys to Longer Life for CMOS
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers

Data Sheet

- ADF4108: PLL Frequency Synthesizer Data Sheet

User Guides

- UG-160: Evaluation Board for Integer-N PLL Frequency Synthesizer
- UG-476: PLL Software Installation Guide

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADF4108 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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REVISION HISTORY

4/13—Rev. D to Rev. E

Changed RF_{INA} to RF_{INB} Parameter from ± 320 mV to ± 600 mV, Table 3

1/13—Rev. C to Rev. D

Change to Table 1

Added RF_{INA} to RF_{INB} Parameter, Table 4.....

7/12—Rev. B to Rev. C

Changes to Figure 3.....

Updated Outline Dimensions (Changed CP-20-1 to CP-20-6).....

Changes to Ordering Guide

9/11—Rev. A to Rev. B

Changes to Normalized Phase Noise Floor (PN_{SYNTH}) Parameter and Endnote 9, Table 1.....

Added Normalized $1/f$ Noise ($PN_{1/f}$) Parameter and Endnote 10, Table 1

Changes to Figure 3 and Table 4.....

Updated Outline Dimensions

12/07—Rev. 0 to Rev. A

Removed TSSOP Package

Changes to Features

Changes to Table 1 Endnote 10 and Endnote 11.....

Changes to Table 3.....

Deleted Figure 3.....

Changes to Table 4.....

Changes to Figure 10 and Figure 11.....

Updated Outline Dimensions

Deleted Figure 24.....

Changes to Ordering Guide

4/06—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD} = DV_{DD} = 3.3 \text{ V} \pm 2\%$, $AV_{DD} \leq V_P \leq 5.5 \text{ V}$, $AGND = DGND = CPGND = 0 \text{ V}$, $R_{SET} = 5.1 \text{ k}\Omega$, dBm referred to 50Ω , $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	B Version ¹	B Chips ² (Typ)	Unit	Test Conditions/Comments
RF CHARACTERISTICS				
RF Input Frequency (RF_{IN})	1.0/8.0	1.0/8.0	GHz min/max	See Figure 11 for input circuit
RF Input Sensitivity	-5/+5	-5/+5	dBm min/max	For lower frequencies, ensure slew rate (SR) > 320 V/ μ s
Maximum Allowable Prescaler Output Frequency ³	300	300	MHz max	P = 8
	325	325	MHz max	P = 16
REF_{IN} CHARACTERISTICS				
REF _{IN} Input Frequency	20/250	20/250	MHz min/max	For f < 20 MHz, ensure SR > 50 V/ μ s
REF _{IN} Input Sensitivity ⁴	0.8/ V_{DD}	0.8/ V_{DD}	V p-p min/max	Biased at $AV_{DD}/2^5$
REF _{IN} Input Capacitance	10	10	pF max	
REF _{IN} Input Current	± 100	± 100	μ A max	
PHASE DETECTOR				
Phase Detector Frequency ⁶	104	104	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				Programmable; see Figure 18
High Value	5	5	mA typ	With $R_{SET} = 5.1 \text{ k}\Omega$
Low Value	625	625	μ A typ	
Absolute Accuracy	2.5	2.5	% typ	With $R_{SET} = 5.1 \text{ k}\Omega$
R_{SET} Range	3.0/11	3.0/11	k Ω typ	See Figure 18
I_{CP} Three-State Leakage	1	1	nA typ	1 nA typical; $T_A = 25^\circ\text{C}$
Sink and Source Current Matching	2	2	% typ	$0.5 \text{ V} \leq V_{CP} \leq V_P - 0.5 \text{ V}$
I_{CP} vs. V_{CP}	1.5	1.5	% typ	$0.5 \text{ V} \leq V_{CP} \leq V_P - 0.5 \text{ V}$
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{IH} , Input High Voltage	1.4	1.4	V min	
V_{IL} , Input Low Voltage	0.6	0.6	V max	
I_{INH} , I_{INL} , Input Current	± 1	± 1	μ A max	
C_{IN} , Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH} , Output High Voltage	1.4	1.4	V min	Open-drain output chosen; 1 k Ω pull-up resistor to 1.8 V
V_{OH} , Output High Voltage	$V_{DD} - 0.4$	$V_{DD} - 0.4$	V min	CMOS output chosen
I_{OH} , Output High Current	100	100	μ A max	
V_{OL} , Output Low Voltage	0.4	0.4	V max	$I_{OL} = 500 \mu\text{A}$
POWER SUPPLIES				
AV_{DD}	3.2/3.6	3.2/3.6	V min/max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	$AV_{DD}/5.5$	$AV_{DD}/5.5$	V min/max	$AV_{DD} \leq V_P \leq 5.5 \text{ V}$
I_{DD} ($AI_{DD} + DI_{DD}$) ⁷	17	17	mA max	15 mA typ
I_P	0.4	0.4	mA max	$T_A = 25^\circ\text{C}$
Power-Down Mode ($AI_{DD} + DI_{DD}$) ⁸	10	10	μ A typ	

Parameter	B Version ¹	B Chips ² (Typ)	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS				
Normalized Phase Noise Floor (PN _{SYNTH}) ⁹	-223	-223	dBc/Hz typ	PLL loop B/W = 500 kHz, measured at 100 kHz offset
Normalized 1/f Noise (PN _{1-f}) ¹⁰	-122	-122	dBc/Hz typ	10 kHz offset; normalized to 1 GHz
Phase Noise Performance ¹¹ 7900 MHz Output ¹²	-81	-81	dBc/Hz typ	@ VCO output @ 1 kHz offset and 1 MHz PFD frequency
Spurious Signals 7900 MHz Output ¹²	-82	-82	dBc typ	@ 1 MHz offset and 1 MHz PFD frequency

¹ Operating temperature range (B version) is -40°C to +85°C.

² The B chip specifications are given as typical values.

³ This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.

⁴ AV_{DD} = DV_{DD} = 3.3 V.

⁵ AC coupling ensures AV_{DD}/2 bias.

⁶ Guaranteed by design. Sample tested to ensure compliance.

⁷ T_A = 25°C; AV_{DD} = DV_{DD} = 3.3 V; P = 32; RF_{IN} = 8 GHz; f_{PFD} = 200 kHz; REF_{IN} = 10 MHz.

⁸ T_A = 25°C; AV_{DD} = DV_{DD} = 3.3 V; R = 16,383; A = 63; B = 891; P = 32; RF_{IN} = 7.0 GHz.

⁹ The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. PN_{SYNTH} = PN_{ROT} - 10 log F_{PFD} - 20 log N.

¹⁰ The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset, f, is given by PN = PN_{1-f} + 10 log(10 kHz/f) + 20 log(f_{RF}/1 GHz). All phase noise measurements were performed with the [EV-ADF4108EBZ1](#) and the Agilent E5500 phase noise system. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.

¹¹ The phase noise is measured with the [EV-ADF4108EB1Z](#) evaluation board, with the ZComm CRO8000Z VCO. The spectrum analyzer provides the REF_{IN} for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).

¹² f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; f_{RF} = 7900 MHz; N = 7900; loop B/W = 30 kHz, VCO = ZComm CRO8000Z.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = 3.3\text{ V} \pm 2\%$, $AV_{DD} \leq V_P \leq 5.5\text{ V}$, $AGND = DGND = CPGND = 0\text{ V}$, $R_{SET} = 5.1\text{ k}\Omega$, dBm referred to $50\ \Omega$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 2.

Parameter ¹	Limit ² (B Version)	Unit	Test Conditions/Comments
t ₁	10	ns min	DATA to CLOCK setup time
t ₂	10	ns min	DATA to CLOCK hold time
t ₃	25	ns min	CLOCK high duration
t ₄	25	ns min	CLOCK low duration
t ₅	10	ns min	CLOCK to LE setup time
t ₆	20	ns min	LE pulse width

¹ Guaranteed by design but not production tested.

² Operating temperature range (B Version) is -40°C to $+85^\circ\text{C}$.

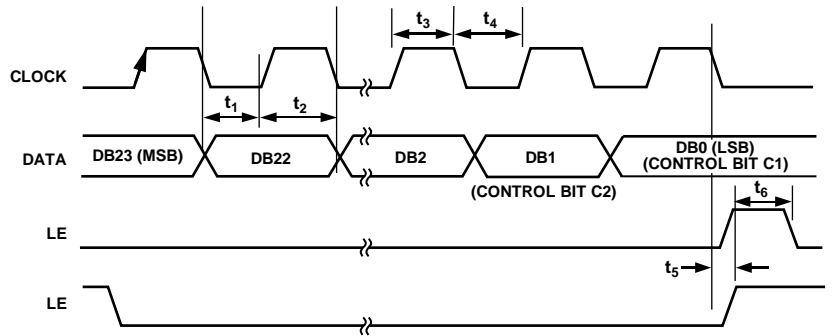


Figure 2. Timing Diagram

06015-002

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND ¹	-0.3 V to +3.9 V
AV_{DD} to DV_{DD}	-0.3 V to +0.3 V
V_P to GND	-0.3 V to +5.8 V
V_P to AV_{DD}	-0.3 V to +5.8 V
Digital I/O Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
Analog I/O Voltage to GND	-0.3 V to $V_P + 0.3$ V
REF_{IN} , $RF_{IN A}$, $RF_{IN B}$ to GND	-0.3 V to $V_{DD} + 0.3$ V
$RF_{IN A}$ to $RF_{IN B}$	± 600 mV
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C
Maximum Junction Temperature	150°C
CSP θ_{JA} Thermal Impedance (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature (60 sec)	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	6425
Bipolar	303

¹ GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

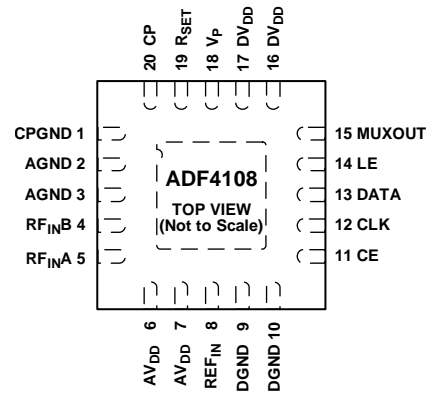
This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO AGND.

06015-003

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
4	RFINB	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 11.
5	RFINA	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
6, 7	AVDD	Analog Power Supply. This voltage may range from 3.2 V to 3.6 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AVDD must be the same value as DVDD.
8	REFIN	Reference Input. This is a CMOS input with a nominal threshold of VDD/2 and a dc equivalent input resistance of 100 kΩ. See Figure 10. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9, 10	DGND	Digital Ground.
11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, F2.
12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
13	DATA	Serial Data Input. The serial data is loaded MSB first with the 2 LSBs being the control bits. This input is a high impedance CMOS input.
14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
16, 17	DVDD	Digital Power Supply. This may range from 3.2 V to 3.6 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DVDD must be the same value as AVDD.
18	VP	Charge Pump Power Supply. This voltage should be greater than or equal to VDD. In systems where VDD is 3.3 V, it can be set to 5 V and used to drive a VCO with a tuning range of up to 5 V.
19	RSET	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the RSET pin is 0.66 V. The relationship between ICP and RSET is $I_{CP\ MAX} = \frac{25.5}{R_{SET}}$ with RSET = 5.1 kΩ, ICP MAX = 5 mA.
20	CP	Charge Pump Output. When enabled, this pin provides ±ICP to the external loop filter, which in turn drives the external VCO.
	EP	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ UNIT: GHz KEYWORD: R			FREQ UNIT: GHz KEYWORD: R		
PARAM TYPE: s			PARAM TYPE: s		
DATA FORMAT: MA			DATA FORMAT: MA		
Freq	MAGS11	ANGS11	Freq	MAGS11	ANGS11
0.50000	0.89148	-17.2820	4.30000	0.45555	-159.890
0.60000	0.88133	-20.6919	4.40000	0.46108	-164.916
0.70000	0.87152	-24.5386	4.50000	0.45325	-168.452
0.80000	0.85855	-27.3228	4.60000	0.45054	-173.462
0.90000	0.84911	-31.0638	4.70000	0.45200	-176.697
1.00000	0.83512	-34.8623	4.80000	0.45043	-178.824
1.10000	0.82374	-38.5574	4.90000	0.45282	-174.947
1.20000	0.80871	-41.9093	5.00000	0.44237	-170.237
1.30000	0.79176	-45.6990	5.10000	0.44909	-166.617
1.40000	0.77205	-49.4185	5.20000	0.44294	-162.786
1.50000	0.75696	-52.8898	5.30000	0.44558	-158.766
1.60000	0.74234	-56.2923	5.40000	0.45417	-153.195
1.70000	0.72239	-60.2384	5.50000	0.46038	-147.721
1.80000	0.69419	-63.1446	5.60000	0.47128	-139.750
1.90000	0.67288	-65.6464	5.70000	0.47439	-132.657
2.00000	0.66227	-68.0742	5.80000	0.48604	-125.782
2.10000	0.64758	-71.3530	5.90000	0.50637	-121.110
2.20000	0.62454	-75.5658	6.00000	0.52172	-115.400
2.30000	0.59466	-79.6404	6.10000	0.53342	-107.705
2.40000	0.55932	-82.8246	6.20000	0.53716	-101.572
2.50000	0.52256	-85.2795	6.30000	0.55804	-97.5379
2.60000	0.48754	-85.6298	6.40000	0.56362	-93.9936
2.70000	0.46411	-86.1854	6.50000	0.58268	-89.2227
2.80000	0.45776	-86.4997	6.60000	0.59248	-86.3300
2.90000	0.44859	-86.8080	6.70000	0.61066	-83.0956
3.00000	0.44588	-87.9737	6.80000	0.61830	-80.8843
3.10000	0.43810	-95.4087	6.90000	0.61633	-78.0872
3.20000	0.43369	-99.1282	7.00000	0.61873	-75.3727
3.30000	0.42777	-102.748	7.10000	0.60597	-73.9456
3.40000	0.42859	-107.167	7.20000	0.58376	-73.5883
3.50000	0.43365	-111.883	7.30000	0.57873	-74.1975
3.60000	0.43849	-117.548	7.40000	0.58157	-76.2136
3.70000	0.44475	-123.856	7.50000	0.60040	-77.1545
3.80000	0.44800	-130.399	7.60000	0.61332	-76.1122
3.90000	0.45223	-136.744	7.70000	0.62927	-74.8359
4.00000	0.45555	-142.766	7.80000	0.63938	-74.0546
4.10000	0.45313	-149.259	7.90000	0.65320	-72.0061
4.20000	0.45622	-154.884	8.00000	0.65804	-69.9926

Figure 4. S Parameter Data for the RF Input

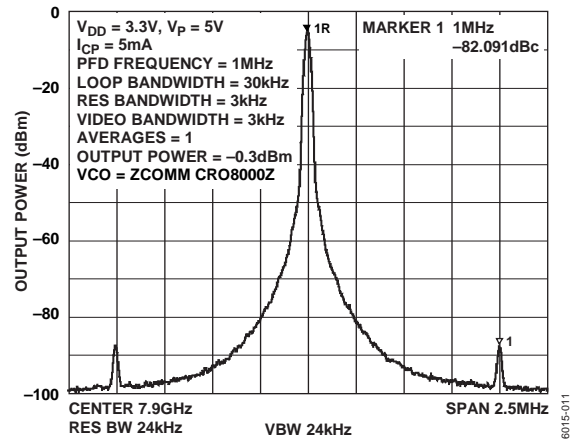


Figure 7. Reference Spurs at 7.9 GHz

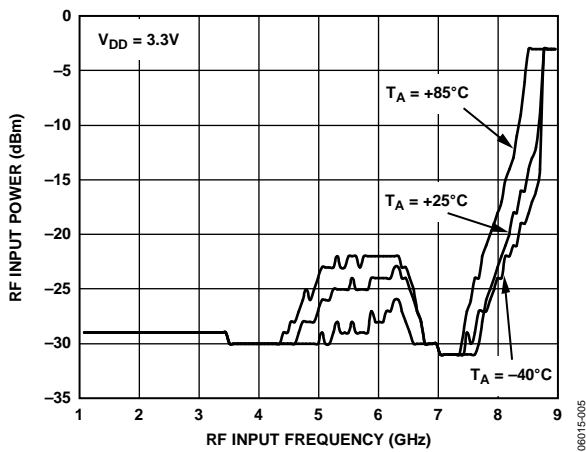


Figure 5. RF Input Sensitivity

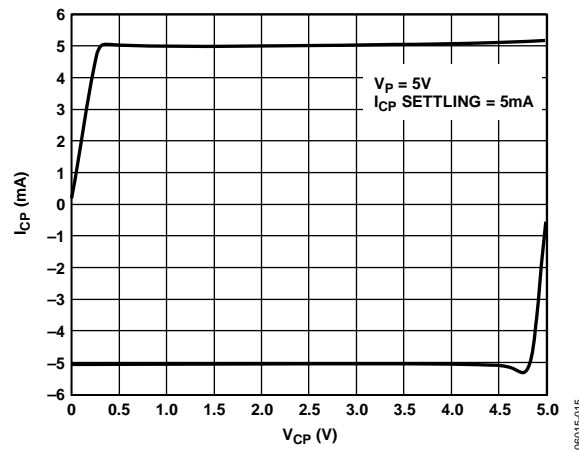


Figure 8. Charge Pump Output Characteristics

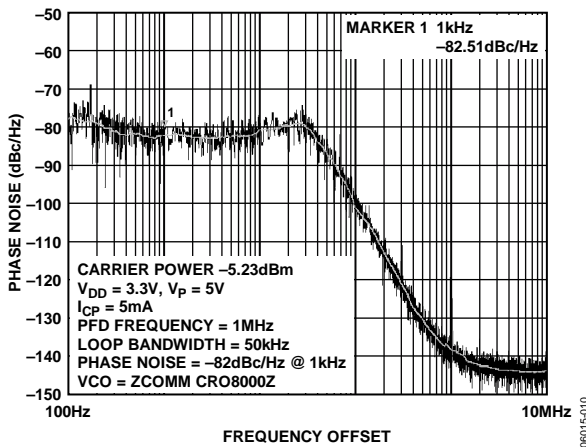


Figure 6. Phase Noise at 7.9 GHz

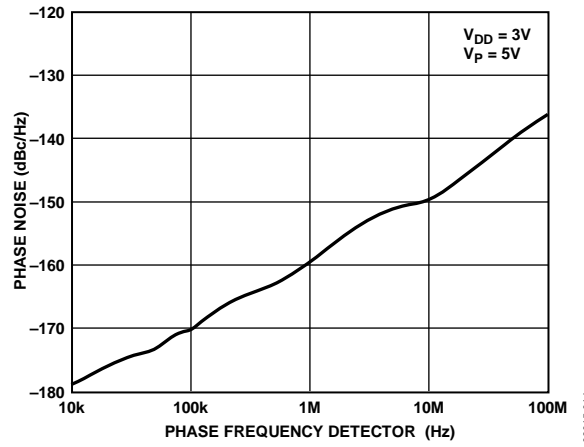


Figure 9. Phase Noise (Referred to CP Output) vs. PFD Frequency

THEORY OF OPERATION

REFERENCE INPUT STAGE

The reference input stage is shown in Figure 10. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

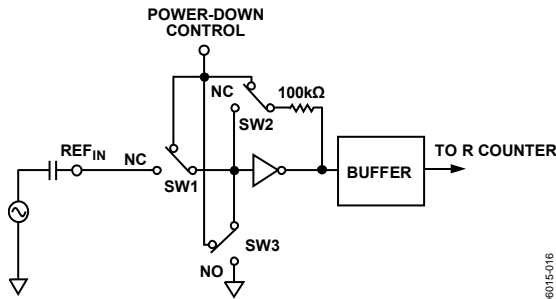


Figure 10. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 11. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

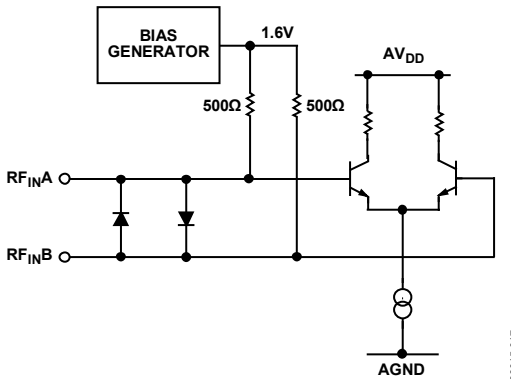


Figure 11. RF Input Stage

PRESCALER (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. A minimum divide ratio is possible for contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by (P² - P).

A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times \frac{f_{REFIN}}{R}$$

where:

f_{VCO} is the output frequency of external voltage controlled oscillator (VCO).

P is the preset modulus of dual-modulus prescaler (8/9, 16/17, and so on.).

B is the preset divide ratio of binary 13-bit counter (3 to 8191). A is the preset divide ratio of binary 6-bit swallow counter (0 to 63).

f_{REFIN} is the external reference frequency oscillator.

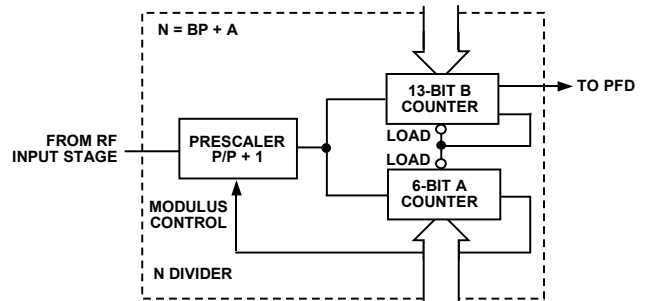


Figure 12. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR AND CHARGE PUMP

The phase frequency detector (PFD) takes inputs from the R counter and N counter ($N = BP + A$) and produces an output proportional to the phase and frequency difference between them. Figure 13 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse (see Figure 16). Use of the minimum antibacklash pulse width is not recommended.

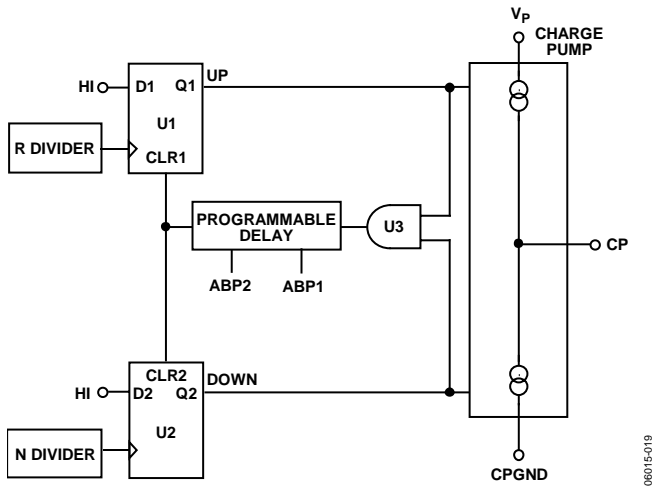


Figure 13. PFD Simplified Schematic and Timing (in Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4108 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 18 shows the full truth table. Figure 14 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When the lock detect precision (LDP) bit in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output is high with narrow, low going pulses.

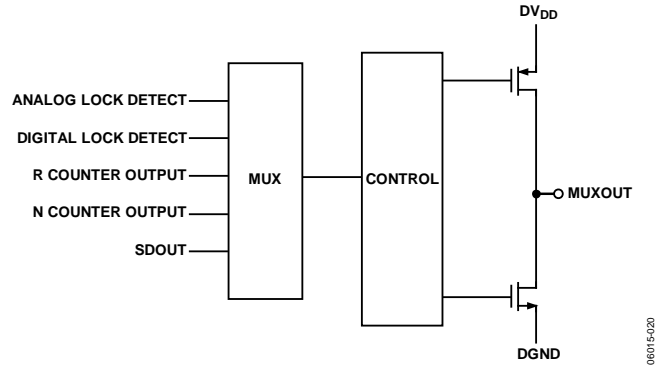


Figure 14. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4108 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the 2 LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 5.

Figure 15 shows a summary of how the latches are programmed.

Table 5. C2 and C1 Truth Table

Control Bits		Data Latch
C2	C1	
0	0	R counter
0	1	N counter (A and B)
1	0	Function latch (including prescaler)
1	1	Initialization latch

LATCH SUMMARY

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS			ANTI- BACKLASH WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21		DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED			CP GAIN	13-BIT B COUNTER											6-BIT A COUNTER						CONTROL BITS		
DB23	DB22	DB21		DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCALER VALUE		POWER- DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE- STATE	PD POLARITY	MUXOUT CONTROL			POWER- DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22		DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12					DB11	DB10	DB9			DB8	DB7
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER- DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE- STATE	PD POLARITY	MUXOUT CONTROL			POWER- DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22		DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12					DB11	DB10	DB9			DB8	DB7
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

Figure 15. Latch Summary

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REFERENCE COUNTER LATCH MAP

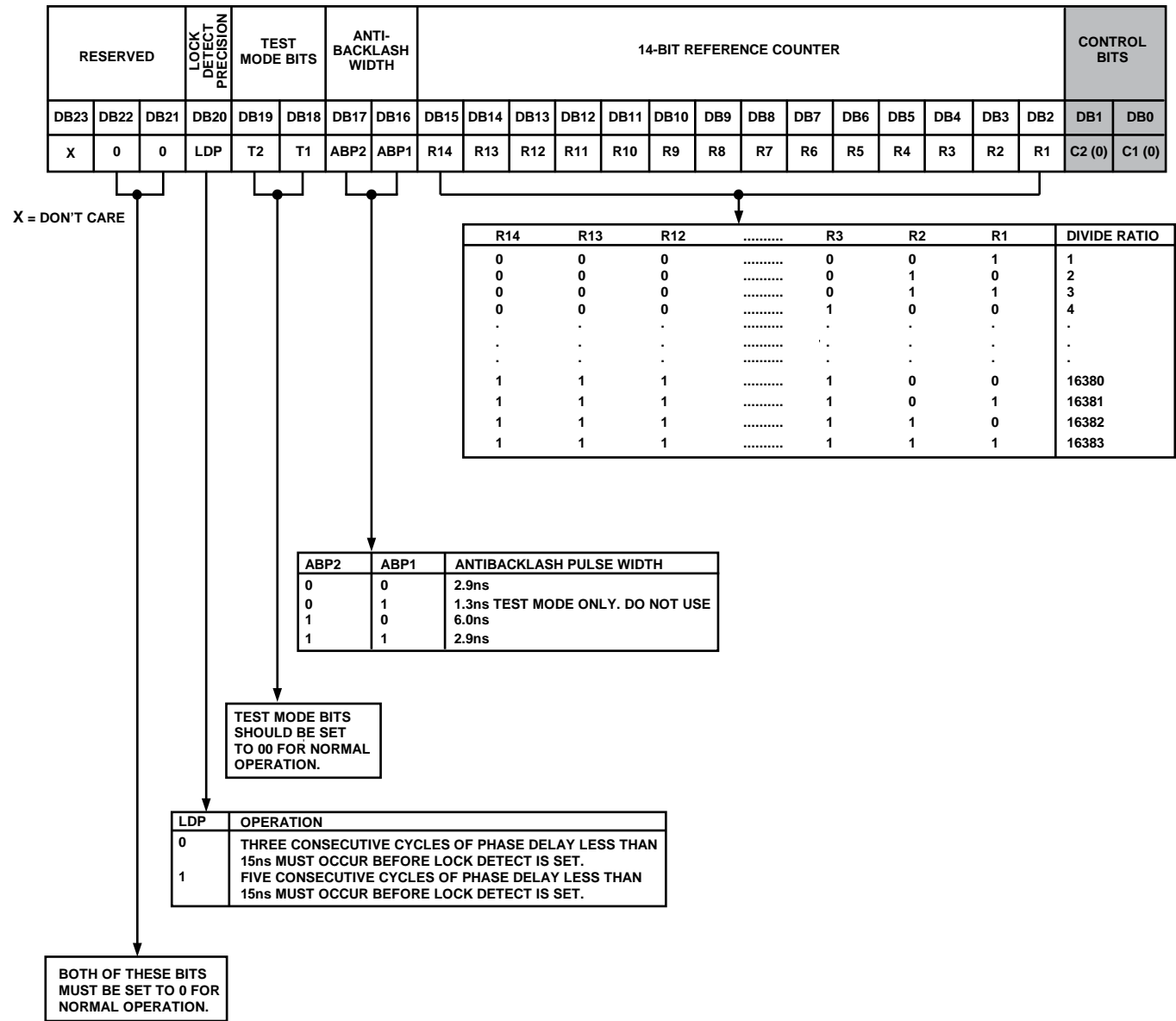


Figure 16. Reference Counter Latch Map

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AB COUNTER LATCH MAP

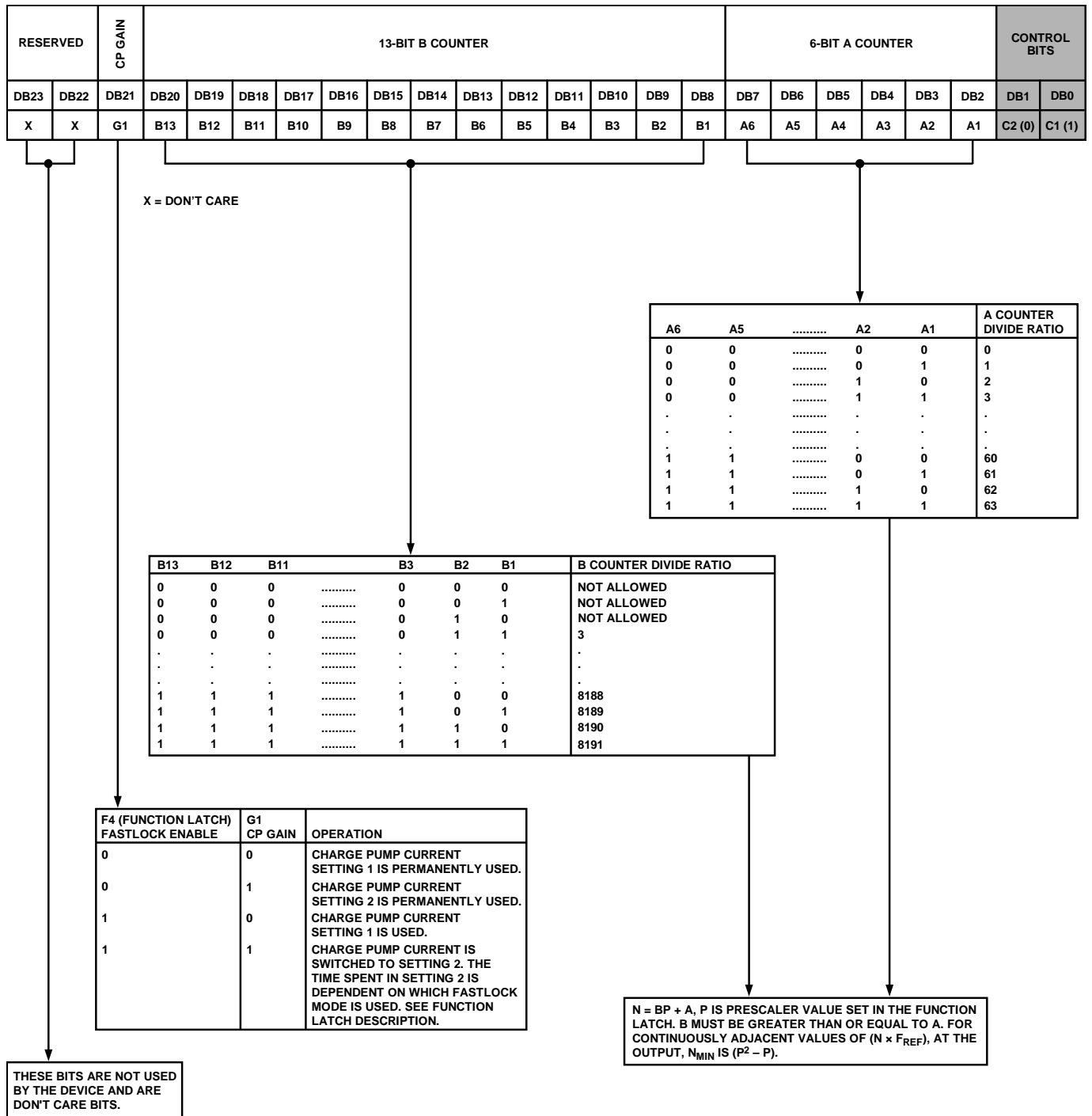


Figure 17. AB Counter Latch Map

FUNCTION LATCH MAP

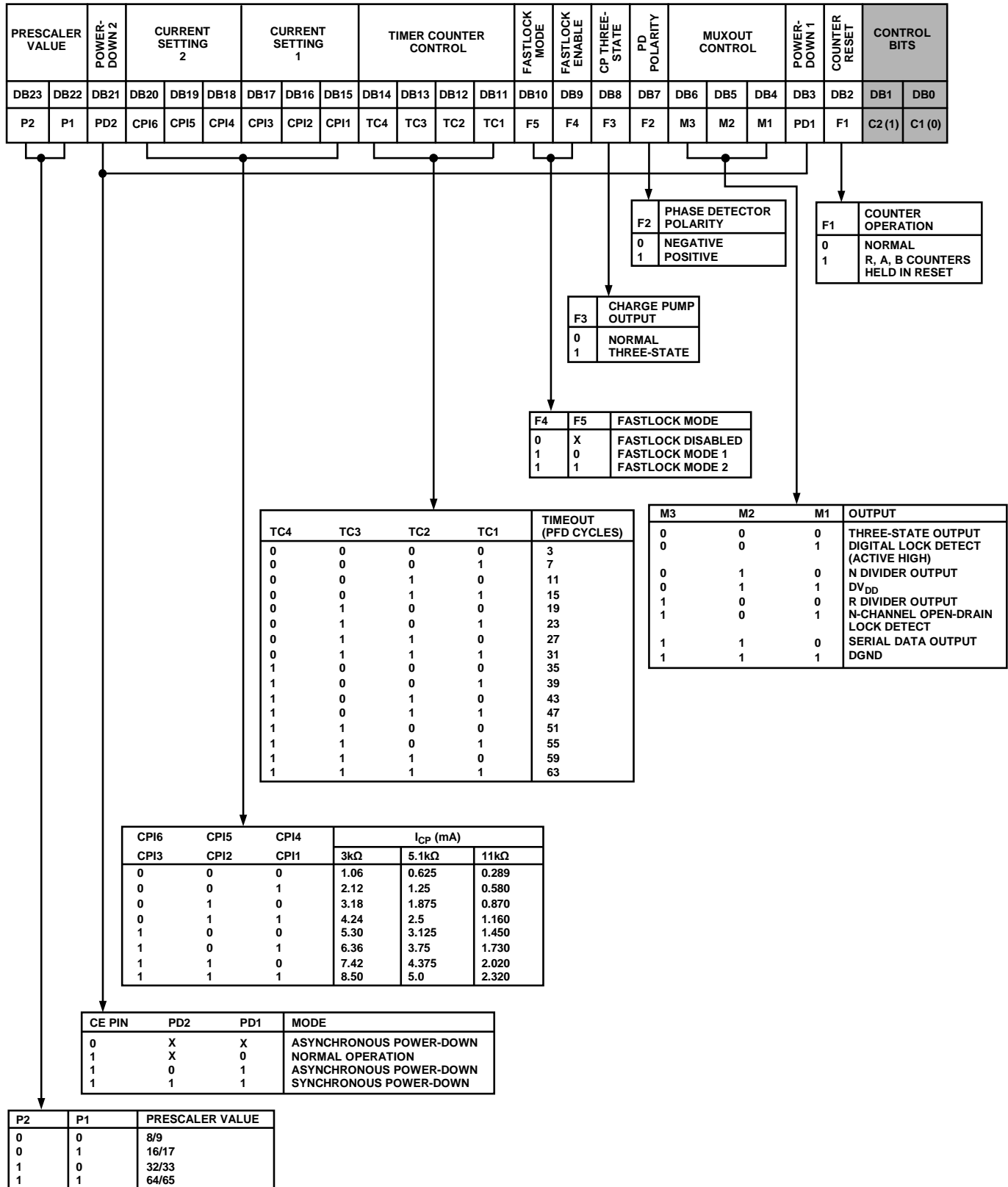


Figure 18. Function Latch Map

INITIALIZATION LATCH MAP

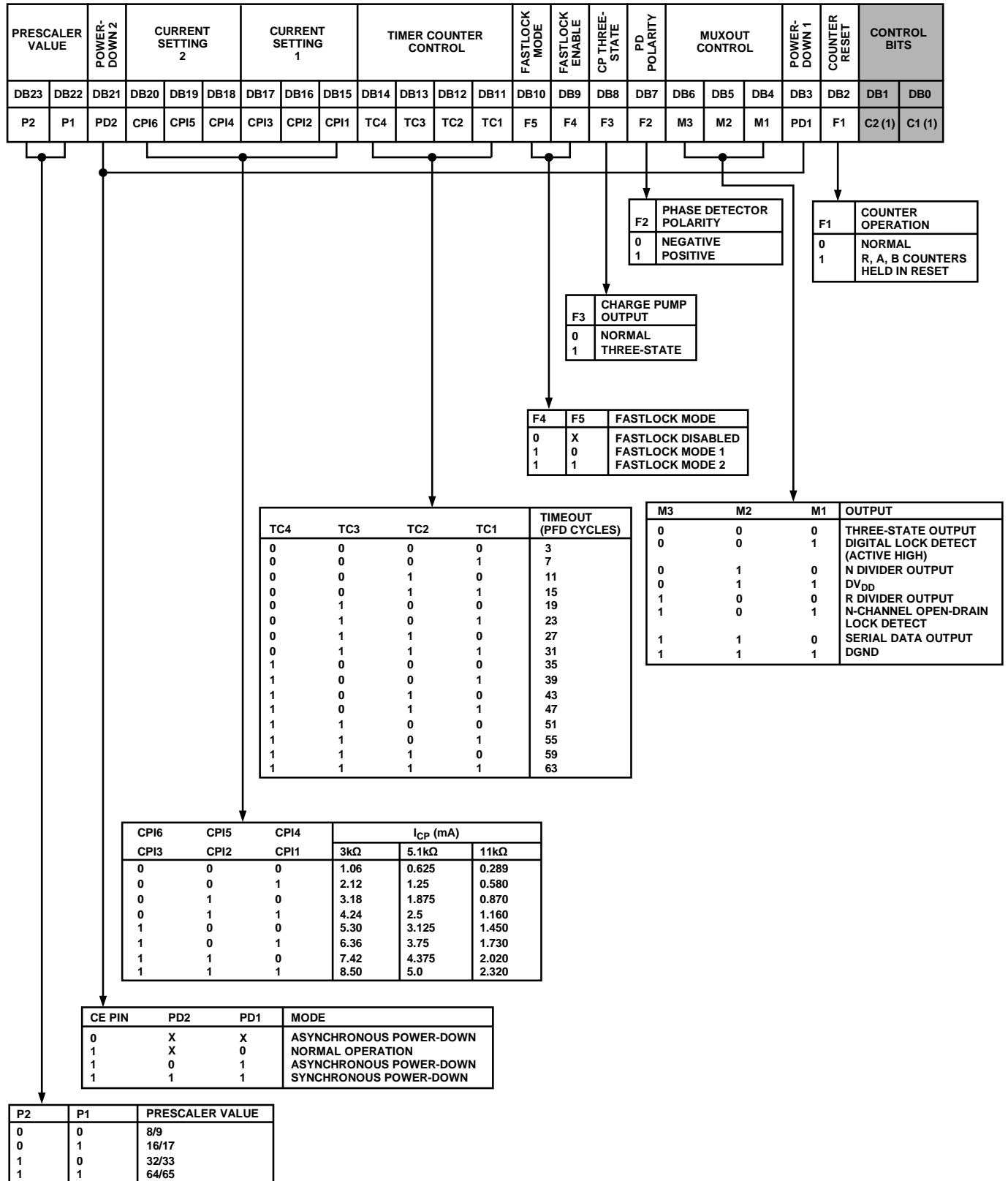


Figure 19. Initialization Latch Map

FUNCTION LATCH

The on-chip function latch is programmed with C2 and C1 set to 1 and 0, respectively. Figure 18 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this bit is 1, the R counter and the AB counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit needs to be disabled (set to 0). Then, the N counter resumes counting in close alignment with the R counter. (The maximum error is one prescaler cycle.)

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2 and PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into the PD1 bit, with the condition that PD2 has been loaded with a 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into PD1 (on condition that a 1 has also been loaded to PD2), the device goes into power-down on the occurrence of the next charge pump event.

When a power-down is activated (either synchronous or asynchronous mode, including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RFIN input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the [ADF4108](#). Figure 18 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. Fastlock is enabled only when this bit is 1.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected; and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2.

The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2.

The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4:TC1, the CP gain bit in the AB counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Figure 18 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed).

The normal sequence of events is as follows:

The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, it must be decided how long the secondary current is to stay active before reverting to the primary current. This is controlled by the timer counter control bits, DB14:DB11 (TC4:TC1) in the function latch. The truth table is given in Figure 18.

Now, to program a new output frequency, the user simply programs the AB counter latch with new values for A and B. At the same time, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6:CPI4 for a period of time determined by TC4:TC1. When this time is up, the charge pump current reverts to the value set by CPI3:CPI1. At the same time, the CP gain bit in the AB counter latch is reset to 0 and is now ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Figure 18.

Prescaler Value

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 300 MHz. Thus, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

PD Polarity

This bit sets the phase detector polarity bit. See Figure 18.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

INITIALIZATION LATCH

The initialization latch is programmed when C2 and C1 are set to 1 and 1. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0).

However, when the initialization latch is programmed, an additional internal reset pulse is applied to the R and AB counters. This pulse ensures that the AB counter is at load point when the AB counter data is latched and the device will begin counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high; PD1 bit is high; PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse and so close phase alignment is maintained when counting resumes.

When the first AB counter data is latched after initialization, the internal reset pulse is again activated. However, successive AB counter loads after this do not trigger the internal reset pulse.

Device Programming After Initial Power-Up

After initially powering up the device, there are three ways to program the device.

Initialization Latch Method

1. Apply V_{DD} .
2. Program the initialization latch (11 in 2 LSBs of input word). Make sure that the F1 bit is programmed to 0.
3. Next, do a function latch load (10 in 2 LSBs of the control word), making sure that the F1 bit is programmed to a 0.
4. Then do an R load (00 in 2 LSBs).
5. Then do an AB load (01 in 2 LSBs).

When the initialization latch is loaded, the following occurs:

1. The function latch contents are loaded.
2. An internal pulse resets the R, AB, and timeout counters to load state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first AB counter data after the initialization word activates the same internal reset pulse. Successive AB loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method

1. Apply V_{DD} .
2. Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the AB counter latch (01).
6. Bring CE high to take the device out of power-down. The R and AB counters will now resume counting in close alignment.

Note that after CE goes high, a duration of 1 μ s may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after V_{DD} was initially applied.

Counter Reset Method

1. Apply V_{DD} .
2. Do a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in 2 LSBs).
4. Do an AB counter load (01 in 2 LSBs).
5. Do a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

POWER SUPPLY CONSIDERATIONS

The [ADF4108](#) operates over a power supply range of 3.2 V to 3.6 V. The [ADP3300ART-3.3](#) is a low dropout linear regulator from Analog Devices, Inc. It outputs 3.3 V with an accuracy of 1.4% and is recommended for use with the [ADF4108](#).

INTERFACING

The **ADF4108** has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 μ s. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

ADUC812 INTERFACE

Figure 20 shows the interface between the **ADF4108** and the **ADuC812** MicroConverter[®]. Because the **ADuC812** is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the **ADF4108** needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the **ADF4108**, it needs four writes (one each to the initialization latch, function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the **ADuC812** are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the **ADuC812** is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

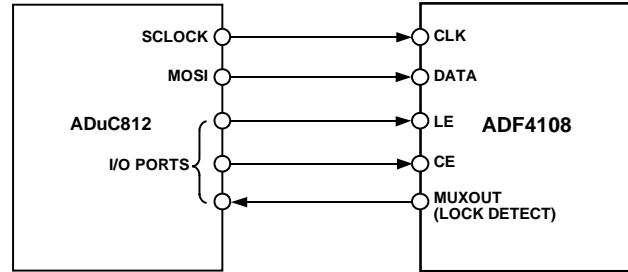


Figure 20. **ADuC812** to **ADF4108** Interface

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ADSP-21xx INTERFACE

Figure 21 shows the interface between the **ADF4108** and the **ADSP-21xx** digital signal processor. The **ADF4108** needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the **ADSP-21xx** family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

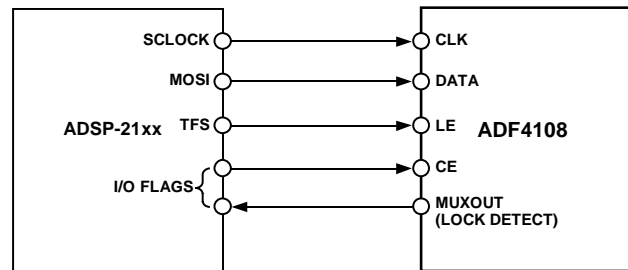


Figure 21. **ADSP-21xx** to **ADF4108** Interface

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PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

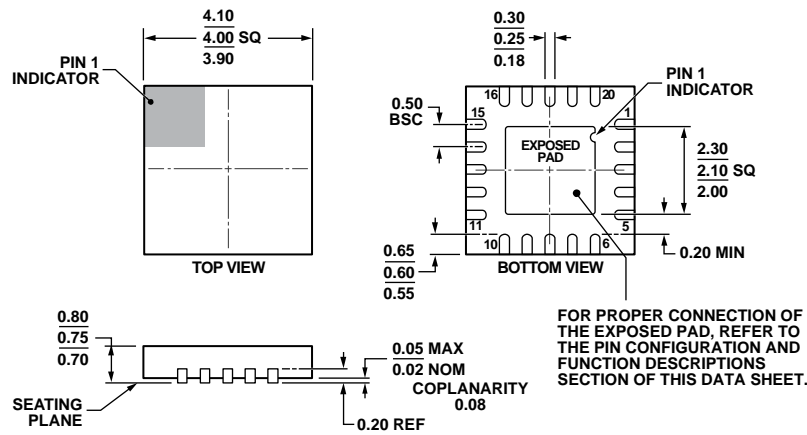
The lands on the chip scale package (CP-20-6) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad.

The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz. copper to plug the via.

The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.
 Figure 22. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
 4 mm x 4 mm Body, Very Very Thin Quad
 (CP-20-6)
 Dimensions shown in millimeters

08-16-2010-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADF4108BCPZ	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4108BCPZ-RL	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4108BCPZ-RL7	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
EV-ADF4108EB1Z		Evaluation Board	
EV-ADF4108EB2Z		Evaluation Board	

¹ Z = RoHS Compliant Part.