19-5032; Rev 3; 9/11

Dual DCL with Integrated Level Setters

General Description

The MAX19000 is a fully integrated, dual-channel, high-performance pin-electronics driver/comparator/load (DCL) with built-in level setters, and is ideal for memory and SOC ATE systems. Each MAX19000 channel includes a three-level pin driver, a window comparator, dynamic clamps, an active load, programmable cable-loss compensation, and built-in programmable level setters.

The driver features a wide -2V to +6V operating range and a data rate of 1200Mbps at +2V operation. The driver includes high impedance, active termination (3rd-level drive), and is highly linear even at low-voltage swings. The window comparators provide extremely low timing variation with changes in slew rate, common mode, pulse width, and overdrive. The active load has an extended I_{OH} and I_{OL} current range, providing up to 20mA. The dynamic clamps provide damping of high-speed DUT waveforms when the DCL is in high-impedance receive mode. A serial interface configures the device, easing PCB signal routing.

The MAX19000 is available in a 64-pin TQFP package with an exposed pad.

Applications

Memory Testers

SOC Testers

Features

- **High Speed: 1200Mbps at +2V Operation**
- **Fast Rise/Fall Times: 400ps Maximum at +2V (20% to 80%)**
- **Extremely Low Power Dissipation: 1.3W/Channel**
- **Wide, High-Speed Voltage Range: -2V to +6V**
- **Low-Leakage Mode: 10nA Maximum**
- **Integrated Termination On the Fly (3rd-Level Drive)**
- **Programmable Cable-Loss Compensation (Drive and Receive)**
- **20mA Active Load**
- **Digital Slew-Rate Control**
- **Integrated Voltage Clamps**
- **Integrated Level Setters**
- **Adjustable Output Resistance**
- **Adjustable Comparator Hysteresis**
- **Very Low Timing Dispersion**
- **Serial-Control Interface**
- **Minimal External Component Count**

Ordering Information/Selector Guide

PART	TEMP RANGE	COMPARATOR OUTPUT (mA)	DATA_/NDATA_ RCV_/NRCV_ DIFFERENTIAL TERMINATION (Ω)	PIN-PACKAGE
MAX19000BECB+	0°C to +70°C	12	100	64 TQFP-EP*
MAX19000BECB+T	0°C to +70°C	12	100	64 TQFP-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... -0.3V to +11V
V_{EE} to GND ..... -6V to +0.3V
Any V_{CC} to Any V_{EE} ..... +16.5V
V_{DD} to DGND ..... -0.3V to +5V
DGND to GND ..... ±0.3V
GNDDAC_ to GND ..... ±0.3V
DGND to GNDDAC_ ..... ±0.3V
DGS to GND ..... ±1V
CTV_ to GND ..... -0.3V to +5V
DATA_, NDATA_ to GND ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
RCV_, NRCV_ to GND ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
CH_, NCH_, CL_, NCL_ to GND ..... ($V_{CTV\_}$ - 1.1V) to ($V_{CTV\_}$ + 0.3V)
Current into CH_, NCH_, CL_, NCL_ ..... ±10mA
DATA_ to NDATA_, RCV_ to NRCV_ ..... ±10mA
DUT_ to GND ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
$\overline{SCLK}$, DIN, $\overline{CS}$, $\overline{LOAD}$ to DGND ..... -0.3V to (V_{DD} + 0.3V)
$\overline{RST}$, $\overline{LLEAKP\_}$ to DGND ..... -0.3V to (V_{DD} + 0.3V)
OVALARM, TALARM to DGND ..... -0.3V to (V_{DD} + 0.3V)
TEMP to GND ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
REF to GND ..... -0.3V to the lower of ($V_{GNDDAC\_}$ + 2.6V) and (V_{CC} + 0.3V)
REF Current ..... ±75mA
All Digital Inputs ..... ±30mA
DUT_ Short-Circuit Duration ..... Continuous
Continuous Power Dissipation
64-Pin TQFP (derate 125mW/°C above +70°C) 10W
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C
ESD, Human Body Model:
All Pins Excluding Pins Below 2.000V
ESD, Human Body Model: DATA_, NDATA_ 1.500V
ESD, Human Body Model: RCV_, NRCV_ 1.500V
Humidity ..... 10% to 90%

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

64 TQFP-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 40°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
DRIVER DC CHARACTERISTICS (R_L ≥ 10MΩ, unless otherwise noted; includes level-setter error)						
Output-Voltage Range	$V_{DHV\_}$	$V_{DLV\_}$ = -2V, $V_{DTV\_}$ = +1.5V	-1.8		+6	V
	$V_{DLV\_}$	$V_{DHV\_}$ = +6V, $V_{DTV\_}$ = +1.5V	-2		+5.8	
	$V_{DTV\_}$	$V_{DHV\_}$ = +6V, $V_{DLV\_}$ = -2V	-2		+6	
Output Offset Voltage (Note 2)	V_{DHVOS}	$V_{DHV\_}$ = +0.125V, $V_{DLV\_}$ = -2V, $V_{DTV\_}$ = +1.5V			±2	mV
	V_{DLVOS}	$V_{DLV\_}$ = +0.125V, $V_{DHV\_}$ = +6V, $V_{DTV\_}$ = +1.5V			±2	
	V_{DLVOS}	$V_{DTV\_}$ = +0.125V, $V_{DHV\_}$ = +6V, $V_{DLV\_}$ = -2V			±2	
Output-Voltage Temperature Coefficient (Notes 3, 4)	$V_{DHV\_}$			±75	±500	µV/°C
	$V_{DLV\_}$			±75	±500	
	$V_{DTV\_}$			±75	±500	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain (Note 2)	$A_{DHV\_}$	$V_{DLV\_}$ = -2V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +0.125V and +3.875V	0.998	1	1.002	V/V
	$A_{DLV\_}$	$V_{DHV\_}$ = +6V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = +0.125V and +3.875V	0.998	1	1.002	
	$A_{DTV\_}$	$V_{DHV\_}$ = +6V, $V_{DLV\_}$ = -2V, $V_{DTV\_}$ = +0.125V and +3.875V	0.998	1	1.002	
Linearity Error, -0.5V to +4.5V (Note 2)		$V_{DLV\_}$ = -2V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -0.5V to +4.5V		±1	±6	mV
		$V_{DHV\_}$ = +6V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -0.5V to +4.5V		±1	±6	
		$V_{DLV\_}$ = -2V, $V_{DHV\_}$ = +6V, $V_{DTV\_}$ = -0.5V to +4.5V		±1	±6	
Linearity Error, -1.75V to +5.125V (Note 2)		$V_{DLV\_}$ = -2V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -1.75V and +5.125V			±12	mV
		$V_{DHV\_}$ = +6V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -1.75V and +5.125V			±12	
		$V_{DLV\_}$ = -2V, $V_{DHV\_}$ = +6V, $V_{DTV\_}$ = -1.75V and +5.125V			±12	
Linearity Error, Full Range (Note 2)		$V_{DLV\_}$ = -2V, $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = -1.8V and +6V		±5	±14	mV
		$V_{DHV\_}$ = +6V, $V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = -2V and +5.8V		±5	±14	
		$V_{DLV\_}$ = -2V, $V_{DHV\_}$ = 6V, $V_{DTV\_}$ = -2V and +6V		±5	±14	
DHV_-to-DLV_ Crosstalk		$V_{DLV\_}$ = -0.5V, $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = -0.3 and +6V			±3	mV
DLV_-to-DHV_ Crosstalk		$V_{DHV\_}$ = +4.5V, $V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = -2.0 and +4.3V			±3	mV
DTV_-to-DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = -2V and +6V			±2	mV
DHV_-to-DTV_ Crosstalk		$V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 1.6V and +3V			±3	mV
DLV_-to-DTV_ Crosstalk		$V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V and +1.4V			±3	mV
Term Voltage Dependence on DATA_		$V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, DATA_ = 0 and 1			±2	mV

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Power-Supply Rejection	$PSRR_{DHV}$	$V_{DHV\_}$ = +3V, V_{CC} and V_{EE} independently varied full range		39			dB
	$PSRR_{DLV}$	$V_{DLV\_}$ = 0V, V_{CC} and V_{EE} independently varied full range		39			
	$PSRR_{DTV}$	$V_{DTV\_}$ = +1.5V, V_{CC} and V_{EE} independently varied full range		39			
DC Drive Current Limit		R_L= 0, when DATA_ = H, $V_{DHV\_}$ = +6V and $V_{DUT\_}$ = -2V; when DATA_ = L, $V_{DLV\_}$ = -2V and $V_{DUT\_}$ = +6V		±65		±110	mA
DC Output Resistance		(Note 5)		46	48	50	Ω
DC Output Resistance Variation (Note 6)		DATA_ = H, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1V, $I_{DUT\_}$ = 1mA to 40mA			1	2	Ω
		DATA_ = L, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1V, $I_{DUT\_}$ = -1mA to -40mA			1	2	
Adjustable Output Resistance Range	ΔR_O	R_O = Fh vs. R_O = 8h and R_O = 0h vs. R_O = 8h, resolution of 0.36Ω conditions (Note 5)		±2.5			Ω
DRIVER AC CHARACTERISTICS (R_L = 50Ω to GND) (Note 7)							
Dynamic Drive Current		(Note 8)		±100			mA
Drive Mode Overshoot		Cable-droop compensation off, CDRP_ = 000b	$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +0.1V	40			%
			$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V	8			
			$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +3V	3			
			$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +5V	2			
Drive Mode Undershoot		Cable-droop compensation off, CDRP_ = 000b	$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +0.1V	20			%
			$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V	5			
			$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +3V	2			
			$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +5V	2			
Cable-Droop Compensation Range, Fast Time Constant		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V, CDRP_S = 000		0			%
		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V, CDRP_S = 111		20			

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cable-Droop Compensation Range, Slow Time Constant		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V, CDRP_L = 000		0		%
		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V, CDRP_L = 111		20		
Driver Cable-Droop Compensation, Short Time Constant				80		ps
Driver Cable-Droop Compensation, Long Time Constant				1.3		ns
Termination Mode Overshoot		Cable-droop compensation off (Notes 4, 9)		0	50	mV
Settling Time (Note 4)		To within 100mV, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V (Note 10)		0.25	1	ns
		To within 50mV, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V (Note 10)		0.25	1	
		To within 25mV, $V_{DHV\_}$ = +0.5V, $V_{DLV\_}$ = 0V (Note 10)		0.25	1	
TIMING CHARACTERISTICS (Notes 7, 11)						
Propagation Delay, Data to Output		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V (Note 12)	0.6	1.0	1.4	ns
Propagation Delay Match, t_{LH} vs. t_{HL}		(Note 4)		±40	±80	ps
Propagation Delay Match, Drivers Within Package		Same edge		40		ps
Propagation Delay Temperature Coefficient		(Note 4)		1	5	ps/°C
Propagation Delay Change vs. Pulse Width		$V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V, 0.85ns to 24.150ns pulse width (Note 4)		±25	±50	ps
		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 1ns to 24ns pulse width (Note 4)		±35	±60	
		$V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, 1.5ns to 23.5ns pulse width		±100		
Propagation Delay Change vs. Common Mode (Note 4)		$V_{DHV\_}$- $V_{DLV\_}$ = +1V, $V_{DHV\_}$ = +1V to +4V (using a DC block)		50	60	ps
		$V_{DHV\_}$- $V_{DLV\_}$ = +1V, $V_{DHV\_}$ = -1V to +6V (using a DC block)		50	120	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay, Drive to High Impedance, High Impedance to Drive		$V_{DHV\_}$ = +1V, $V_{DLV\_}$ = -1V (Notes 4, 13)	1.5	2.1	2.8	ns
Delay Match, Drive to High Impedance vs. High Impedance to Drive		$V_{DHV\_}$ = +1V, $V_{DLV\_}$ = -1V (Note 14)		±0.5		ns
Delay Match, High Impedance vs. Data				±1.3		ns
Propagation Delay, Drive to Term, Term to Drive		(Notes 4, 15)	1.7	2.5	3.4	ns
Delay Match, Drive to Term vs. Term to Drive		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V (Note 16)		±0.5		ns
Delay Match, Term vs. Data				±1.5		ns
Rise and Fall Time		+0.2V_{P-P} programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V, 20% to 80% (Note 17)		140		ps
		+0.2V_{P-P} programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V, 20% to 80% (Note 18)		150		
		+1V_{P-P} programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V, 10% to 90% (Notes 4, 17)	200	270	400	
		+1V_{P-P} programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V, 10% to 90% (Note 18)		350		
		+1V_{P-P} programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V, 20% to 80% (Notes 4, 17)	140	190	275	
		+2V_{P-P} programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V, 20% to 80% (Notes 4, 17)	230	280	400	
		+2V_{P-P} programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V, 20% to 80% (Note 18)		280		
		+3V_{P-P} programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 10% to 90% trim condition (Note 17)	450	550	800	
		+3V_{P-P} programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 10% to 90% (Note 18)		600		
		+5V_{P-P} programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, 10% to 90% (Notes 4, 17)	650	850	1050	
		+5V_{P-P} programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, 10% to 90% (Note 18)		910		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise and Fall Time Matching (Note 17)		+0.2V_{P-P} programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V, 20% to 80%		±20		ps
		+1V_{P-P} programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V, 10% to 90%		±30	±55	
		+2V_{P-P} programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V, 20% to 80%		±25	±50	
		+3V_{P-P} programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 10% to 90%		±40	±100	
		+5V_{P-P} programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, 10% to 90%		±30		
Slew Rate, Relative to SC1 = SC0 = 0		SC1 = 0, SC0 = 1, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 20% to 80%		75		%
		SC1 = 1, SC0 = 0, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 20% to 80%		50		
		SC1 = 1, SC0 = 1, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 20% to 80%		25		
Minimum Pulse Width (Positive or Negative)		+0.2V_{P-P} programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V (Note 19)		400		ps
		+1V_{P-P} programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V (Notes 4, 19)		475	610	
		+1V_{P-P} programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V; output reaches at least 90% of its nominal DC output level (Note 4)		390	525	
		+2V_{P-P} programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V (Notes 4, 19)		665	833	
		+3V_{P-P} programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V (Notes 4, 19)		800	1000	
		+5V_{P-P} programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V (Note 19)		1300		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate		+0.2V_{P-P} programmed, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V (Note 20)		2500		Mbps
		+1V_{P-P} programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V (Notes 4, 20)	1650	2100		
		+1V_{P-P} programmed, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V; output reaches at least 90% of its nominal DC output level (Note 4)	1750	2570		
		+2V_{P-P} programmed, $V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V (Notes 4, 20)	1200			
		+3V_{P-P} programmed, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V (Notes 4, 20)	1000			
		+5V_{P-P} programmed, $V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V (Note 20)		900		
Rise and Fall Time, Drive to Term		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V; measured 10% to 90% of waveform (Note 21)	250	700	1300	ps
Rise and Fall Time, Term to Drive		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V; measured 10% to 90% of waveform (Note 21)	400	550	800	ps
COMPARATOR						
COMPARATOR DC CHARACTERISTICS (Note 22)						
Input-Voltage Range			-2.2		±6.2	V
Differential Input Voltage		$V_{DUT\_}$ - $V_{CH\_}$, $V_{DUT\_}$ - $V_{CL\_}$			±8.4	V
Input Offset Voltage		$V_{DUT\_}$ = +2V (Note 23)		±1	±5	mV
Input-Voltage Temperature Coefficient		(Notes 23, 24)		±50		µV/°C
Common-Mode Rejection	CMRR	$V_{DUT\_}$ = -2V, +6V (Notes 23, 25)	45	50		dB
Linearity Error		-0.5V to +4.5V, $V_{DUT\_}$ = -0.5V to +4.5V (Notes 23, 26)		±1	±5	mV
		-1.75V to +5.125V, $V_{DUT\_}$ -1.75V to 5.125V (Notes 23, 26)			±8	
		-2V to +6V, $V_{DUT\_}$ = -2V, +6V (Notes 23, 26)		±2	±10	
		Full range, $V_{DUT\_}$ = -2.2V, +6.2V (Notes 23, 26)		±2		
Power-Supply Rejection	PSRR	$V_{DUT\_}$ = -2V and +6V (Notes 23, 27)	45	50		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hysteresis		HYST2 = 0, HYST1 = 0, HYST0 = 0		0		mV
		HYST2 = 0, HYST1 = 0, HYST0 = 1		2		
		HYST2 = 0, HYST1 = 1, HYST0 = 0		4		
		HYST2 = 0, HYST1 = 1, HYST0 = 1		6		
		HYST2 = 1, HYST1 = 0, HYST0 = 0		8		
		HYST2 = 1, HYST1 = 0, HYST0 = 1		10		
		HYST2 = 1, HYST1 = 1, HYST0 = 0		12		
		HYST2 = 1, HYST1 = 1, HYST0 = 1		15		
COMPARATOR AC CHARACTERISTICS (Notes 22, 28, 29, 30)						
Effective Comparator Bandwidth, Term Mode		(Notes 4, 31)	1.85	3.2		GHz
		(Note 32)		2.3		
Effective Comparator Bandwidth, High-Impedance Mode		(Note 31)		620		MHz
		(Note 33)		620		
Minimum Pulse Width		(Notes 4, 34)		0.5	0.65	ns
Propagation Delay			0.5	0.9	1.5	ns
Propagation Delay Temperature Coefficient				2.1		ps/°C
Propagation Delay Match, High/Low vs. Low/High		Absolute value of delta for each comparator (Note 4)		±10	±60	ps
PROPAGATION DELAY DISPERSIONS						
Propagation Delay Dispersion vs. Common-Mode Input		V_{CM} = -1.9V to +5.9V (Notes 4, 35)		±40	±55	ps
Propagation Delay Dispersion vs. Overdrive		V_{OD} = 50mV to +0.5V, $V_{DUT\_}$ = 0 to 1V, 2ns/V; V_{CX} = +0.5V to +0.95V		±40		ps
		V_{OD} = 50mV to +0.5V, $V_{DUT\_}$ = 0 to 1V, 2ns/V; V_{CX} = +0.5V to +0.05V		±40		
Propagation Delay Dispersion vs. Duty Cycle (Note 4)		0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width (Note 36)		±25	±40	ps
Propagation Delay Dispersion vs. Slew Rate (Note 4)		1V/ns to 6V/ns, relative to 3.5V/ns		±30	±40	ps
Waveform Tracking (Note 4)		Driver in term mode, peak-to-peak within 100mV < V_{CX} < 900mV window (Note 37)		50	80	ps
		Driver in term mode, peak-to-peak within 50mV < V_{CX} < 950mV window (Note 37)		80	130	
High-Impedance Waveform Tracking (Note 4)		Driver in high-Z, peak-to-peak within 100mV < V_{CX} < 900mV window (Note 37)		150	200	ps

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cable-Droop Compensation Range, Fast Time Constant		+1V swing, rise/fall time = 300ps, CDRP_S = 000		0		%
		+1V swing, rise/fall time = 300ps, CDRP_S = 111		20		
Cable-Droop Compensation Range, Slow Time Constant		+1V swing, rise/fall time = 300ps, CDRP_L = 000		0		%
		+1V swing, rise/fall time = 300ps, CDRP_L = 111		20		
Comparator Cable-Droop Compensation, Short Time Constant				80		ps
Comparator Cable-Droop Compensation, Long Time Constant				1.3		ns
Input Slew Rate with Cable Compensation Enabled		$V_{DUT\_}$ = 0 to 1V (Note 32)		6.0		V/ns
LOGIC OUTPUTS CH_, NCH_, CL_, NCL_ (Note 38)						
Termination Voltage CTV_		External termination voltage (Note 39)	0	1.2	3.5	V
CTV_ Current		Without external 50Ω resistors		48	56	mA
Output High Voltage		With external 50Ω resistors	$V_{CTV\_}$ - 0.1	$V_{CTV\_}$ - 0.02	$V_{CTV\_}$ + 0.05	V
Output Low Voltage		With external 50Ω resistors	$V_{CTV\_}$ - 0.45	$V_{CTV\_}$ - 0.3	$V_{CTV\_}$ - 0.25	V
Output-Voltage Swing		With external 50Ω resistors	250	300	350	mV
Output Termination Resistor		CTV0 to CH0, NCH0, CL0, NCL0; CTV1 to CH1, NCH1, CL1, NCL1	47		53	Ω
Differential Rise Time		10% to 90% (Note 4)		210	400	ps
Differential Fall Time		10% to 90% (Note 4)		210	400	ps
DYNAMIC CLAMPS (always and only enabled in driver high-impedance mode)						
Functional Clamp Range, $V_{CPHV\_}$		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = -0.9V and +6.3V, $V_{CPLV\_}$ = -2V	-0.8		6.2	V
Functional Clamp Range, $V_{CPLV\_}$		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -2.3V and +4.9V, $V_{CPHV\_}$ = +6V	-2.2		4.8	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Programmable $V_{CPHV\_}$		$I_{DUT\_}$ = 0mA (Note 40)		6.7	7.0		V
Minimum Programmable $V_{CPLV\_}$		$I_{DUT\_}$ = 0mA (Note 40)			-3.0	-2.7	V
Offset Voltage		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = +2V, $V_{CPLV\_}$ = -2V				±10	mV
		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = +2V, $V_{CPHV\_}$ = +6V				±10	
Power-Supply Rejection		V_{CC} and V_{EE} independently varied over their full range	I_{CLAMP} = -1mA, $V_{CPHV\_}$ = +2V, $V_{CPLV\_}$ = -2V	40			dB
			I_{CLAMP} = 1mA, $V_{CPLV\_}$ = +2V, $V_{CPHV\_}$ = +6V	40			
High Clamp Voltage Gain		$V_{CPHV\_}$ = -0.5V, +5.75V, $I_{DUT\_}$ = -1mA		0.998		1.002	V/V
Low Clamp Voltage Gain		$V_{CPLV\_}$ = -1.75V, +4.5V, $I_{DUT\_}$ = -1mA		0.998		1.002	V/V
Output Temperature Coefficient $V_{CPHV\_}$, $V_{CPLV\_}$		(Notes 4, 41)			±75	±750	µV/°C
Linearity, Relative to End Points		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = -0.8V to +6V				±30	mV
		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -2V to +4.8V				±30	
Static Output Current		$V_{CPHV\_}$ = 0V, $V_{CPLV\_}$ = -2V, R_L = 0Ω to +6V		-120		-60	mA
		$V_{CPLV\_}$ = +5V, $V_{CPHV\_}$ = +6V, R_L = 0Ω to -2V		60		120	
DC Impedance, High Clamp		$I_{DUT\_}$ = -5mA and -15mA, $V_{CPHV\_}$ = +3V, $V_{CPLV\_}$ = 0V		48		56	Ω
DC Impedance, Low Clamp		$I_{DUT\_}$ = 5mA and 15mA, $V_{CPHV\_}$ = +3V, $V_{CPLV\_}$ = 0V		48		56	Ω
DC Impedance Variation, High Clamp		$I_{DUT\_}$ = -20mA and -30mA, $V_{CPHV\_}$ = +2.5V, $V_{CPLV\_}$ = -2V (Note 42)			±5		Ω
DC Impedance Variation, Low Clamp		$I_{DUT\_}$ = 20mA and 30mA, $V_{CPLV\_}$ = +2.5V, $V_{CPHV\_}$ = +6V (Note 42)			±5		Ω
Ripple		(Note 43)			50		mV
ACTIVE LOAD							
DC ELECTRICAL CHARACTERISTICS ($V_{COMV\_}$ = +2V, $V_{LDHV\_}$ = $V_{LDLV\_}$ = +5.5V, unless otherwise noted)							
COMV_ Voltage Range	$V_{COMV\_}$			-2		+6	V

Dual DCL with Integrated Level Setters

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMV_ Offset Voltage	V_{COMVOS}	$I_{DUT\_}$ = 0A, $V_{COMV\_}$ = +2V			±5	mV
Differential Voltage Range		$V_{DUT\_}$ - $V_{COMV\_}$			±8	V
COMV_ Temperature Coefficient		(Notes 4, 41)		±100	±750	µV/°C
COMV_ Voltage Gain	A_V	$V_{COMV\_}$ = +0.125V and +3.875V	0.998		1.002	V/V
COMV_ Linearity Error		V_{COMV} = -2V to +6V, relative to end points		±3	±15	mV
COMV_ Output-Voltage Power-Supply Rejection Ratio	$PSRR_{COM}$	V_{CC} and V_{EE} independently varied over full range	40			dB
Output Resistance, Sink or Source	R_O	I_{SRC} = I_{SNK} = 20mA, $V_{DUT\_}$ = +2.5V, +6V with $V_{COMV\_}$ = -2V or $V_{DUT\_}$ = -2V, +1.5V with $V_{COMV\_}$ = +6V	30			kΩ
		I_{SRC} = I_{SNK} = 1mA, $V_{DUT\_}$ = +2.5V, +6V with $V_{COMV\_}$ = -2V or $V_{DUT\_}$ = -2V, +1.5V with $V_{COMV\_}$ = +6V	500			
Output Resistance, Linear Region	R_O	$I_{DUT\_}$ = ±14.25mA, I_{SRC} = I_{SNK} = 15mA, $V_{COMV\_}$ = +1.5V (Note 44)		22	27	Ω
Dead Band		I_{SRC} = I_{SNK} = 15mA, 80% commutation		450		mV
		I_{SRC} = I_{SNK} = 15mA, 95% I_{SRC} to 95% I_{SNK}		625	700	
SOURCE CURRENT ($V_{DUT\_}$ = -1.5V, $V_{COMV\_}$ = +5.5V, $V_{LDLV\_}$ = -0.5V, $V_{LDHV\_}$ = +5.5V, unless otherwise noted)						
Source Current Output Range	I_{SRC}	$V_{LDHV\_}$ = 0 to +6V	0		20	mA
Source Current Offset		I_{SRC} = 1mA	-20		+20	µA
Source Current Programming Gain		I_{SRC} = 1mA, 18mA	3.326	3.333	3.34	mA/V
Source Current Temperature Coefficient		I_{SRC} = 10mA		-10		µA/°C
Source Current Power-Supply Rejection		V_{CC} and V_{EE} independently varied over full range			±90	µA/V
Source Current Linearity		I_{SRC} = 0.33mA, 1mA, 5mA, 10mA, 18mA, and 20mA relative to 2-point calibration at 1mA and 18mA			±60	µA
SINK CURRENT ($V_{DUT\_}$ = +5.5V, $V_{COMV\_}$ = -1.5V, $V_{LDHV\_}$ = -0.5V, $V_{LDLV\_}$ = +5.5V, unless otherwise noted)						
Sink Current Output Range	I_{SNK}	$V_{LDLV\_}$ = 0 to +6V	0		20	mA
Sink Current Offset		I_{SNK} = 1mA	-20		+20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sink Current Programming Gain		I_{SNK} = 1mA, 18mA	3.326	3.333	3.34	mA/V
Sink Current Temperature Coefficient		I_{SNK} = 10mA		10		µA/°C
Sink Current Power-Supply Rejection Ratio		V_{CC} and V_{EE} independently varied over full range			±60	µA/V
Sink Linearity		I_{SNK} = 0.33mA, 1mA, 5mA, 10mA, 18mA, and 20mA relative to 2-point calibration at 1mA and 18mA			±60	µA
AC ELECTRICAL CHARACTERISTICS (Z_L = 50Ω to GND, $V_{LDHV\_}$ = $V_{LDLV\_}$ = +6V, TMSEL = LDDIS = LDCAL = 0)						
Transition Time to/from Inhibit through RCV_ Input (from Load to Drive)		Measured from 50% crossing of RCV_ to 10% level of output waveform; $V_{COMV\_}$ = -1.5V and +1.5V		2.5		ns
Transition Time to/from Inhibit through RCV_ Input (from Drive to Load)		Measured from 50% crossing of RCV_ to 10% level of output waveform; $V_{COMV\_}$ = -1.5V and +1.5V		4.5		ns
Spike During Enable/Disable Time (Note 4)		50Ω load to ground, I_{SRC} = I_{SNK} = 20mA, $V_{COMV\_}$ = 0V		200	300	mV
TEMPERATURE MONITOR (TSMUX0 = 1)						
Nominal Voltage		T_J = +70°C, $R_L \geq$ 10MΩ		3.43		V
Nominal Voltage Variation		T_J = +125°C, $R_L \geq$ 10MΩ, one standard deviation		±50		mV
Temperature Coefficient				10		mV/°C
Output Resistance				22		kΩ
TEMPERATURE COMPARATOR/ALARM						
Comparator Hysteresis				0		°C
Alarm Threshold				125		°C
TEMP Leakage Current, Disabled		TSMUX0 = 0, tested at V_{FORCE} = 4V			1	µA
Temperature Alarm Accuracy				±5		°C
DIGITAL I/O						
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_)						
Input High Voltage	V_{IH}	Functional test	+0.2		3.5	V
Input Low Voltage	V_{IL}	Functional test	-0.2		3.1	V
Differential Input Voltage		Functional test	±0.15		±1.0	V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Termination Resistance		Differential termination between DATA_/ NDATA_ and RCV_/NRCV_; tested at ±4mA	96		104	Ω
SINGLE-ENDED INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$, $\overline{LOAD}$, $\overline{LLEAKP\_}$)						
Input High			2/3 (V_{DD})		V_{DD}	V
Input Low			-0.1		1/3 (V_{DD})	V
Input Bias Current					±25	µA
SINGLE-ENDED OUTPUT (DOUT)						
High Output	V_{OH}	I_{OH} = 25µA	V_{DD} - 0.15		V_{DD} + 0.1	V
Low Output	V_{OL}	I_{OL} = - 25µA	V_{DGND} - 0.01		V_{DGND} + 0.15	V
SINGLE-ENDED OPEN-COLLECTOR OUTPUTS (OVALARM, TALARM) (with external 1kΩ to V_{DD})						
V_{VOC} Voltage Range			V_{DD} - 0.3		V_{DD} + 0.3	V
Low Output	V_{OL}		V_{DGND}		V_{VOC} - 1	V
SERIAL-PORT TIMING						
SCLK Frequency					50	MHz
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}		10			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		4.25			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		4.25			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		4.25			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		4.25			ns
DIN to SCLK High Setup	t_{DS}		4.25			ns
DIN to SCLK High Hold	t_{DH}		4.25			ns
$\overline{CS}$ High Pulse Width	t_{CSWH}		40			ns
$\overline{LOAD}$ Low Pulse Width	t_{LDW}		20			ns
$\overline{RST}$ Low Pulse Width	t_{RST}		20			ns
$\overline{CS}$ High to $\overline{LOAD}$ Low Hold	t_{CSHLD}		50			ns
SCLK to DOUT Delay	t_{DO}				62.4	ns
COMMON FUNCTIONS (V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, unless otherwise noted)						
Operating Voltage Range			-2.2		+6.2	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Impedance Leakage	$I_{DUT\_}$	$V_{DUT\_}$ = 0V, +1.5V, +3V			±2	µA
		$V_{CL\_}$ = $V_{CH\_}$ = +6V, $V_{DUT\_}$ = -2V			±3	
		$V_{CL\_}$ = $V_{CH\_}$ = -2V, $V_{DUT\_}$ = +6V			±3	
Low-Leakage Mode	$I_{DUT\_}$	$V_{DUT\_}$ = 0V, +1.5V, +3V, T_J < +90°C			±10	nA
		$V_{CL\_}$ = $V_{CH\_}$ = 6V, $V_{DUT\_}$ = -2V, T_J < +90°C			±10	
		$V_{CL\_}$ = $V_{CH\_}$ = -2V, $V_{DUT\_}$ = +6V, T_J < +90°C			±10	
Combined Capacitance		Driver in terminate mode (Note 4)		2.5	3	pF
		Driver in high-Z		5		
Low-Leakage Enable Time		$\overline{LLEAKP\_}$ low to $I_{DUT\_}$ specification		20		µs
Low-Leakage Disable Time		$\overline{LLEAKP\_}$ high to normal operation		20		µs
Low-Leakage Spike, $V_{DLV\_}$/Leakage		$V_{DLV\_}$ = 0V, Z_L = 10MΩll8pF to GND (Note 4)	-200		+600	mV
Low-Leakage Spike, $V_{DHV\_}$/Leakage		$V_{DHV\_}$ = +2V, Z_L = 10MΩll8pF to GND (Note 4)	-200		+350	mV
Low-Leakage Spike, High Impedance/Leakage		R_L = 50Ω to GND (Note 4)	-125		+350	mV
DUT_ OVERVOLTAGE ALARM						
Maximum Programmable $V_{CPH\_}$			6.7	7		V
Minimum Programmable $V_{CPL\_}$				-3	-2.7	V
Voltage Accuracy		$V_{CPHV\_}$ = 6.7V and $V_{CPLV\_}$ = -2.7V			150	mV
Will-Operate Current				±6		mA
Comparator Delay		With 50mV overdrive on DUT_ signal		390		ns
Comparator Hysteresis				10		mV
POWER SUPPLIES						
Positive Supply	V_{CC}		9	9.25	10	V
Negative Supply	V_{EE}		-5.35	-5.25	-4.75	V
Logic Supply	V_{DD}		2.3	3.3	3.6	V
Positive Supply	I_{CC}	(Note 45)		145	160	mA
Negative Supply	I_{EE}	(Note 45)		235	260	mA
Logic Supply	I_{DD}	(Note 45)		8	10	mA
Power Dissipation		V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, load disabled		1.33	1.47	W/Ch

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation, Load Enabled		V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V; load enabled; I_{SRC} = I_{SNK} = 20mA; $V_{COMV\_}$ = +1.5V; $V_{DUT\_}$ held at 0V by short to GND		1.52	1.7	W/Ch
ANALOG INPUTS (DUT_ GROUND SENSE)						
Input Range	V_{DGS}	Relative to GNDDAC_, under the full DAC range (Note 46)	-250		+250	mV
		Relative to GNDDAC_, under the limited DAC range of -1.5V to +5.5V (Note 46)	-750		+750	mV
Input Bias Current		V_{DGS} = 0V	-10		+10	µA
Gain		Levels output	0.98	1	1.02	V/V
2.5V REFERENCE						
Nominal Voltage	V_{REF}			2.5		V
Input Bias Current			-10		10	µA
LEVEL DACS						
Settling Time		Full scale transition to within 5mV		1		µs
Differential Nonlinearity (Tested at Major Carries)		All levels not shown below; 1 LSB = 610µV			±1	mV
		$V_{LDHV\_}$, $V_{LDLV\_}$			±5	µA

Note 2: $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ levels are calibrated for gain at +0.125V and +3.875V and are calibrated for offset at +0.125V; relative to straight line between +0.125V and +3.875V.

Note 3: Change in level over operating range. Includes both gain and offset temperature effects. Simulated over entire operating range. Verified at worst-case points, which are at the endpoints $V_{DHV\_}$ - $V_{DLV\_}$ ≥ 200mV.

Note 4: Guaranteed by design and characterization.

Note 5: DATA_ = H, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, I_{OUT} = ±30mA. Nominal target value is 48Ω.

Note 6: Resistance measurements are made using ±2.5mA current changes in the loading instrument about the noted value. Absolute value of the difference in measured resistance over the specified range is tested separately for each current polarity. Test conditions are at $I_{DUT\_}$ = ±1mA, ±12mA, and ±40mA, respectively.

Note 7: Rise time of the differential inputs DATA_ and RCV_ is 150ps (10% to 90%). SC1 = SC0 = 0, 40MHz, unless otherwise noted.

Note 8: Current supplied for a minimum of 10ns. Verified to be greater than or equal to the DC drive current by design and characterization.

Note 9: $V_{DTV\_}$ = +1V, R_S = 50Ω. External signal driven into T-line to produce a 0 to +2V edge at the comparator input with a 250ps rise time (10% to 90%). Measurement point is at comparator input.

Note 10: Measured from the 90% point of the driver output (relative to its final value) to the waveform settling to within the specified limit.

Note 11: Propagation delays are measured from the crossing point of the differential input signals to the 50% point of expected output swing.

Note 12: Average of the two measurements for propagation delay, data to output (t_{LH} and t_{HL}).

Note 13: Average of the four measurements in propagation delay, drive to high-Z, and high-Z to drive (t_{LZ}, t_{HZ}, t_{ZL}, t_{ZH}). Measured from crossing point of RCV_/NRCV_ to 50% point of the output waveform.

Note 14: Four measurements are made: $V_{DHV\_}$ to high-Z, $V_{DLV\_}$ to high-Z, high-Z to $V_{DHV\_}$, and high-Z to $V_{DLV\_}$ (t_{LZ}, t_{HZ}, t_{ZL}, t_{ZH}). The worst-case difference is reported.

Note 15: Average of the four measurements in propagation delay, drive to term, and term to drive (t_{LT}, t_{HT}, t_{TL}, t_{TH}). Measured from crossing point of RCV_/NRCV_ to 50% point of the output waveform.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included. The device is tested at T_J = +70°C with an accuracy of ±15°C; specification compliance with supply and temperature variations are verified by guardbanding mean shifts of characterized data, unless otherwise noted. Temperature coefficients are measured at T_J = +40°C and +100°C, unless otherwise noted.)

Note 16: Four measurements are made: $V_{DHV\_}$ to $V_{DTV\_}$, $V_{DLV\_}$ to $V_{DTV\_}$, $V_{DTV\_}$ to $V_{DHV\_}$, and $V_{DTV\_}$ to $V_{DLV\_}$ (t_{LT}, t_{HT}, t_{TL}, t_{TH}). The worst-case difference is reported.

Note 17: Cable-droop compensation disabled. Measured as close to DUT_ as possible using a high-bandwidth cable.

Note 18: Cable-droop compensation enabled. Measured at the end of a 2m RG174 cable.

Note 19: At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at the DATA_ (input) pins.

Note 20: Maximum data rate in transitions/second. A waveform that reaches at least 95% of its programmed amplitude can be generated at one-half of this frequency.

Note 21: This specification is indicative of switching speed from $V_{DHV\_}$ or $V_{DLV\_}$ to $V_{DTV\_}$ and $V_{DTV\_}$ to $V_{DHV\_}$ or $V_{DLV\_}$ when $V_{DLV\_}$< $V_{DTV\_}$< $V_{DHV\_}$. If $V_{DTV\_}$< $V_{DLV\_}$ or $V_{DTV\_}$> $V_{DHV\_}$, the switching speed is degraded by roughly a factor of 3.

Note 22: Both high and low comparators are tested for all tests.

Note 23: Measured by using a servo to locate comparator thresholds.

Note 24: Change in offset at any voltage over operating range. Includes both gain (CMRR) and offset temperature effects. Simulated over entire operating range. Verified at worst-case points, which are at the endpoints.

Note 25: Change in offset voltage over input range.

Note 26: $V_{CHV\_}$ and $V_{CLV\_}$ levels are calibrated for gain at +0.125V and +3.875V and are calibrated for offset at +2V. Relative to straight line between +0.125V and +3.875V.

Note 27: Change in offset voltage with power supplies independently varied over their full range. Both high and low comparators are tested.

Note 28: All propagation delays are measured from the $V_{DUT\_}$ crossing to the differential output crossing.

Note 29: Characterization is done with 50Ω to ground at the end of a transmission line with a round-trip delay greater than 4ns.

Note 30: 40MHz, 0 to +1V input to comparator, V_{CX} reference = +0.5V, 50% duty cycle, 250ps rise/fall time, Z_S = 50Ω, Driver in term mode with $V_{DTV\_}$ = +0.5V, unless otherwise noted. Hysteresis is disabled.

Note 31: Input rise/fall time = 150ps. Cable-droop compensation disabled.

Note 32: Input rise/fall time = 150ps. Cable-droop compensation enabled. Signal applied at beginning of 2m RG174 cable with compensation tuned for the cable.

Note 33: Input rise/fall time = 150ps. Cable-droop compensation enabled. Signal applied at beginning of 2m RG174 cable with compensation tuned for the cable. Tested with both +1V and +5V input swings.

Note 34: At this pulse width, the output reaches at least 90% of its nominal peak-to-peak swing. The pulse width is measured at the crossing points of the differential outputs. 250ps rise/fall time.

Note 35: $V_{DUT\_}$ = 200mV_{P-P}, rise/fall time = 150ps, overdrive = 100mV, $V_{DTV\_}$ = V_{CM}.

Note 36: Input rise/fall time = 250ps. Cable-droop compensation disabled.

Note 37: Input to comparator is 40MHz at 0 to +1V, 50% duty cycle, 1ns rise/fall time.

Note 38: Unless otherwise noted, comparator outputs are terminated with 50Ω to +1.2V and CTV_ = +1.2V.

Note 39: The min/max value of CTV_ specifications are guaranteed by simulation.

Note 40: This specification is implicitly tested by meeting the high-impedance leakage specification $I_{DUT\_}$ ($V_{CLV\_}$ = $V_{CHV\_}$ = +6V, $V_{DUT\_}$ = +2V), and $I_{DUT\_}$ ($V_{CLV\_}$ = $V_{CHV\_}$ = -2V, $V_{DUT\_}$ = +6V).

Note 41: Change in level over operating range. Includes both gain and offset temperature effects. Simulated over entire operating range. Verified at worst-case points.

Note 42: Resistance measurements are made using ±2.5mA current changes in the loading instrument about the noted value Absolute value of the difference in measured resistance over the specified range, tested separately for each current polarity.

Note 43: Ripple in the DUT_ signal after one round-trip delay. Stimulus is 0 to +3V, +2.5V/ns square wave from far end of 3ns transmission line with R_S = 25Ω, clamps set to 0 and +3V.

Note 44: Verified by dead-band test.

Note 45: Typical values are at V_{CC} = +9.25V, V_{EE} = -5.25V. Production tests are performed with worst-case supply conditions for each specification. Supply conditions are either min V_{CC} and max V_{EE}, or max V_{CC} and min V_{EE}. Some tests may require both conditions.

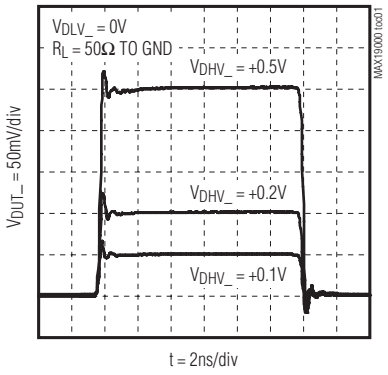
Note 46: Increasing DGS beyond 0V requires a proportional increase in the minimum supply levels. Specified ranges for all levels except $V_{LDHV\_}$, $V_{LDLV\_}$ are defined with respect to DGS.

Dual DCL with Integrated Level Setters

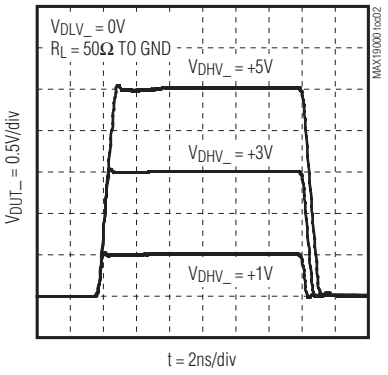
Typical Operating Characteristics

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included, T_J = +70°C, temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.)

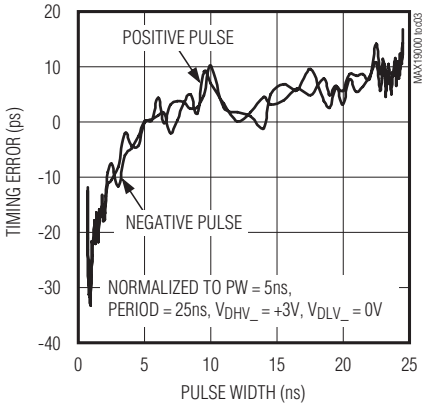
DRIVER SMALL-SIGNAL RESPONSE



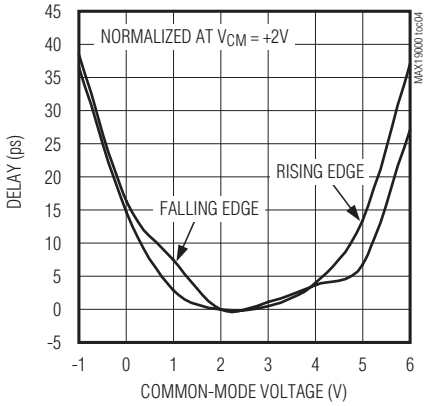
DRIVER LARGE-SIGNAL RESPONSE



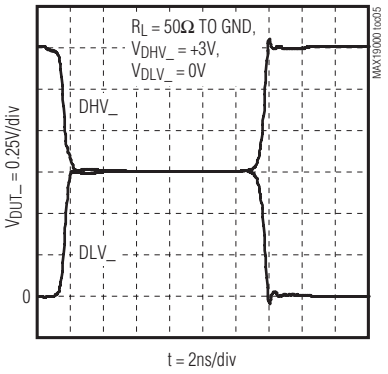
DRIVER TRAILING-EDGE ERROR vs. PULSE WIDTH



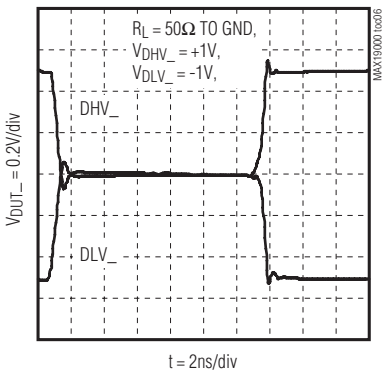
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



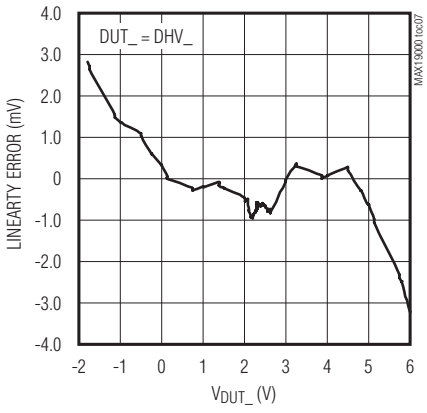
DRIVER-TO-TERM TRANSITION



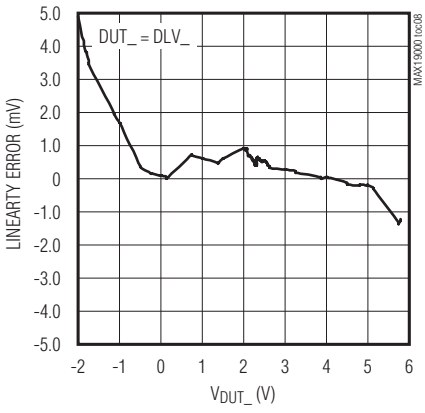
DRIVER-TO-HIGH-IMPEDANCE TRANSITION



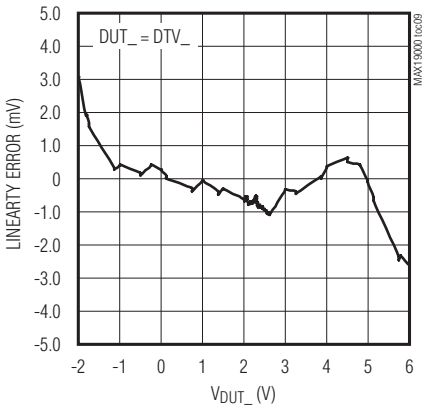
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



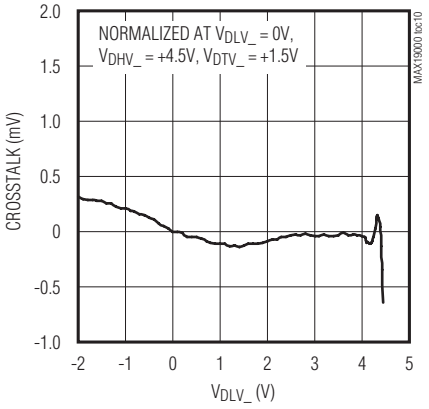
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



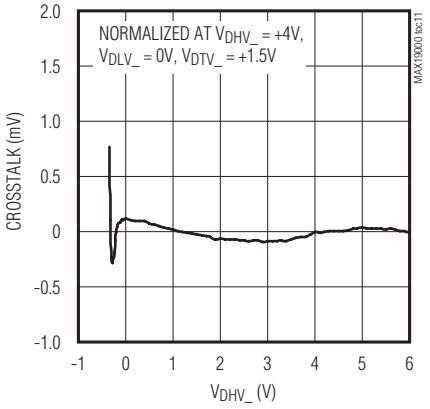
Typical Operating Characteristics (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included, T_J = +70°C, temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.)

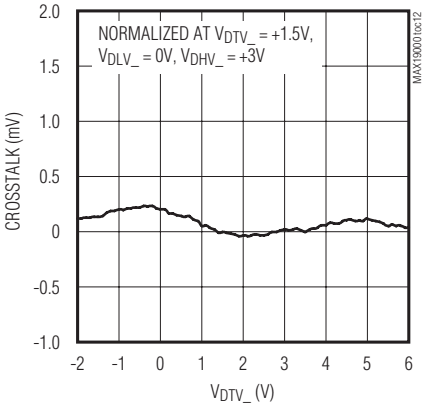
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



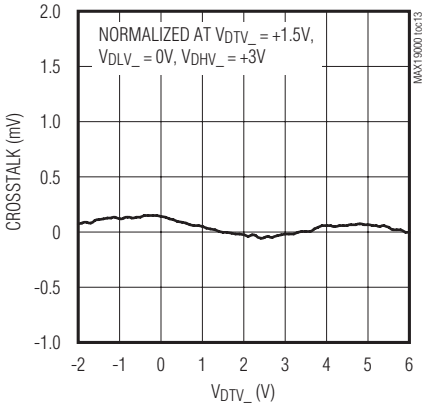
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_



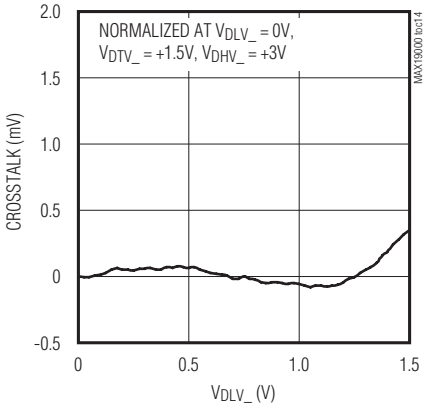
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



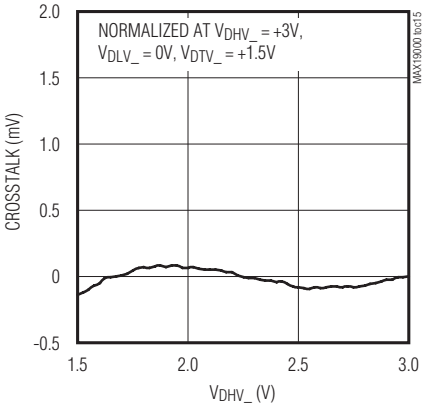
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



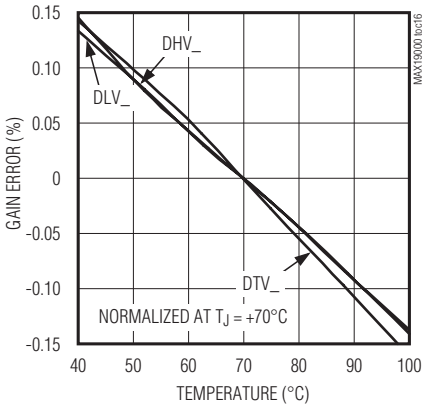
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



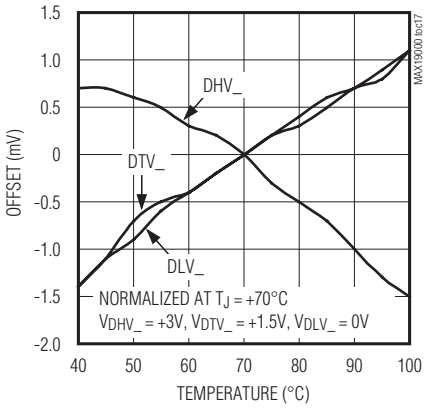
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



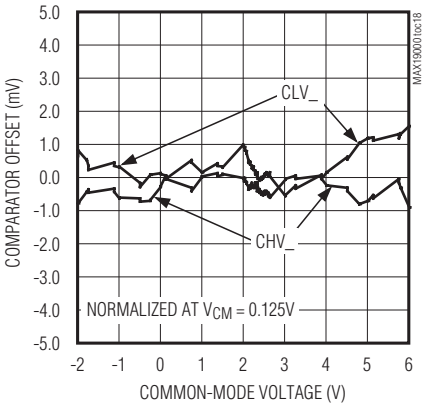
DRIVER GAIN ERROR vs. TEMPERATURE



DRIVER OFFSET vs. TEMPERATURE



COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE

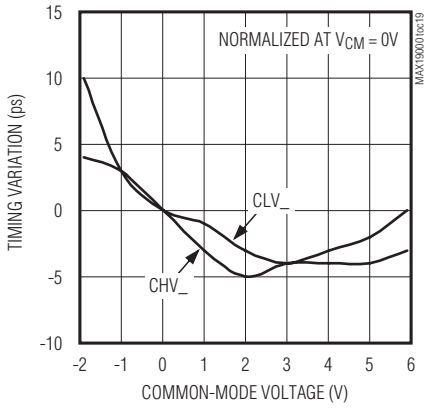


Dual DCL with Integrated Level Setters

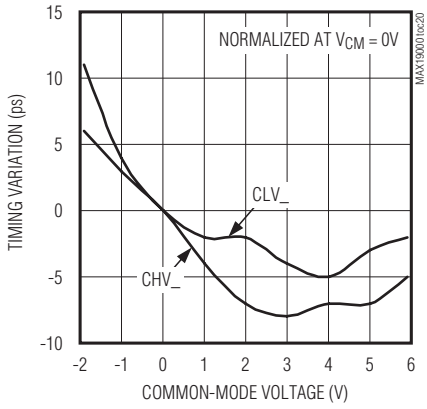
Typical Operating Characteristics (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included, T_J = +70°C, temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.)

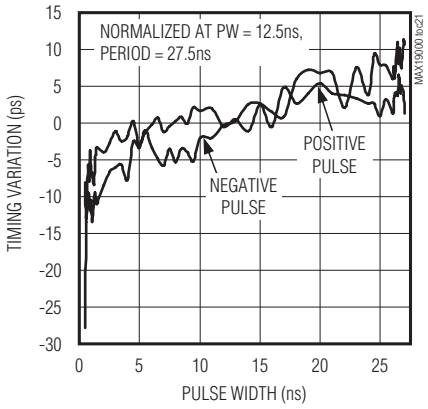
COMPARATOR RISING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE



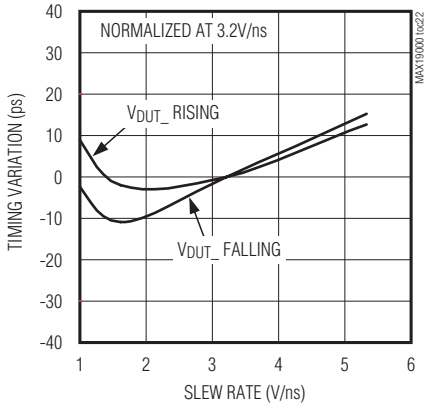
COMPARATOR FALLING-EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE



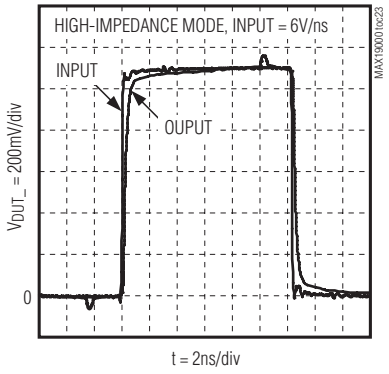
COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



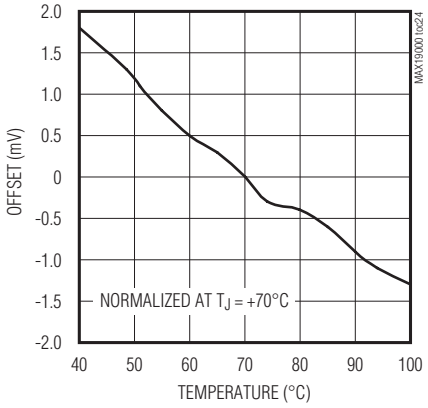
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE



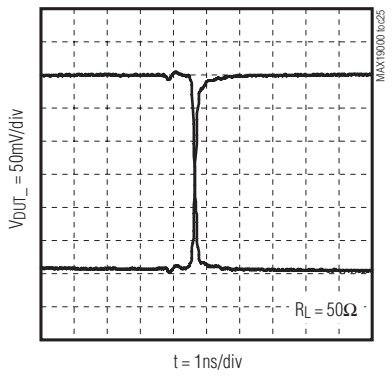
COMPARATOR RESPONSE TO HIGH SLEW-RATE OVERDRIVE



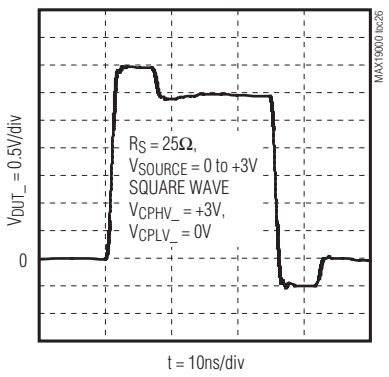
COMPARATOR OFFSET vs. TEMPERATURE



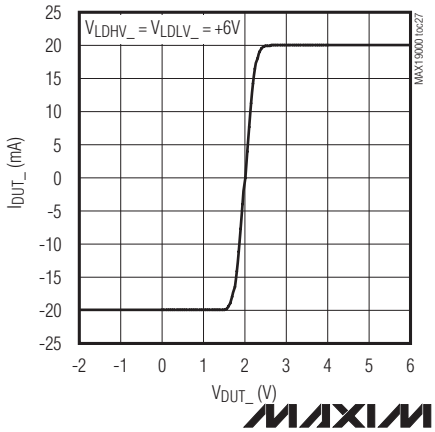
COMPARATOR DIFFERENTIAL OUTPUT REPONSE



CLAMP RESPONSE AT COMPARATOR INPUT



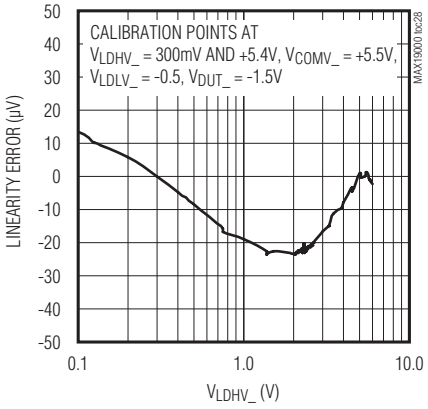
ACTIVE LOAD CURRENT vs. VOLTAGE



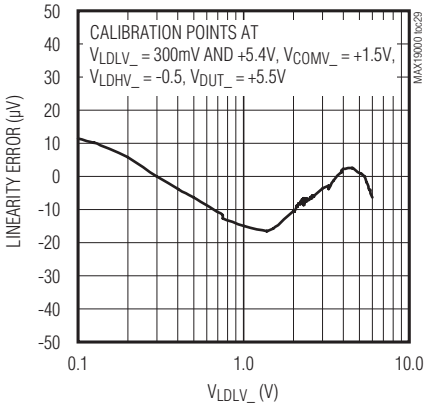
Typical Operating Characteristics (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included, T_J = +70°C, temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.)

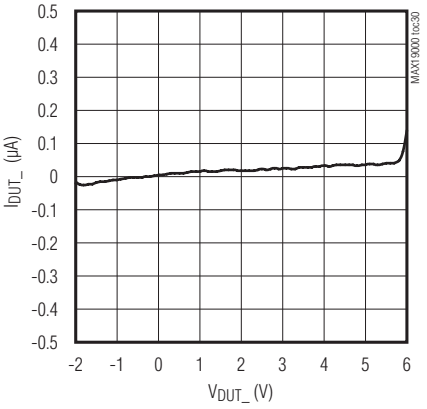
ACTIVE-LOAD LINEARITY ERROR
$I_{DUT\_}$ vs. $V_{LDHV\_}$



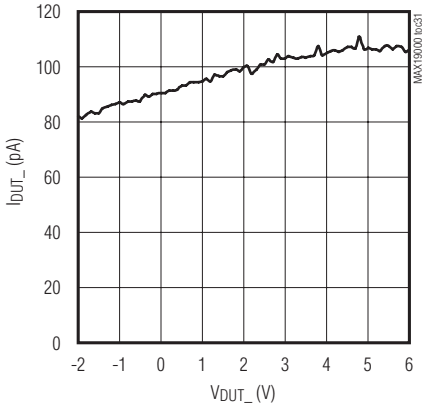
ACTIVE-LOAD LINEARITY ERROR
$I_{DUT\_}$ vs. $V_{LDLV\_}$



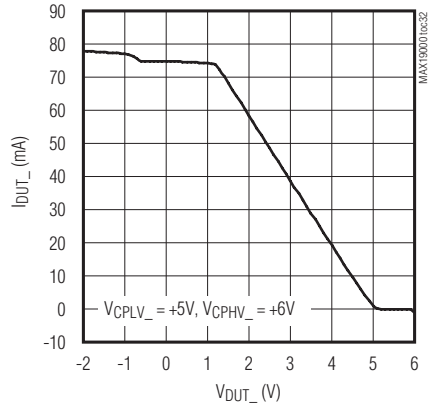
HIGH-IMPEDANCE LEAKAGE CURRENT
vs. DUT_ VOLTAGE



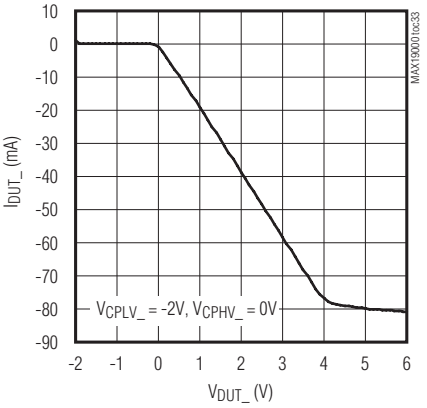
LOW-LEAKAGE CURRENT
vs. DUT_ VOLTAGE



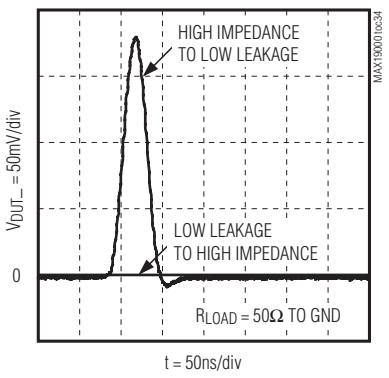
HIGH-IMPEDANCE CLAMP CURRENT
vs. DIFFERENCE VOLTAGE



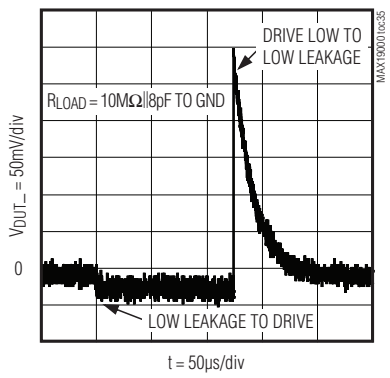
HIGH-IMPEDANCE CLAMP CURRENT
vs. DIFFERENCE VOLTAGE



HIGH IMPEDANCE TO LOW-LEAKAGE TRANSITION



DRIVE LOW TO LOW-LEAKAGE TRANSITION

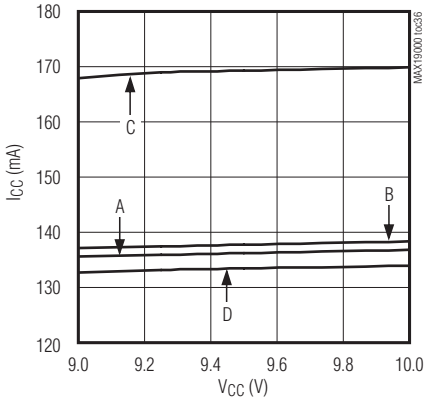


Dual DCL with Integrated Level Setters

Typical Operating Characteristics (continued)

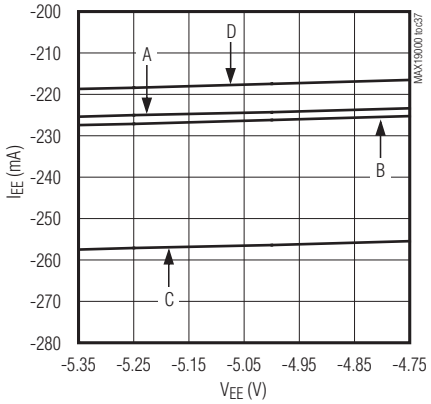
(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included, T_J = +70°C, temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.)

SUPPLY CURRENT
I_{CC} vs. V_{CC}



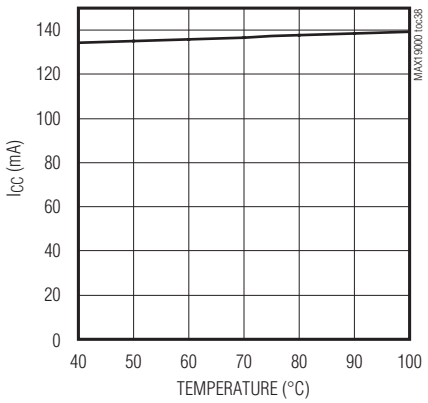
A: $V_{DUT\_}$ = $V_{DTV\_}$ = +1.5V, CHV_ = CLV_ = 0, I_{SRC} = I_{SNK} = 0, R_L = 100kΩ, C_L = 0.5pF.
B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED.
C: SAME AS B EXCEPT I_{SRC} = I_{SNK} = 20mA.
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED.

SUPPLY CURRENT
I_{EE} vs. V_{EE}



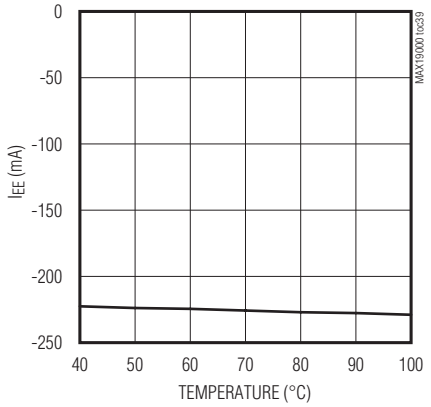
A: $V_{DUT\_}$ = $V_{DTV\_}$ = +1.5V, CHV_ = CLV_ = 0, I_{SRC} = I_{SNK} = 0, R_L = 10kΩ, C_L = 0.5pF.
B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED.
C: SAME AS B EXCEPT I_{SRC} = I_{SNK} = 20mA.
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED.

SUPPLY CURRENT
I_{CC} vs. TEMPERATURE



$V_{DUT\_}$ = $V_{DTV\_}$ = +1.5V, CHV_ = CLV_ = 0, DRIVER TERM MODE, NO LOAD.

SUPPLY CURRENT
I_{EE} vs. TEMPERATURE

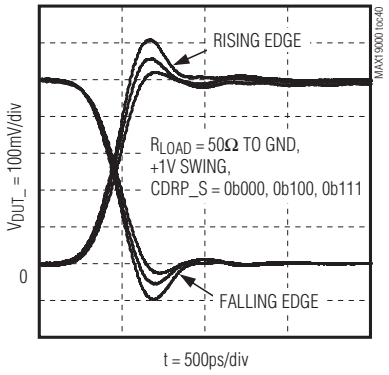


$V_{DUT\_}$ = $V_{DTV\_}$ = +1.5V, CHV_ = CLV_ = 0, DRIVER TERM MODE, NO LOAD.

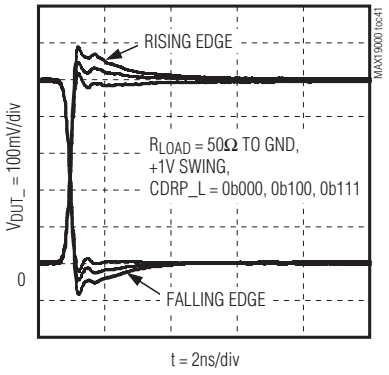
Typical Operating Characteristics (continued)

(V_{CC} = +9.25V, V_{EE} = -5.25V, V_{DD} = +3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = +1.5V, $V_{CHV\_}$ = +2V, $V_{CLV\_}$ = +1V, $V_{CPHV\_}$ = +6.7V, $V_{CPLV\_}$ = -2.7V, $V_{COMV\_}$ = +2.5V, $V_{LDHV\_}$ = 0V, $V_{LDLV\_}$ = 0V, $V_{CTV\_}$ = +1.2V, CDRP_ = 000b, RO_ = 1100b, HYST_ = 000b, SC_ = 00b, V_{DGS} = V_{GND} = V_{GNDDAC} = 0V, specifications apply after calibration, level-setter errors included, T_J = +70°C, temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.)

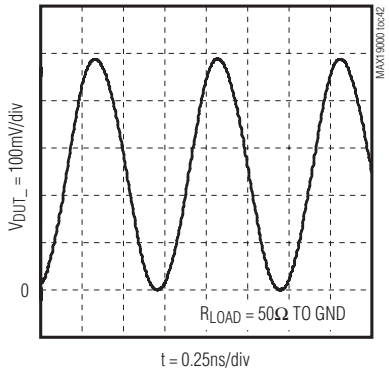
DRIVER CABLE-DROOP COMPENSATION SHORT TIME



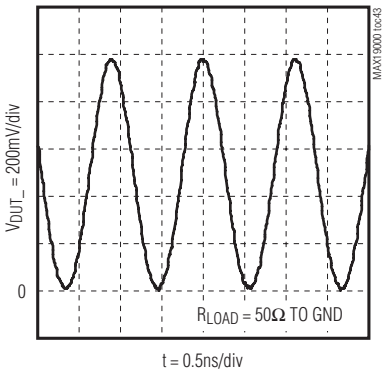
DRIVER CABLE-DROOP COMPENSATION LONG TIME



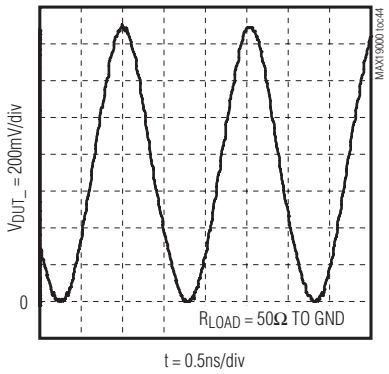
DRIVER 2700Mbps TOGGLE RATE, +1V



DRIVER 1800Mbps TOGGLE RATE, +2V

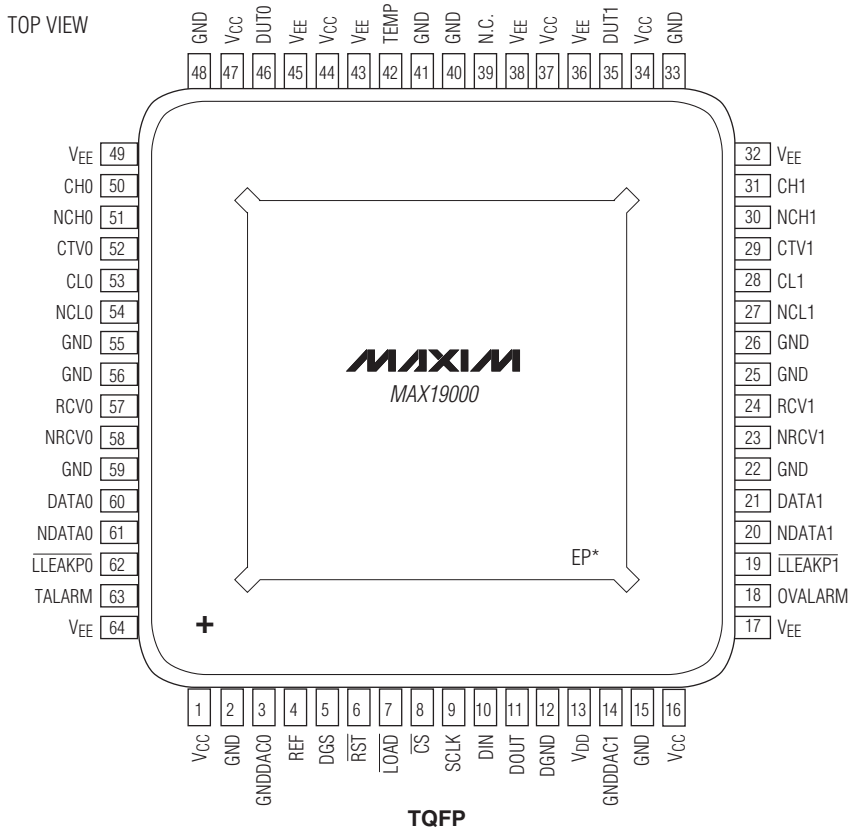


DRIVER 1300Mbps TOGGLE RATE, +3V



Dual DCL with Integrated Level Setters

Pin Configuration



TQFP

*EP = EXPOSED PAD ON PACKAGE TOP.

Pin Description

PIN	NAME	FUNCTION
1, 16, 34, 37 44, 47	V_{CC}	Positive Power Supply
2, 15, 26, 33, 40, 41, 48, 55	GND	Analog Ground
3	GNDDAC0	Channel 0 DAC Ground Input
4	REF	DAC 2.5V Reference Input. Set REF with respect to GNDDAC_.
5	DGS	DUT Ground Sense Input
6	$\overline{RST}$	Active-Low Serial-Port Reset Input
7	$\overline{LOAD}$	Active-Low Serial-Port Load Input
8	$\overline{CS}$	Active-Low Serial-Port Chip-Select Input
9	SCLK	Serial-Port Clock Input
10	DIN	Serial-Port Data Input
11	DOUT	Serial-Port Data Output

Pin Description (continued)

PIN	NAME	FUNCTION
12	DGND	Digital Ground
13	V_{DD}	Logic Power Supply
14	GNDDAC1	Channel 1 DAC Ground Input
17, 32, 36, 38, 43, 45, 49, 64	V_{EE}	Negative Power Supply
18	OVALARM	Overvoltage Alarm Output
19	$\overline{\text{LLEAKP1}}$	Active-Low Channel 1 Low-Leak Control Input
20	NDATA1	Channel 1 Data Input Complement
21	DATA1	Channel 1 Data Input
22, 25, 56, 59	GND	Connect to Ground
23	NRCV1	Channel 1 Receive Input Complement
24	RCV1	Channel 1 Receive Input
27	NCL1	Channel 1 Low Comparator Output Complement
28	CL1	Channel 1 Low Comparator Output
29	CTV1	Channel 1 Comparator Termination Voltage Input
30	NCH1	Channel 1 High Comparator Output Complement
31	CH1	Channel 1 High Comparator Output
35	DUT1	Channel 1 Input/Output
39	N.C.	No Connection. Not Internally Connected. Leave unconnected or connect to GND.
42	TEMP	Temperature Sensor Output
46	DUT0	Channel 0 Input/Output
50	CH0	Channel 0 High Comparator Output
51	NCH0	Channel 0 High Comparator Output Complement
52	CTV0	Channel 0 Comparator Termination
53	CL0	Channel 0 Low Comparator Output
54	NCL0	Channel 0 Low Comparator Output Complement
57	RCV0	Channel 0 Receive Input
58	NRCV0	Channel 0 Receive Input Complement
60	DATA0	Channel 0 Data Input
61	NDATA0	Channel 0 Data Input Complement
62	$\overline{\text{LLEAKP0}}$	Active-Low Channel 0 Low-Leak Control Input
63	TALARM	Temperature Alarm Output
—	EP	Exposed Pad. EP is internally connected to V_{EE}. Connect externally to V_{EE} or leave unconnected. Do not use EP as a primary connection to V_{EE}.

Dual DCL with Integrated Level Setters

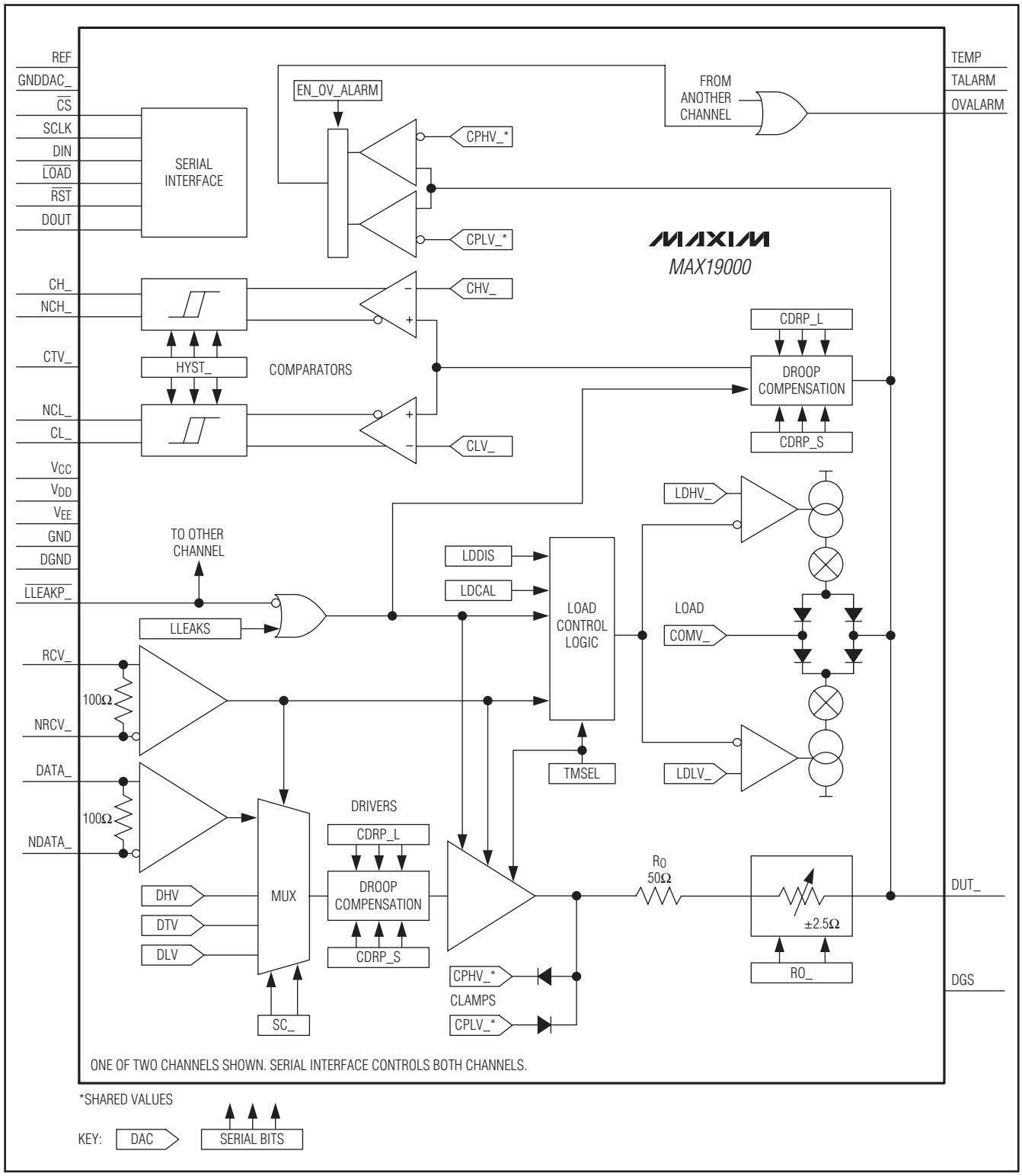


Figure 1. Simplified Block Diagram (only one of two channels is shown; the single serial interface controls both channels)

Detailed Description

The MAX19000 dual-channel, pin-electronics DCL integrates multiple pin-electronics functions into a single IC. Each channel includes a three-level pin driver, a window comparator, dynamic clamps, an active load, and 10 independent 14-bit level-setting DACs. Additionally, each channel of the MAX19000 features programmable cable-droop compensation for the driver output and for the comparator input, adjustable driver output resistance, and driver slew-rate adjustment.

The MAX19000 driver features a wide -2V to +6V high-speed operating range, high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The driver provides high-speed differential control inputs compatible with most high-speed logic families. The window comparators provide extremely low timing variation over changes in slew rate, pulse width, or overdrive voltage, and provide 50Ω source outputs internally terminated to an applied voltage at CTV_. When high-impedance mode is selected, the programmable dynamic clamps provide damping of high-speed DUT_ waveforms. The 20mA active load facilitates fast contact testing when used in conjunction with the comparators, and functions as a pullup for open-drain/collector DUT_ outputs. Placing the MAX19000 DUT_ output into a very low-leakage state disables the DCL functions. This feature is convenient for making IDDQ measurements without the need for an output disconnect relay. Low-leakage control is independent for each channel. An SPI™-compatible serial interface and external inputs configure the MAX19000.

Integrated PE Mode Selection

The MAX19000 features two modes of operation, active and low leakage. The MAX19000 enters low-leakage mode when either $\overline{\text{LLEAKP\_}}$ is driven low or the LLEAKS bit is set to 1. Driving $\overline{\text{LLEAKP\_}}$ to 0 immediately forces the DCL to low leakage.

The serial bit LLEAKS = 1 can be used to force the DCL to low-leakage mode independent of other DCL control bits. Driving LLEAKS to 0 is necessary to allow any other mode of the DCL (Table 1).

Driver

The driver uses a high-speed multiplexer to select one of three DAC voltages ($V_{DHV\_}$, $V_{DLV\_}$, or $V_{DTV\_}$) or to select high-impedance mode. Multiplexer switching is controlled by high-speed differential inputs DATA_/NDATA_ and RCV_/NRCV_ and mode-control bit TMSEL (see Table 2). The multiplexer output is buffered to drive DUT_. A programmable slew-rate circuit controls the slew rate of the buffer output.

In high-impedance mode, the clamps and comparators remain connected to DUT_, the DUT_ bias current is less than ±2µA, and the node continues to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than ±10nA, and signal tracking slows.

The nominal driver output resistance is 50Ω and features an adjustment range of ±2.5Ω through the serial interface in 360mΩ increments.

Driver Slew-Rate Control

A slew-rate circuit controls the slew rate of the buffer output. Select one of four possible slew rates according to Table 3. The speed of the internal multiplexer sets the 100% driver slew rate (see the "Driver Large-Signal Response" graph in the *Typical Operating Characteristics* section). SC1 and SC0 are set to 0 at power-up or when $\overline{\text{RST}}$ is forced low.

Driver Cable-Droop Compensation

The driver incorporates programmable active cable-droop compensation. At high frequencies, transmission-

Table 1. DCL Mode Control

$\overline{\text{LLEAKP\_}}$	LLEAKS	DRIVER	COMP	LOAD
0	0	Low leakage	Low leakage	Low leakage
0	1	Low leakage	Low leakage	Low leakage
1	0	Active	Active	Active
1	1	Low leakage	Low leakage	Low leakage

Table 2. Driver Functional Overview

TMSEL	RCV_	DATA_	DRIVER OUTPUT
X	0	0	Drive to $V_{DLV\_}$
X	0	1	Drive to $V_{DHV\_}$
0	1	X	High-Z receive
1	1	X	Drive to $V_{DTV\_}$

X = Don't care.

Table 3. Driver Slew-Rate Control

SC1	SC0	DRIVER SLEW RATE (%)
0	0	100
0	1	75
1	0	50
1	1	25

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Dual DCL with Integrated Level Setters

line effects from the tester signal delivery path (PCB trace, connectors, and cabling between the MAX19000 DUT_ output and the device under test itself) can degrade the output waveform fidelity at the DUT_, resulting in a highly degraded or unusable signal. The compensation circuit reduces this degradation by adding a double time-constant decaying waveform to the nominal output waveform (preemphasis). Figure 2 depicts a comparison between a typical driver and the MAX19000, and shows how droop compensation counters signal degradation. There are long-time-constant control bits and short-time-constant control bits in the DCL calibration registers to set the amount of compensation. Control bits CDRP_[2:0] vary the amplitude of the compensation signal. Table 4 shows the percent compensation as a function of control bit settings. The default power-on reset (POR) value is 000 for zero compensation.

Adjustable Driver Output Impedance (ΔR_O)

The MAX19000 driver output impedance is adjustable to ±2.5Ω with a 360mΩ resolution. The RO bits in the DCL calibration register set the impedance value. Table 5 presents the output resistance control logic. The output resistance is set to R_O + 0.0Ω (0b1000) at power-up.

Driver Voltage Clamps

The voltage clamps (high and low) limit the voltage at DUT_ and suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers (Figure 1). Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using the level-setting DACs (CPHV_ and CPLV_). The driver clamps are enabled only when the driver is in the high-impedance mode. For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT_ voltage range. The optimal clamp voltages are application-specific and must be empirically determined. Set the clamp voltages at a minimum of +0.7V outside the expected DUT_ voltage range when not using the clamps. Overvoltage protection then remains active without loading DUT_.

High-Speed Comparators

The MAX19000 provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (Figure 3). Cable-droop compensation is present on both channels. The comparators act as a high-speed window comparator. DAC voltages CHV_ and CLV_ control the comparator thresholds. Table 6 shows the truth table for the comparators. Figure 3 shows the comparator block diagram.

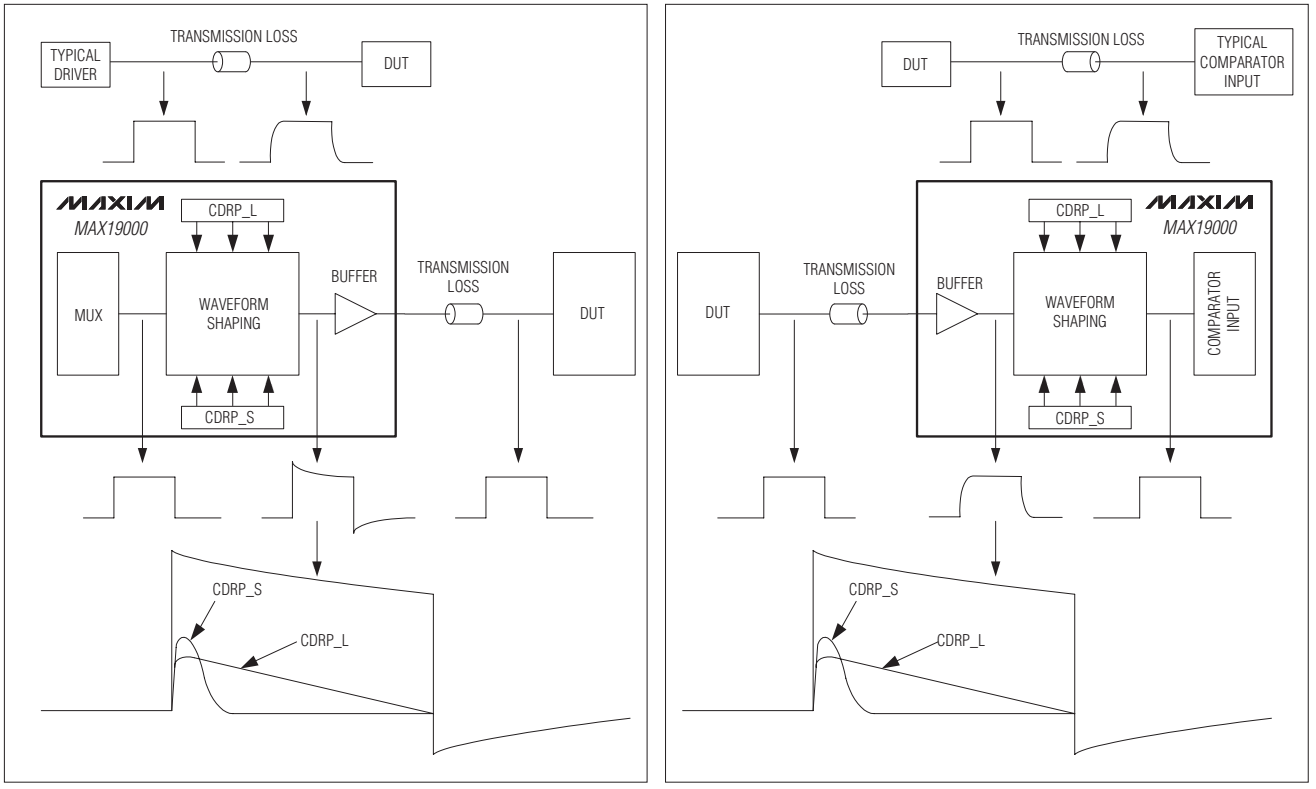
This configuration switches a 12mA current source between the two outputs, and each output provides an internal termination resistor connected to CTV_. These resistors are typically 50Ω. Use alternate configurations to terminate different path impedance provided that the absolute maximum ratings are not exceeded. Note that the resistor value also sets the voltage swing. The output provides a nominal 300mV_{P-P} swing with a 100Ω differential load termination and a 50Ω source termination. See the *Logic Outputs CH_, NCH_, CL_, NCL_* parameters in the *Electrical Characteristics* table for definition of the V_{OH} voltage.

Table 4. Driver and Comparator Cable-Droop Compensation Control Logic

CDRP_2	CDRP_1	CDRP_0	DROOP COMPENSATION (%)
0	0	0	0
0	0	1	3
0	1	0	6
0	1	1	9
1	0	0	11
1	0	1	14
1	1	0	17
1	1	1	20

Table 5. Driver Delta R_O Control

RO3	RO2	RO1	RO0	DRIVER OUTPUT RESISTANCE (Ω)
0	0	0	0	R_O - 2.88
0	0	0	1	R_O - 2.52
0	0	1	0	R_O - 2.16
0	0	1	1	R_O - 1.80
0	1	0	0	R_O - 1.44
0	1	0	1	R_O - 1.08
0	1	1	0	R_O - 0.72
0	1	1	1	R_O - 0.36
1	0	0	0	R_O + 0.0
1	0	0	1	R_O + 0.36
1	0	1	0	R_O + 0.72
1	0	1	1	R_O + 1.08
1	1	0	0	R_O + 1.44
1	1	0	1	R_O + 1.80
1	1	1	0	R_O + 2.16
1	1	1	1	R_O + 2.52



NOTE: THE MAXIMUM AC SWING WHILE MAINTAINING LINEAR COMPENSATION OF DRIVER CABLE DROOP IS 4.4V_{P-P}.
THE MAXIMUM AC SWING WHILE MAINTAINING LINEAR COMPENSATION OF COMPARATOR CABLE DROOP IS 3V_{P-P}.

Figure 2. Driver/Comparator Cable-Droop Compensation

Table 6. Comparator Truth Table

CONDITION		CH_	CL_
$V_{DUT\_} < V_{CHV\_}$	$V_{DUT\_} < V_{CLV\_}$	0	0
$V_{DUT\_} < V_{CHV\_}$	$V_{DUT\_} > V_{CLV\_}$	0	1
$V_{DUT\_} > V_{CHV\_}$	$V_{DUT\_} < V_{CLV\_}$	1	0
$V_{DUT\_} > V_{CHV\_}$	$V_{DUT\_} > V_{CLV\_}$	1	1

Table 7. Comparator Hysteresis Control

HYST2	HYST1	HYST0	COMPARATOR HYSTERESIS (mV)
0	0	0	0
0	0	1	2
0	1	0	4
0	1	1	6
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	15

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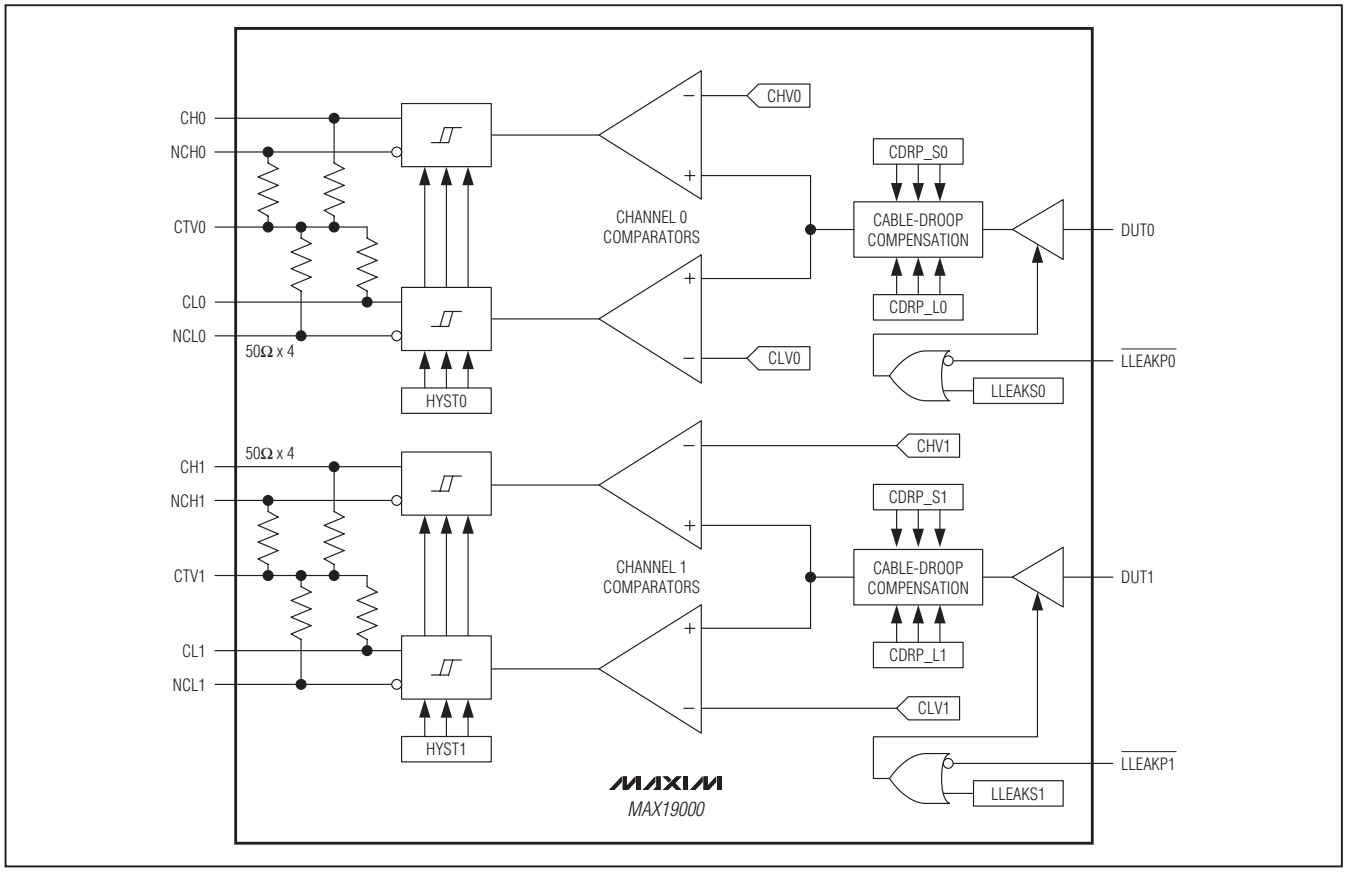

Figure 3. High-Speed Comparators Block Diagram

Comparator Hysteresis

The DCL register controls the high-speed comparator hysteresis. The HYST[2:0] bits of that register select one of eight values (0mV, 2mV, 4mV, 6mV, 8mV, 10mV, 12mV, or 15mV).

The HYST[2:0] bits are set to 0b000 at power-up or when $\overline{RST}$ is forced low. Table 7 shows the HYST[2:0] bit functions.

Comparator Cable-Droop Compensation

Comparator cable-droop compensation works the same as driver cable-droop compensation. See the *Driver Cable-Droop Compensation* section for a description.

Active Load

The active load is a linearly programmable current source and sink, a commutation buffer, and a diode bridge (Figure 4). Level-setting DACs LDHV_ and LDLV_ set the sink and source currents from 0mA to 20mA. Level-setting DAC COMV_ sets the commutation buffer output voltage. The source and sink naming convention is referenced to the MAX19000, so current out of the MAX19000 constitutes source current and current into the MAX19000 constitutes sink current.

The programmed source current loads the device under test when $V_{DUT\_} < V_{COMV\_}$. The programmed sink current loads the device under test when $V_{DUT\_} > V_{COMV\_}$. The high-speed differential inputs (RCV_/NRCV_) and three bits of the control word (LDDIS, LDCAL, and TMSEL) control the load. $\overline{LLEAKP\_}$ and LLEAKS place the load into low-leakage mode. The low-leakage controls override other controls. Table 8 details load control logic.

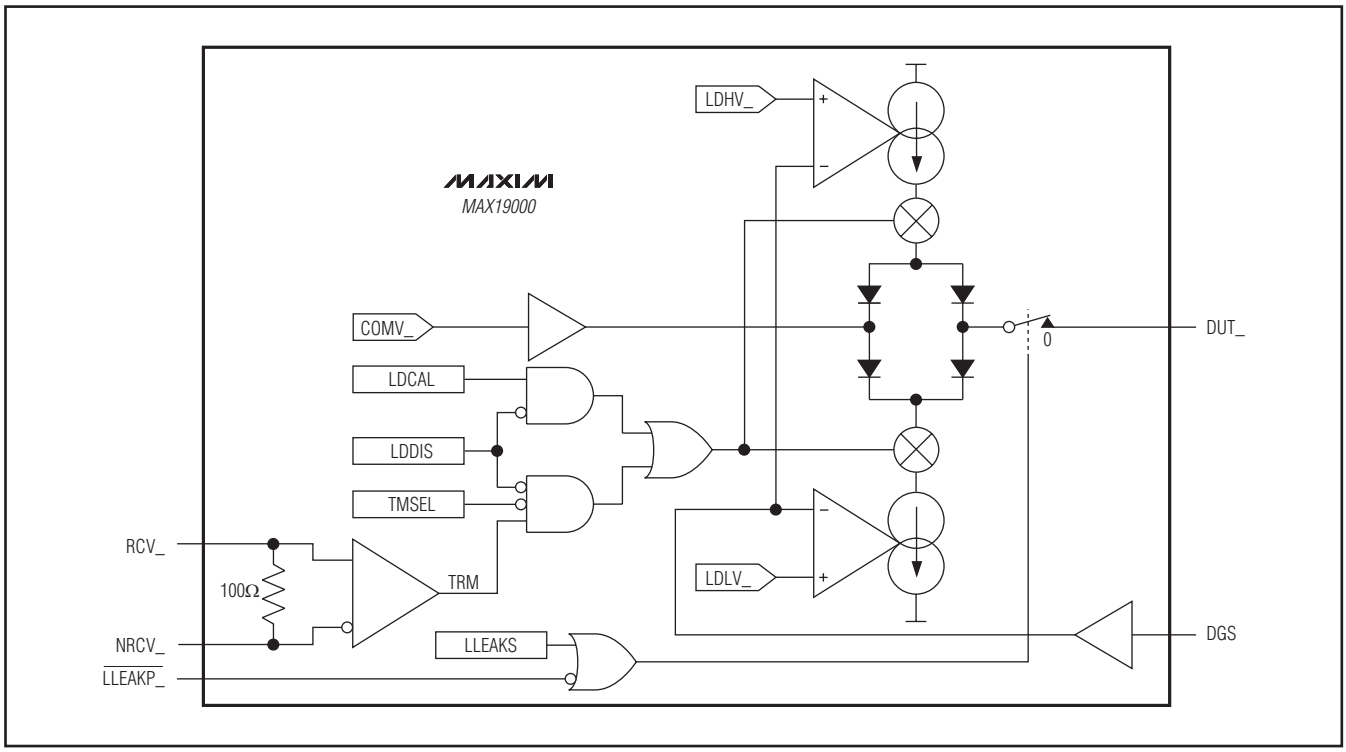

Figure 4. Active Load Block Diagram (One Channel Shown)

Table 8. Active Load Control

RCV_	TMSEL	LDDIS	LDCAL	LEAK*	LOAD STATE
X	X	X	X	1	Low leakage
0	X	0	0	0	Off
X	X	1	X	0	Off
1	1	0	0	0	Off
1	0	0	0	0	On
X	X	0	1	0	On

X = Don't care.

**LEAK = LLEAKS + ($\overline{LLEAKP\_}$)*

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Load Calibration Enable (LDCAL)

LDCAL allows the load and driver to be simultaneously enabled for diagnostic purposes. LDDIS overrides LDCAL.

Serial Interface

An SPI-compatible serial interface controls the MAX19000. The serial interface, detailed in Figure 5, operates with clock speeds up to 50MHz and includes the $\overline{CS}$, SCLK, DIN, $\overline{RST}$, $\overline{LOAD}$, and DOUT signals. Serial-interface timing is shown in Figure 8 and timing specifications are detailed in the *Electrical Characteristics* table.

Loading Data Into the MAX19000

Load data into the 24-bit shift register from DIN on the rising edge of SCLK, while $\overline{CS}$ is low (Figure 5). Enter the address and data bits in order from MSB to LSB. The MAX19000 is updated when the control and level-setting data are latched into the control and level-setting registers. The control and level-setting registers are separated from the shift register by the input and channel-select registers. Two methods allow data to transfer from the shift register to the control and level-setting registers, depending on the state of external digital input $\overline{LOAD}$.

Holding $\overline{LOAD}$ high during the rising edge of $\overline{CS}$ allows the shift register data to transfer only into the input and channel-select registers. Force $\overline{LOAD}$ low to transfer the data into the control and level-setting registers. Changes update on the falling edge of $\overline{LOAD}$, which allows preloading of data and facilitates synchronizing updates across multiple devices.

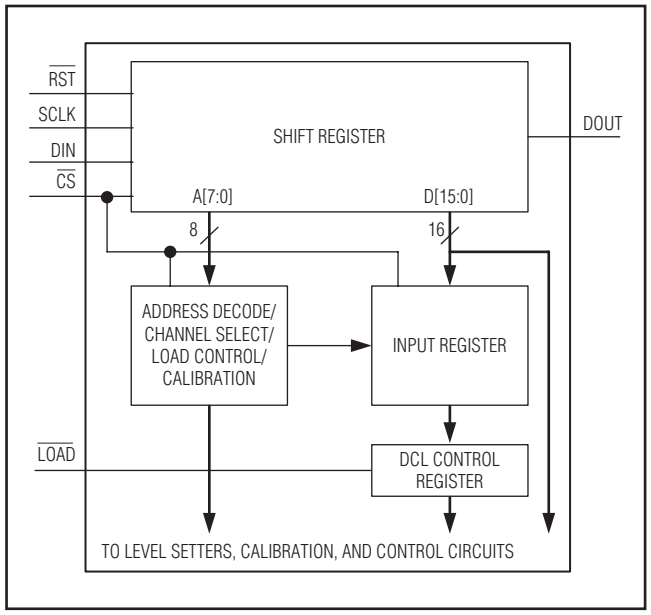

Figure 5. Serial-Interface Block Diagram

Holding $\overline{LOAD}$ low during the rising edge of $\overline{CS}$ forces the input and channel-select registers to become transparent and all data transfers through these registers directly to the control and level-setting registers. Changes update on the rising edge of $\overline{CS}$. Figures 6 and 7 show how $\overline{LOAD}$ and $\overline{CS}$ function, and also the data configuration of SCLK, DIN, and DOUT. The calibration registers change on the rising edge of $\overline{CS}$, regardless of the state of $\overline{LOAD}$.

Serial-Port Timing

Timing and arrangement of the serial-port signals is shown in Figures 6, 7, and 8.

Serial-Interface DOUT

DOUT is a buffered version of the last bit in the serial-interface shift register. The complete contents of the shift register can be read at DOUT during the next write cycle. To shift data out without modifying any registers, perform a write with address bits A4 = A5 = A6 = 1. Use DOUT to daisy-chain multiple devices and/or to verify that data was properly shifted in during the previous write cycle.

Data is shifted in to the shift register on the rising edge of the SCLK, when $\overline{CS}$ is low. The shift register is 24 bits long.

Device Control

Control and level-setting registers are selected to receive data based on the channel and mode-select bits (A[7:0]). Tables 9 and 10 present the control register bits and functions. Level-setting DAC data and control register data are contained in the 16 data bits D[15:0]. Tables 9, 10, and 11 detail the bit functions. Clock in bit A7 first and bit D0 last, as shown in Figure 8.

Bit A7 allows access to the DAC calibration registers. Use the calibration registers to adjust the gain and offset of each DAC. Set bit A7 to write to the calibration registers. See the *Level-Setter DAC and Calibration Addresses* section for more information.

Table 9. Serial-Interface Control Bits

DIN	FUNCTION
A7	Calibration register write
A6*	Broadcast enable
A[5:4]	Channel address
A[3:0]	Register address
D[15:0]	Register data

**Asserting the broadcast enable bit (A6) overrides the settings of bits A[5:4]; all channels are written to when bit A6 is set high.*

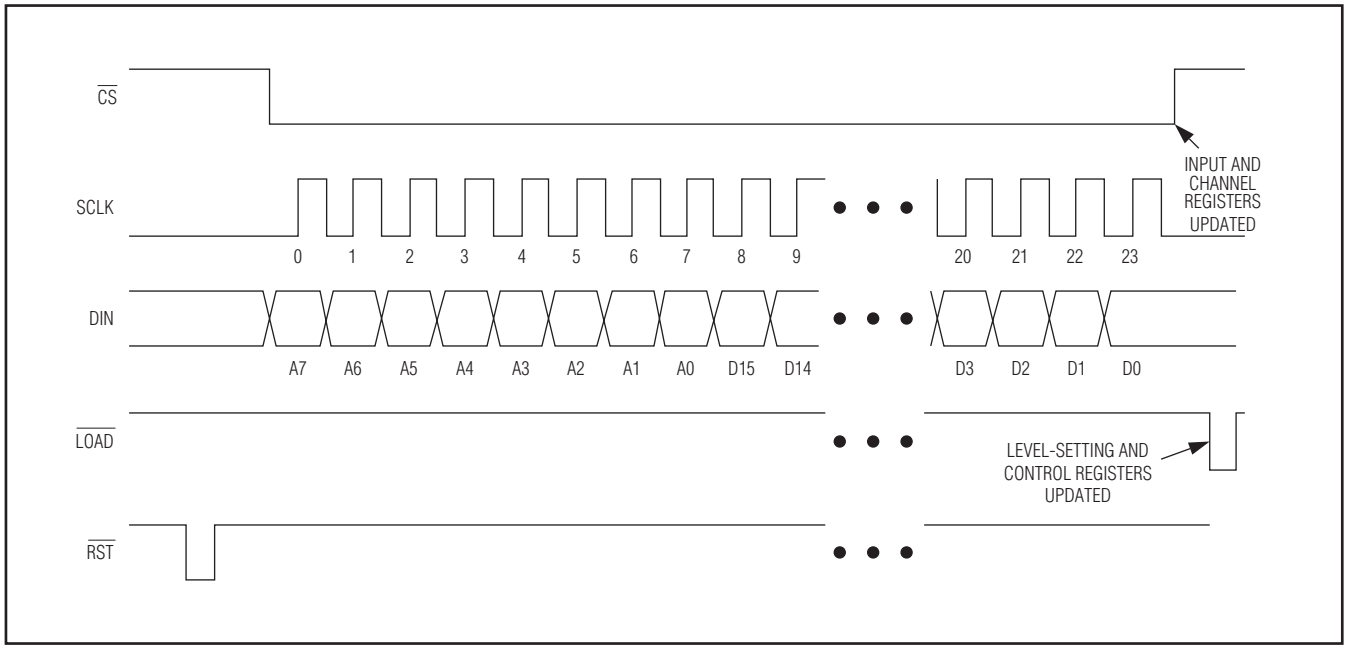

Figure 6. Serial-Port Timing with Asynchronous Load

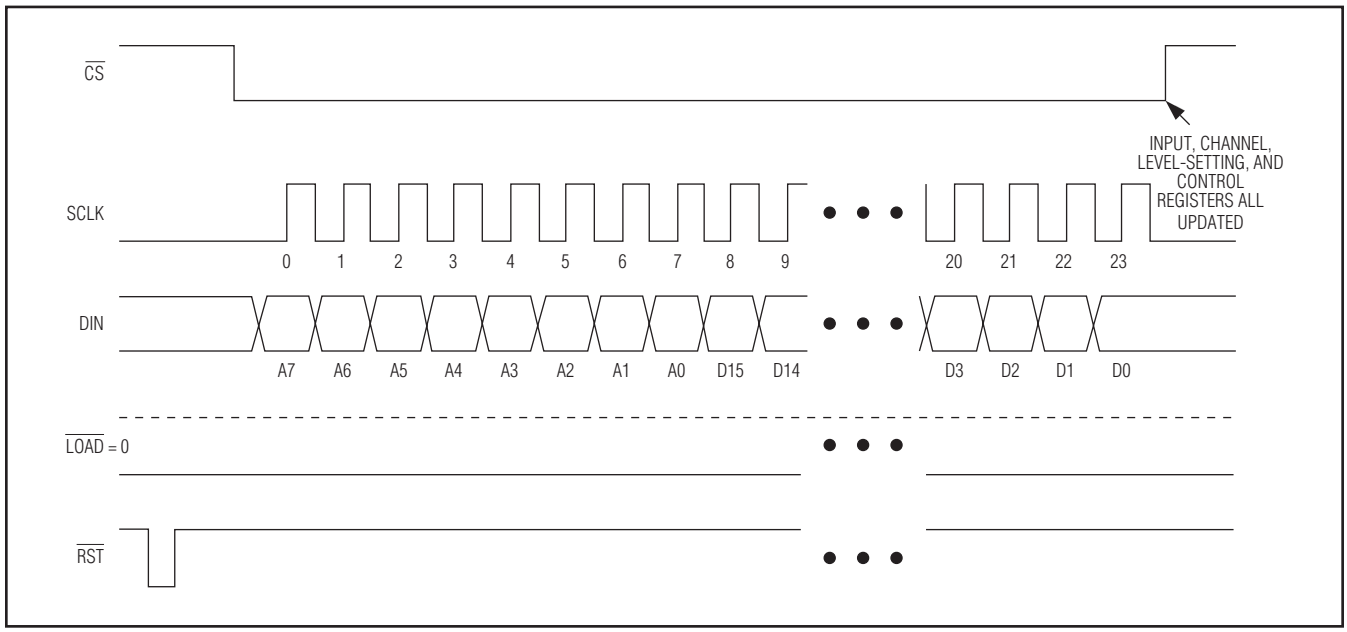

Figure 7. Serial-Port Timing with Synchronous Load ($\overline{LOAD}$ Held Low)

Dual DCL with Integrated Level Setters

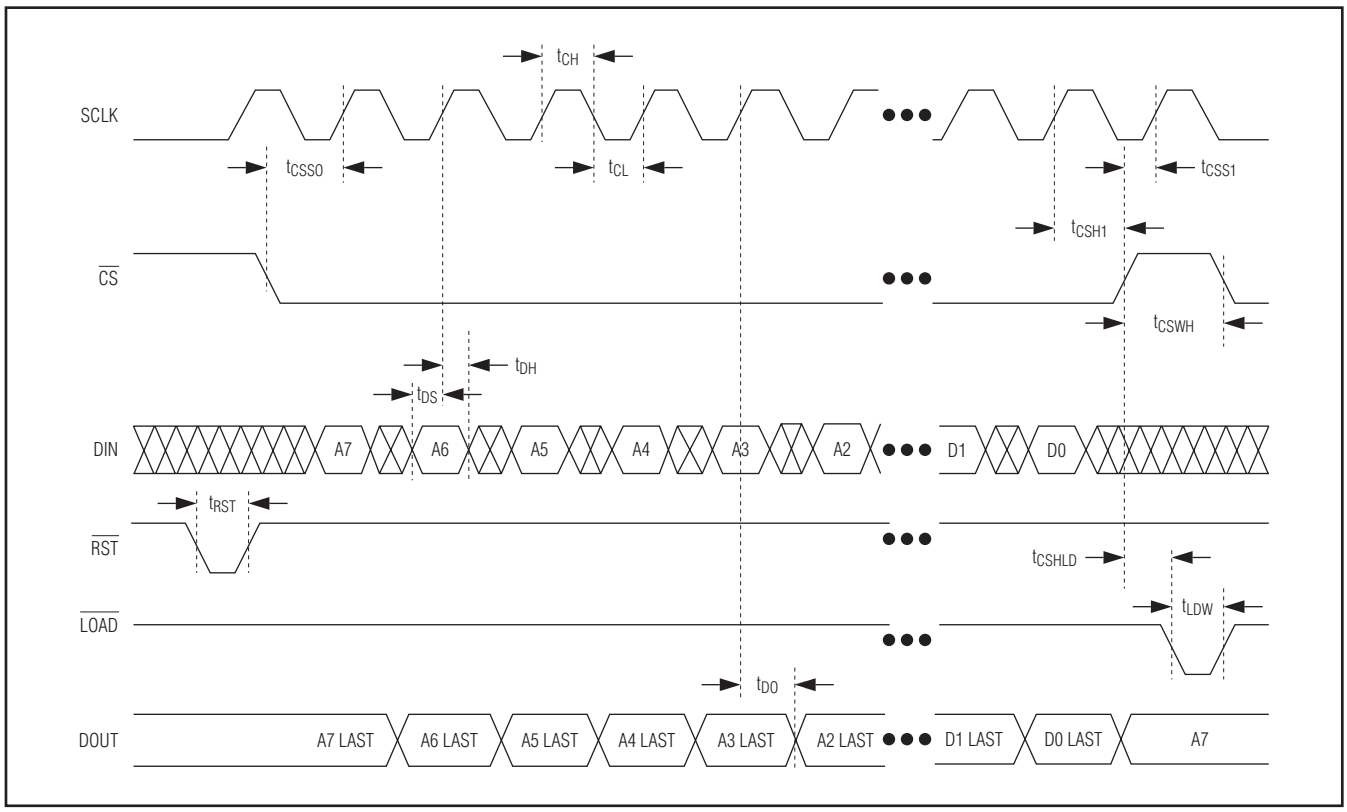

Figure 8. Detailed Serial-Port Timing Diagram

Level-Setter DAC and Calibration Addresses

The MAX19000 contains a total of 20 DACs to generate the DC voltage levels for the various control and monitor circuits of the 2-channel MAX19000, a total of 10 levels per channel. All DAC levels are set by a 14-bit code value that varies between a hex value of 0x0000 and 0x3FFF.

Table 12 identifies the serial-interface address of each DAC and the address of the associated calibration register. Registers can be addressed by individual channel or by utilizing a "broadcast address" that accesses both channels simultaneously. The level-setter output block diagram is shown in Figure 9.

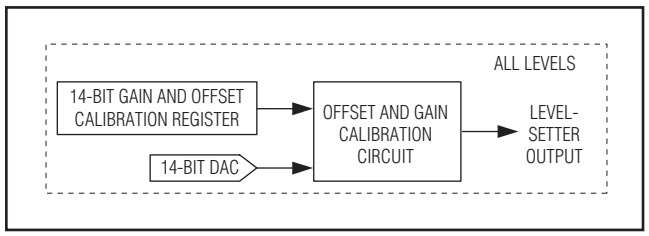

Figure 9. Level-Setter Block Diagram

Level-Setter Calibration Registers (Gain and Offset Codes)

DAC calibration registers adjust the gain and offset of each DAC. Each DAC includes one calibration register. All DAC calibration registers are programmed with a 14-bit code (Table 10). The codes are divided into two fields, one field each for gain (GCAL_) and offset (OCAL_). All DACs provide a 6-bit field for gain and an 8-bit field for offset.

Calibration registers are reset to default values only during a POR. Asserting the $\overline{RST}$ does not force the calibration registers to default values.

Table 10. Register Map

REGISTER NAME	ADDRESS (A[7:0])			MSB		DATA (BIT)											LSB	RESET ORDER	
	CH0, A6 = 0	CH1, A6 = 0	BOTH, A6 = 1	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	RESET CODE	RESET SIGNAL (Note 1)
	A5 = 0, A4 = 0	A5 = 0, A4 = 1	A5 = 0, A4 = 0																		
DCL (Notes 2, 3)	0x00	0x10	0x40	—	—	—	—	—	EN_TEMP_ALARM	EN_OV_ALARM	HYST2	HYST1	HYST0	LDCAL	LDDIS	TMSEL	LLEAKS	SC1	SC0	0x0004	ROR/ RST
DHV: Driver High (Note 2)	0x01	0x11	0x41	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0V)	ROR/ RST
DLV: Driver Low (Note 2)	0x02	0x12	0x42	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0V)	ROR/ RST
DTV: Driver Term (Note 2)	0x03	0x13	0x43	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0V)	ROR/ RST
CHV: High Comparator (Note 2)	0x04	0x14	0x44	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0V)	ROR/ RST
CLV: Low Comparator (Note 2)	0x05	0x15	0x45	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0V)	ROR/ RST
CPHV: High High-Z Clamp, High Overvoltage Detect (Note 2)	0x06	0x16	0x46	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0V)	ROR/ RST
CPLV: Low High-Z Clamp, Low Overvoltage Detect (Note 2)	0x07	0x17	0x47	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0V)	ROR/ RST

Table 10. Register Map (continued)

REGISTER NAME	ADDRESS (A[7:0])			MSB		DATA (BIT)												LSB	RESET ORDER	
	CH0, A6 = 0 A5 = 0, A4 = 0	CH1, A6 = 0 A5 = 0, A4 = 1	BOTH, A6 = 1 A5 = 0, A4 = 0	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	RESET CODE	RESET SIGNAL (Note 1)
COMV: Load Commutation Voltage (Note 2)	0x08	0x18	0x48	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0V)	ROR/RST
LDHV: Load Source Current (Note 2)	0x09	0x19	0x49	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0mA)	ROR/RST
LDLV: Load Sink Current (Note 2)	0x0A	0x1A	0x4A	—	—	DLVL13	DLVL12	DLVL11	DLVL10	DLVL9	DLVL8	DLVL7	DLVL6	DLVL5	DLVL4	DLVL3	DLVL2	DLVL1	DLVL0	0x1333 (0.0mA)	ROR/RST
TS (Notes 2, 4)	0x0F	0x1F	0x4F	—	—	—	—	—	—	—	—	—	TSMUX0	—	—	—	—	—	—	0x0000	ROR/RST
DCL Calibration (Notes 2, 5, 6)	0x80	0x90	0xC0	CDRP_CMP_L2	CDRP_CMP_L1	CDRP_CMP_L0	CDRP_CMP_S2	CDRP_CMP_S1	CDRP_CMP_S0	CDRP_DRV_L2	CDRP_DRV_L1	CDRP_DRV_L0	CDRP_DRV_S2	CDRP_DRV_S1	CDRP_DRV_S0	RO3	RO2	RO1	RO0	0x0008	POR
DHVC: Driver High Calibration (Notes 2, 5, 6)	0x81	0x91	0xC1	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR
DLVC: Driver Low Calibration (Notes 2, 5, 6)	0x82	0x92	0xC2	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR
DTVC: Driver Term Calibration (Notes 2, 5, 6)	0x83	0x93	0xC3	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR

Table 10. Register Map (continued)

REGISTER NAME	ADDRESS (A[7:0])			MSB	DATA (BIT)												LSB	RESET ORDER	
	CH0, A6 = 0	CH1, A6 = 0	BOTH, A6 = 1															RESET CODE	RESET SIGNAL (Note 1)
	A5 = 0, A4 = 0	A5 = 0, A4 = 1	A5 = 0, A4 = 0	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00		
CHVC: High Comparator Calibration (Notes 2, 5, 6)	0x84	0x94	0xC4	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR
CLVC: Low Comparator Calibration (Notes 2, 5, 6)	0x85	0x95	0xC5	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR
CPHVC: High High-Z Clamp, High Overvoltage Detect Calibration (Notes 2, 5, 6)	0x86	0x96	0xC6	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR
CPLVC: Low High-Z Clamp, Low Overvoltage Detect Calibration (Notes 2, 5, 6)	0x87	0x97	0xC7	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR
COMVC: Load Commutation Voltage Calibration (Notes 2, 5, 6)	0x88	0x98	0xC8	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR

Table 10. Register Map (continued)

REGISTER NAME	ADDRESS (A[7:0])			MSB										DATA (BIT)					LSB	RESET ORDER	
	CH0, A6 = 0	CH1, A6 = 0	BOTH, A6 = 1	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	RESET CODE	RESET SIGNAL (Note 1)
	A5 = 0, A4 = 0	A5 = 0, A4 = 1	A5 = 0, A4 = 0																		
LDHVC: Load Source Current Calibration (Notes 2, 5, 6)	0x89	0x99	0xC9	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR
LDLVC: Load Sink Current Calibration (Notes 2, 5, 6)	0x8A	0x9A	0xCA	—	—	GCAL5	GCAL4	GCAL3	GCAL2	GCAL1	GCAL0	OCAL7	OCAL6	OCAL5	OCAL4	OCAL3	OCAL2	OCAL1	OCAL0	0x2080	POR

Note 1: POR/RST denotes that values are reset during a power-on reset (POR) or with the assertion of the RST pin. POR denotes that values are reset during a POR only; thus, the device can be reset to a known state without requiring the reprogramming of calibration registers.
Note 2: Em dash (—) register bits should be set to 0 during write operations.
Note 3: EN_TEMP_ALARM bits are on the CH0 DCL register only (shaded table cell).
Note 4: TSMUX0 bit is on the CH0 TS register only (shaded table cell).
Note 5: The following A[7:0] addresses are not allowed addresses and are not tested:
0x0B ~ 0x0E
0x1B ~ 0x1E
0x4B ~ 0x4E
0x8B ~ 0x8F
0x9B ~ 0x9F
0xCB ~ 0xCF
Note 6: Set A7 = 1 to access calibration registers.

Table 11. Control and Calibration Register Bits

BITS	FUNCTION
CDRP_	Driver and comparator cable-droop compensation
GCAL_	DAC gain calibration
EN_TEMP_ALARM	Enable temperature alarm
EN_OV_ALARM	Enable overvoltage alarm
HYST_	High-speed comparator hysteresis select
LDCAL	Load calibration enable
LDDIS	Load disable
LLEAKS	DCL low-leakage enable
OCAL_	DAC offset calibration
RO_	Driver output-resistance select
SC_	Driver slew-rate control
TSMUX0	Temperature sensor voltage-output control (see Table 14)
TMSEL	Driver terminate select control

Table 12. DAC Addressing Table

LEVEL NAME	LEVEL DESCRIPTION	DAC REGISTER				CALIBRATION REGISTER			
		ADDRESS			RESET VALUE (Note 1)	ADDRESS			RESET VALUE (Note 2)
		CH0	CH1	BOTH		CH0	CH1	BOTH	
$V_{DHV\_}$	Driver high	0x01	0x11	0x41	0x1333	0x81	0x91	0xC1	0x2080
$V_{DLV\_}$	Driver low	0x02	0x12	0x42	0x1333	0x82	0x92	0xC2	0x2080
$V_{DTV\_}$	Driver term	0x03	0x13	0x43	0x1333	0x83	0x93	0xC3	0x2080
$V_{CHV\_}$	High comparator	0x04	0x14	0x44	0x1333	0x84	0x94	0xC4	0x2080
$V_{CLV\_}$	Low comparator	0x05	0x15	0x45	0x1333	0x85	0x95	0xC5	0x2080
$V_{CPHV\_}$	High high-Z clamp, high overvoltage detect	0x06	0x16	0x46	0x1333	0x86	0x96	0xC6	0x2080
$V_{CPLV\_}$	Low high-Z clamp, Low overvoltage detect	0x07	0x17	0x47	0x1333	0x87	0x97	0xC7	0x2080
$V_{COMV\_}$	Load commutation voltage	0x08	0x18	0x48	0x1333	0x88	0x98	0xC8	0x2080
$V_{LDHV\_}$	Load source current	0x09	0x19	0x49	0x1333	0x89	0x99	0xC9	0x2080
$V_{LDLV\_}$	Load sink current	0x0A	0x1A	0x4A	0x1333	0x8A	0x9A	0xCA	0x2080

Note 1: These values are reset during a POR or with the assertion of the $\overline{RST}$ pin.

Note 2: These values are reset during a POR only; thus, the device can be reset to a known state without requiring the reprogramming of calibration registers.

Dual DCL with Integrated Level Setters

Level Transfer Functions

Each of the MAX19000 analog DAC levels is set with a transfer function that includes the 14-bit DAC code setting, the gain code setting, and the offset code setting. The V_{DAC} expression below presents the basic DAC transfer function. Each DAC provides a voltage-output range of -3V to +7V (typ). All 20 of these DACs are identical and generate a voltage according to the following equation:

All DACs except VCOM_ DAC:

$$V_{DAC} = 4 \times (DAC\_code/16,384) \times V_{REF} \times (1 - V_G/V_{REF}) \times (0.98 + 0.02 \times gain\ code/32) - 3V + (0.1 \times offset\_code/128 - 0.1) + V_{DGS} + 1.2 \times V_G$$

where $V_G = V_{GNDDAC\_} - V_{DGS}$.

VCOM_ DAC:

$$V_{DAC} = 4 \times (DAC\_code/16,384) \times V_{REF} \times (1 - V_G/V_{REF}) \times (0.995 + 0.02 \times gain\ code/32) - 3V + (0.1 \times offset\_code/128 - 0.1) + V_{DGS} + 1.2 \times V_G$$

where $V_G = V_{GNDDAC\_} - V_{DGS}$.

For all DACs, the offset code is an integer value between 0 and 255, and the gain code is an integer value between 0 and 63. Offset and gain codes are based on the calibration register settings (Table 13).

The error of the +2.5V external reference impacts the accuracy of the DAC levels; a 1% error in the +2.5V reference translates to a 1% error in the DAC level gain. A precision voltage reference such as the MAX6225 is recommended. The +2.5V external reference must be generated with respect to GNDDAC_. Care must be taken in making GND connections to the MAX19000 from the GND plane. There is a lot of current in each GND connection to the part; typically GND sources approximately 90mA to the part, and this current demand can have significant AC components. The GNDDAC_ connection to the +2.5V reference and to all MAX19000 chips must also be carefully considered. A star connection should be made between GNDDAC_ and DGS. Voltage differences between GNDDAC_ and DGS should be minimized, as V_G is equal to GNDDAC_ - DGS and is an error source for the DAC levels. See the *Level Transfer Functions* section for more information.

Calibration

After mathematically determining the calibration values, shown in Tables 14 and 15, the calibrated levels need to be checked and potentially adjusted up or down because the DAC gain and offset calibration registers have a nonlinear response that could result in the gain or offset values being off by as much as ±3 LSBs, based on mathematical calculations from endpoint measurements during calibration.

Table 13. Level-Setter Transfer Functions

LEVEL	LEVEL-SETTER TRANSFER FUNCTION
$V_{DHV\_}$	DAC voltage x $V_{DHV\_}$ gain + $V_{DHV\_}$ offset
$V_{DLV\_}$	DAC voltage x $V_{DLV\_}$ gain + $V_{DLV\_}$ offset
$V_{DTV\_}$	DAC voltage x $V_{DTV\_}$ gain + $V_{DTV\_}$ offset
$V_{CHV\_}$	DAC voltage x $V_{CHV\_}$ gain + $V_{CHV\_}$ offset
$V_{CLV\_}$	DAC voltage x $V_{CLV\_}$ gain + $V_{CLV\_}$ offset
$V_{CPHV\_}$	DAC voltage x $V_{CPHV\_}$ gain + $V_{CPHV\_}$ offset
$V_{CPLV\_}$	DAC voltage x $V_{CPLV\_}$ gain + $V_{CPLV\_}$ offset
$V_{COMV\_}$	DAC voltage x $V_{COMV\_}$ gain + $V_{COMV\_}$ offset
$V_{LDHV\_}$*	(DAC voltage - V_{DGS}) x (20mA/6V) x $V_{LDHV\_}$ gain + $V_{LDHV\_}$ offset
$V_{LDLV\_}$*	(DAC voltage - V_{DGS}) x (20mA/6V) x $V_{LDLV\_}$ gain + $V_{LDLV\_}$ offset

**$V_{LDHV\_}$ and $V_{LDLV\_}$ levels below zero are truncated.*

Table 14. Offset Calibration Register

CODE	OFFSET VALUE	NOMINAL OFFSET (mV)
11111111	+FS/2 - 1 LSB	+100
• • •	• • •	• • •
10000001	+1 LSB	—
10000000	0	0
01111111	-1 LSB	—
• • •	• • •	• • •
00000000	-FS/2	-100

Table 15. Gain Calibration Register

CODE	OFFSET VALUE	NOMINAL OFFSET (mV)
11111111	+FS/2 – 1 LSB	1.02
• • •	• • •	• • •
10000001	+1 LSB	—
10000000	0	1
01111111	-1 LSB	—
• • •	• • •	• • •
00000000	-FS/2	0.98

Table 16. Calibration Points

DAC	GAIN POINT 1 (V) (CODE)	GAIN POINT 2 (V) (CODE)	OFFSET POINT (V) (CODE)	CONDITION
DHV_	0.125 (0x1400)	3.875 (0x2C00)	0.125 (0x1400)	$V_{DLV\_}$ = -2V, $V_{DTV\_}$ = -1.5V
DLV_	0.125 (0x1400)	3.875 (0x2C00)	0.125 (0x1400)	$V_{DHV\_}$ = +6V, V_{DTV+} = +1.5V
DTV_	0.125 (0x1400)	3.875 (0x2C00)	0.125 (0x1400)	$V_{DLV\_}$ = -2V, $V_{DHV\_}$ = +6V
CHV_	0.125 (0x1400)	3.875 (0x2C00)	2.0 (0x2000)	—
CLV_	0.125 (0x1400)	3.875 (0x2C00)	2.0 (0x2000)	—
CPHV_	-0.5 (0x1000)	5.75 (0x3800)	2.0 (0x2000)	$V_{CPLV\_}$ = -2V, I_{DUT} = -1mA
CPLV_	-1.75 (0x0800)	4.5 (0x3000)	2.0 (0x2000)	$V_{CPHV\_}$ = +6V, I_{DUT} = +1mA
COMV_	0.125 (0x1400)	3.875 (0x2C00)	2.0 (0x2000)	$V_{LDHV\_}$ = +5.5V, $V_{LDLV\_}$ = +5.5V
LDHV_	1mA (0.3V, 0x151F)	18mA (5.4V, 0x35C3)	1mA (0.3V, 0x151F)	$V_{DUT\_}$ = +5.5V, $V_{COMV\_}$ = -1.5V, $V_{LDLV\_}$ = -0.5V
LDLV_	1mA (0.3V, 0x151F)	18mA (5.4V, 0x35C3)	1mA (0.3V, 0x151F)	$V_{DUT\_}$ = -1.5V, $V_{COMV\_}$ = +5.5V, $V_{LDHV\_}$ = -0.5V

Calibration Algorithm

The user can perform a system calibration by overwriting the default values in the gain and offset registers for any DAC level. The DAC calibration points are shown in Table 16.

The DAC calibration algorithm is as follows:

1) Set the offset DAC to midpoint (1000 0000 = 0V nominal).
2) Set the level DAC to gain point 1 (GP1).
3) Set the gain DAC code to minimum = 00 0000.
4) Measure the output and call it $V_{GAINMINGP1}$.
5) Set the gain DAC code to maximum = 11 1111.
6) Measure the output and call it $V_{GAINMAXGP1}$.
7) Set the level DAC to gain point 2 (GP2).
8) Set the gain DAC code to minimum = 00 0000.
9) Measure the output and call it $V_{GAINMINGP2}$.
10) Set the gain DAC code to maximum = 11 1111.
11) Measure the output and call it $V_{GAINMAXGP2}$.
12) Calculate the gain code.

The DAC is not 0V based, so there are gain differences at 0V and at 3V.

For 63 codes, calculate the average range:

$$GAINMIN = (V_{GAINMINGP2} - V_{GAINMINGP1})/(GP2 - GP1)$$

$$GAINMAX = (V_{GAINMAXGP2} - V_{GAINMAXGP1})/(GP2 - GP1)$$

$$GAINRANGE = GAINMAX - GAINMIN$$

$$LSB = GAINRANGE/63$$

Calculated gain code = (1 - GAINMIN)/LSB. Call it GCALC.

13) For gain DAC codes of GCALC - 2 to GCALC + 2, measure the gain (V_{GP2} - V_{GP1})/(GP2 - GP1) at each code, where $V_{GP\_}$ is the output at level DAC code GP_.
14) From codes GCALC - 2 to GCALC + 2, choose the code that yields a gain closest to 1.0 and program the gain DAC to that code.
15) Set the level DAC to the offset point (OP).
16) Set the offset DAC code to minimum = 0000 0000.
17) Measure the output and call it $V_{OFFSMIN}$.
18) Set the offset DAC code to maximum = 1111 1111.
19) Measure the output and call it $V_{OFFSMAX}$.
20) Calculate the offset code:

$$OFFSRANGE = V_{OFFSMAX} - V_{OFFSMIN}$$

$$LSB = OFFSRANGE/255$$

Calculated offset code = (OP - $V_{OFFSMIN}$)/LSB. Call it OCALC.

21) For offset DAC codes of OCALC - 2 to OCALC + 2, measure the offset (V_{OP} - OP) at each code, where V_{OP} is the output at level DAC code OP.
22) From codes OCALC - 2 to OCALC + 2, choose the code that yields an offset closest to the desired value and program the offset DAC to that code.
23) The DAC should now be calibrated.

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Calibration Example

The following is a calibration example for a DHV_ driver output high level:

1) With DHV_ = +0.125V, $V_{GAINMINGP1}$ = +0.1600V and $V_{GAINMAXGP1}$ = +0.084851V.
2) With DHV_ = +3.875V, $V_{GAINMINGP2}$ = +3.8239V and $V_{GAINMAXGP2}$ = +3.9246V.
3) GAINMIN = (3.8239V - 0.1603V)/(3.875V - 0.125V) = 0.976967.
4) GAINMAX = (3.9246V - 0.084851V)/(3.875V - 0.125V) = 1.023933.
5) GAINRANGE = 1.023933 - 0.976967 = 0.046966.
6) LSB = GAINRANGE/63 = 0.000745.
7) Gain code = (1 - 0.976967)/0.000745 = 31.
8) Remeasured +0.125V output at gain codes 29, 30, 31, 32, and 33 = +0.127601V, +0.127091V, +0.126848V, +0.126473V, and +0.126098V.
9) Remeasured +3.875V output at gain codes 29, 30, 31, 32, and 33 = +3.876120V, +3.876615V, +3.877110V, +3.877605V, and +3.878100V.
10) Gains at codes 29, 30, 31, 32, and 33 are +0.999605, +0.999837, +1.000070, +1.000302, and +1.000534.
11) Adjusted gain code = 31 (the closest to 1.0).
12) Program the gain DAC to code 31.
13) Set $V_{DHV\_}$ = +0.125V, $V_{OFFSMIN}$ = +0.0269V, and $V_{OFFSMAX}$ = +0.2180V.
14) Calculate the offset code:

$$OFFSRANGE = V_{OFFSMAX} - V_{OFFSMIN} = +0.2180V - 0.0269V = +0.1911V.$$

$$LSB = OFFSRANGE/255 = + 0.000749V.$$

$$\text{Calculated offset code} = (0.125V - V_{OFFSMIN})/LSB = 131.$$

15) Offsets at codes 129, 130, 131, 132, and 133 are +0.1222V, +0.1230V, +0.1237V, +0.1245V, and +0.1252V.
16) Adjusted offset code = 133 (the closest to +0.125V).
17) Program adjusted offset code.
18) DHV_ should now be calibrated.

Applications

Device Power-Up State

Upon power-up, the DCL enters low-leakage mode; the DCL and calibration registers default to 0x0004 and 0x2080, respectively. See Table 12 for initial power-up values for the levels. Power supplies can be powered on in any sequence.

Alarms

The MAX19000 features two fault-condition alarms. The first is a temperature sense alarm that activates when the MAX19000 internal temperature exceeds +125°C. The second fault condition activates when the voltage on DUT_ falls outside programmable voltage levels, higher than $V_{CPHV\_}$ or below $V_{CPLV\_}$. The $V_{CPHV\_}$ and $V_{CPLV\_}$ levels are set by internal 14-bit DACs and are shared between the high-impedance clamp circuits and OVALARM. Each alarm has an individual enable in the DCL register (channel 0 only) (see Table 10): EN_TEMP_ALARM and EN_OV_ALARM. A binary "1" must be programmed into these enable bits for the monitor circuits to assert their respective alarm outputs (TALARM and OVALARM). Alarm outputs are active low, open drain, and referenced to DGND. It is anticipated that the user implements the latch function in ASIC/FPGA that monitors the TALARM signal. The MAX19000 OVALARM circuit shares its programmable DAC levels with the driver high-Z clamp circuits. The high-Z clamps can never be disabled. To eliminate their influence on the DUT_ line, one simply programs the high-Z clamp voltages out of the way. The proximity of the driver high-Z clamps to the OVALARM thresholds influences the behavior of the OVALARM operation. The OVALARM circuit positively triggers the OVALARM output when a fault condition due to a V_{OVH}/V_{CPH} threshold crossing can source at least 6mA of current to the clamp circuit. Fault conditions causing less than 6mA may or may not

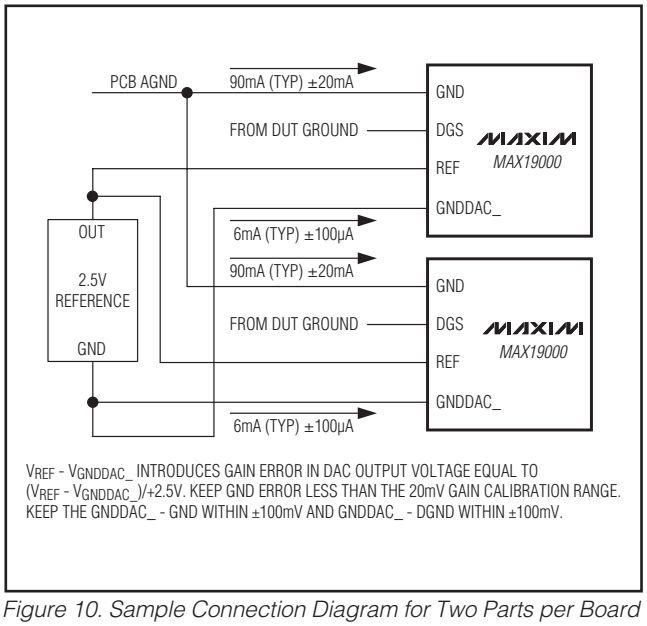

Figure 10. Sample Connection Diagram for Two Parts per Board

trigger an OVALARM output. The same is true near the V_{OVL}/V_{CP} threshold crossing for low voltages (i.e., the fault condition would have to sink at least 6mA of current to the clamp circuit). It should also be noted that when normal high-Z clamp operation is desired because of the lack of source termination at the DUT_, one should disable the OVALARM circuit to eliminate the possibility of nuisance tripping on the OVALARM output due to normal high-Z clamp operation.

Temp Sensor

The temp-sensor function is enabled utilizing the TSMUX0 bit in the TS register. Contents of the TS register can be modified through the serial interface. Table 17 defines the bit code necessary to enable this function. The temp-sensor output is an analog value.

DATA_ and RCV_ Inputs

DATA_ and RCV_ are terminated differentially with internal 100Ω, as shown in Figure 11.

Power-Supply Considerations

Bypass each supply input to GND and REF to DGS with 0.1µF capacitors. Additionally, use bulk bypassing of at least 10µF where the power-supply connections meet the circuit board.

Exposed Pad

The exposed pad (EP) is internally connected to V_{EE}. Connect EP to a large plane or heat sink to maximize thermal performance. EP is not intended as an electrical connection point. Leave EP electrically unconnected, or connect to V_{EE}. Do not connect EP to ground.

Table 17. Temp-Sensor Output Control

TSMUX0 (D6)	TEMP OUTPUT
0	High-Z
1	Temp-sensor voltage

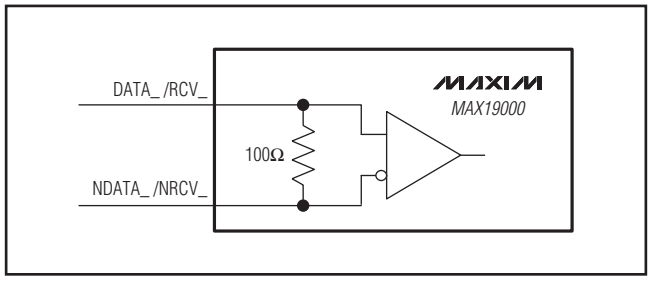

Figure 11. DATA_ and RCV_ Terminations

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 TQFP-EP	C64E+9R	21-0162	90-0164

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	1/10	Updated *General Description*, *Absolute Maximum Ratings*, and *Temp Sensor* sections; *Electrical Characteristics*; and Tables 10, 11, and 14	1, 2, 15, 24, 31, 36–39, 41, 42
2	4/11	Updated *Ordering Information*, *Absolute Maximum Ratings*, *Electrical Characteristics*, *Pin Configuration*, *Pin Description*, and *Driver Cable-Droop Compensation* sections, and Figure 1 and Table 10; added new *Calibration* section	1–26, 28, 36, 40
3	9/11	Corrected typo in V_{DAC} calculation formula	40