Tiny Package, High Performance, Regulated Charge Pump

General Description

The RT9361A/B is a high performance charge pump DC/DC converter that produces a regulated 4.5V and 5V output. No external inductor is required for operation. The operating voltage range is 2.8V to V_{OUT}. Internal soft-start circuitry effectively reduces the in-rush current both while start-up and mode change.

The RT9361A/B features very low quiescent current, over current protection and short circuit protection.

The RT9361A/B is available in WDFN-6L 2x2, SOT-23-6 and TSOT-23-6 package.

Ordering Information

RT9361A/B□ □

- Package Type
  - E : SOT-23-6
  - J6 : TSOT-23-6
  - QW : WDFN-6L 2x2 (W-Type)
- Lead Plating System
  - P : Pb Free
  - G : Green (Halogen Free and Pb Free)
- Output Voltage
  - A : 5V
  - B : 4.5V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

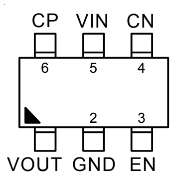
- **Input Voltage Range : 2.8V to V_{OUT}**
- **Internal Soft Start Function**
- **5V/4.5V Fixed Output Voltage**
- **Over Current Protection Function**
- **Short Circuit Protection Function**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

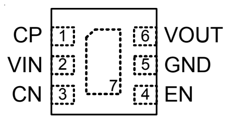
- Mobile phone, Smart Phone LED Backlight
- Camera Flash White LED
- LCD Display Supply

Pin Configurations

(TOP VIEW)



SOT-23-6/TSOT-23-6



WDFN-6L 2x2

Marking Information

RT9361AGJ6

AK=DNN

AK= : Product Code

DNN : Date Code

RT9361APJ6

AK-DNN

AK- : Product Code

DNN : Date Code

RT9361AGE

D3=DNN

D3= : Product Code

DNN : Date Code

RT9361APE

D3-DNN

D3- : Product Code

DNN : Date Code

RT9361AGQW

F8W

F8 : Product Code

W : Date Code

RT9361BPJ6

AL-DNN

AL- : Product Code

DNN : Date Code

RT9361BGE

D4=DNN

D4= : Product Code

DNN : Date Code

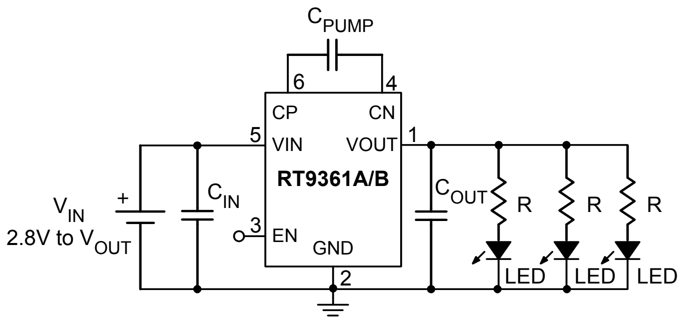
RT9361BPE

D4-DNN

D4- : Product Code

DNN : Date Code

Typical Application Circuit

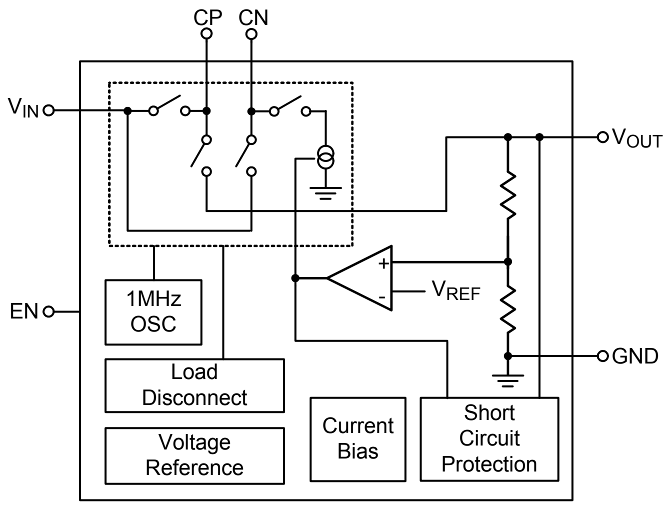


Part No.	Application Configuration	C_{IN} (μF)	C_{PUMP} (μF)	C_{OUT} (μF)
RT9361A	I_{OUT} < 60mA @ V_{IN} > 3.2V,	1 or 2.2	0.22	1 or 2.2
	I_{OUT} < 110mA @ V_{IN} > 3.2V,	10	1	10
RT9361B	I_{OUT} < 80mA @ V_{IN} > 3.2V,	1 or 2.2	0.22	1 or 2.2
	I_{OUT} < 150mA @ V_{IN} > 3.2V,	10	1	10

Functional Pin Description

Pin Number		Pin Name	Pin Function
T/SOT-23-6	WDFN-6L 2x2		
1	6	VOUT	Output Voltage
2	5, Exposed Pad (7)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	4	EN	Chip Enable (Active High)
4	3	CN	Flying Capacitor Negative Terminal
5	2	VIN	Power Input Voltage
6	1	CP	Flying Capacitor Positive Terminal

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 6V
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  T/SOT-23-6 ---------- 0.4W
  WDFN-6L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  T/SOT-23-6, θ_{JA} ---------- 250°C/W
  WDFN-6L 2x2, θ_{JA} ---------- 165°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.7V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage Range	V_{IN}	V_{OUT} = 5V	2.8	--	V_{OUT}	V
Output Voltage	V_{OUT}	RT9361A , V_{IN} = 3.17V to 3.43V, $I_{OUT} \leq$ 55mA	4.83	5	5.2	V
		RT9361A , V_{IN} > 3.2V, I_{OUT} < 110mA	4.8	5	5.2	V
		RT9361B , V_{IN} > 3.2V, I_{OUT} < 150mA	4.32	4.5	4.68	V
Quiescent Current	I_Q	I_{OUT} = 0	--	2	4	mA
Maximum Output Current	I_{OUT}	RT9361A , V_{IN} > 3.2V, C_{PUMP} = 1μF	110	--	--	mA
		RT9361B , V_{IN} > 3.2V, C_{PUMP} = 1μF	150	--	--	
OCP	I_{OCP}		250	350	500	mA
Short Circuit Current			--	60	90	mA
Output Ripple		I_{OUT} = 60mA, C_{OUT} = 2.2μF	--	30	--	mV
Shut Down Current	I_{SHDN}	V_{IN} = 4.5V, V_{EN} < 0.4V	--	0.1	1	μA
Operation Frequency	F_{OSC}		0.8	1	1.3	MHz
Digital Input High Level	V_{IH}		1.5	--	--	V
Digital Input Low Level	V_{IL}		--	--	0.4	V

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at $T_A = 25°C$ on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

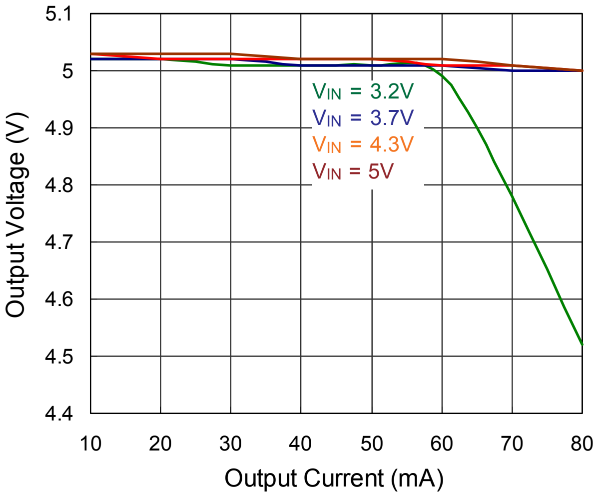
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

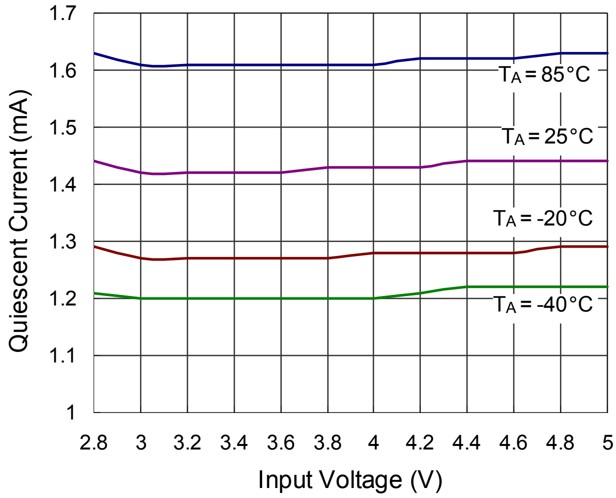
Typical Operating Characteristics

(For RT9361A, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{PUMP} = 0.22\mu F$, $T_A = 25°C$, unless otherwise specified)

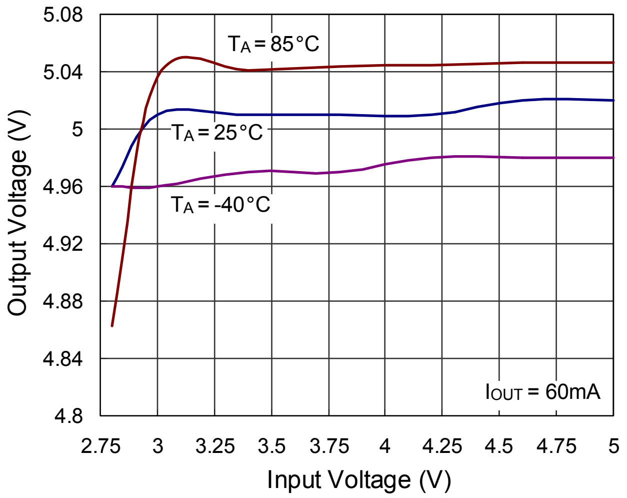
Output Voltage vs. Output Current



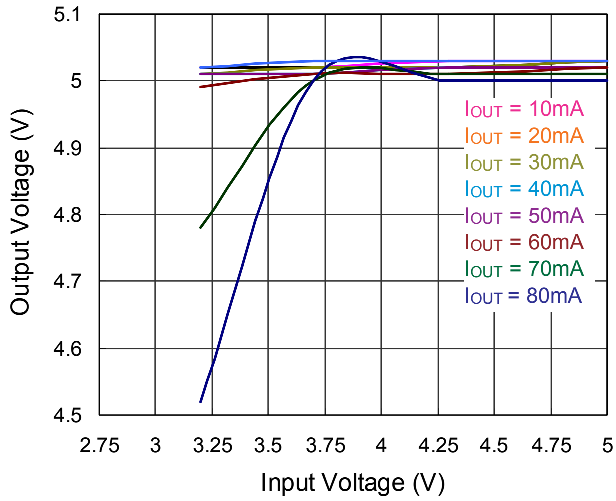
Quiescent Current vs. Input Voltage



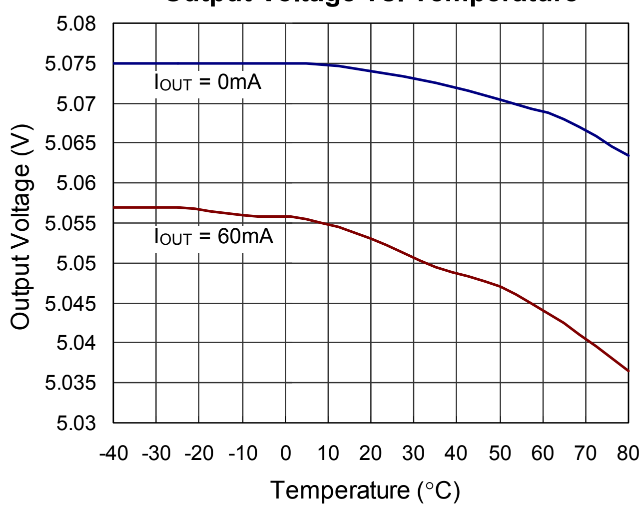
Output Voltage vs. Input Voltage



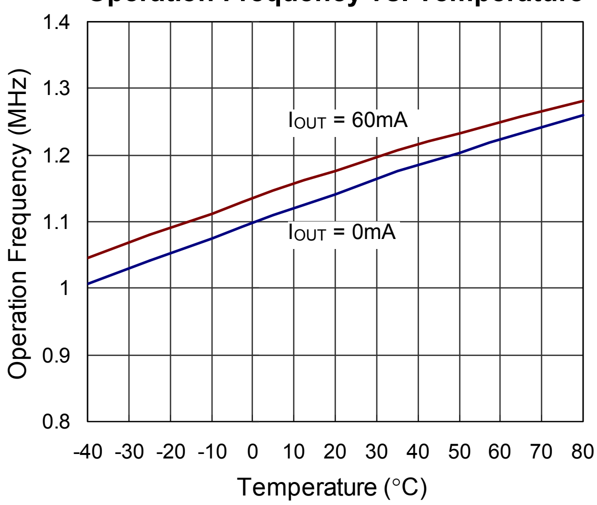
Output Voltage vs. Input Voltage

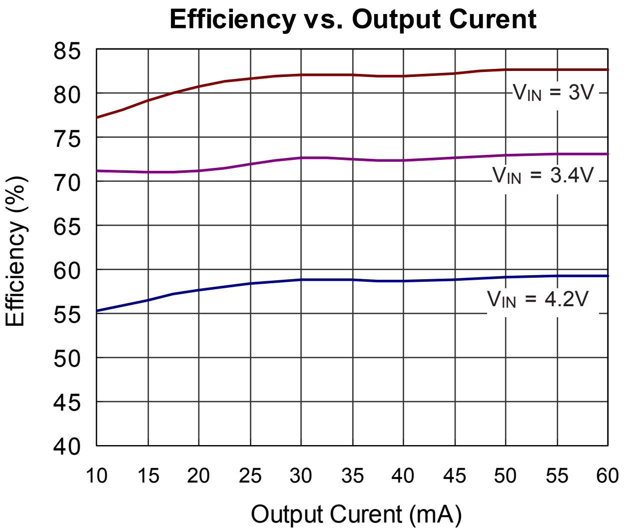


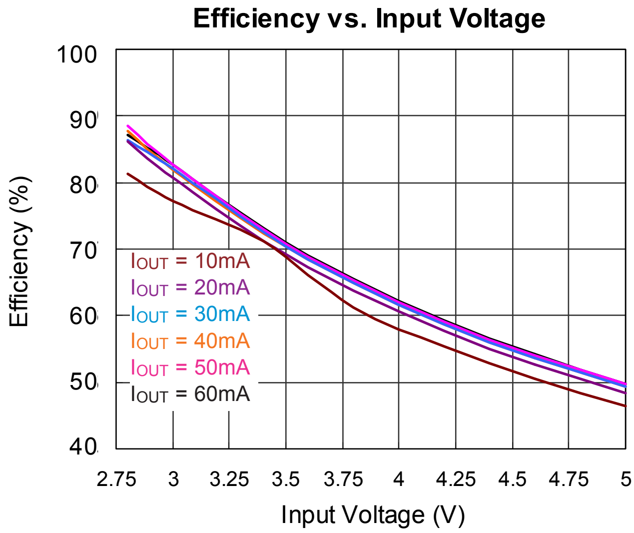
Output Voltage vs. Temperature

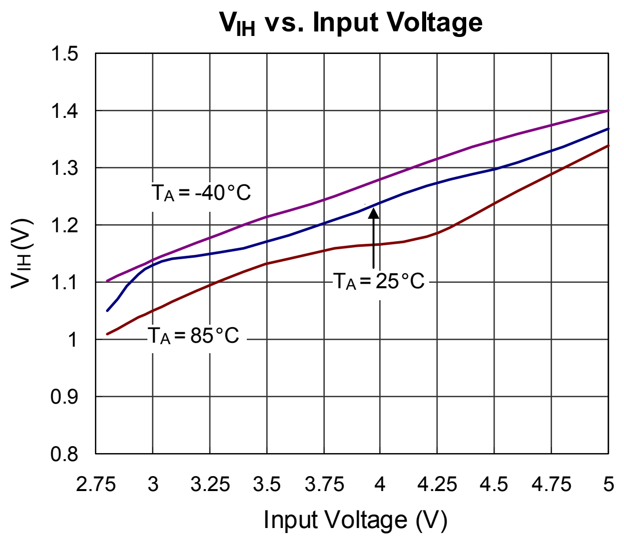


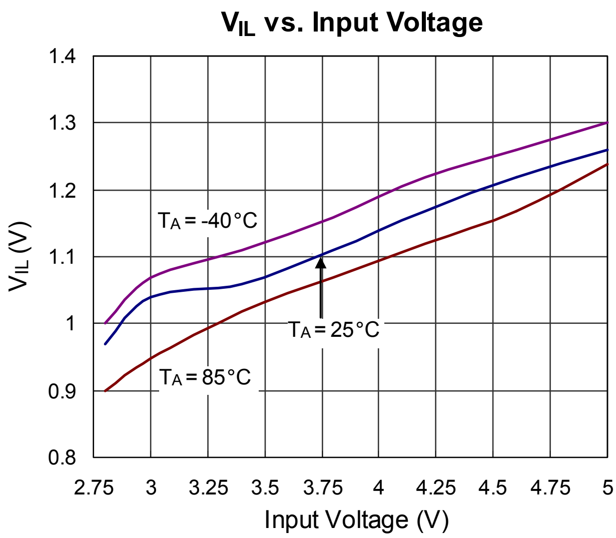
Operation Frequency vs. Temperature

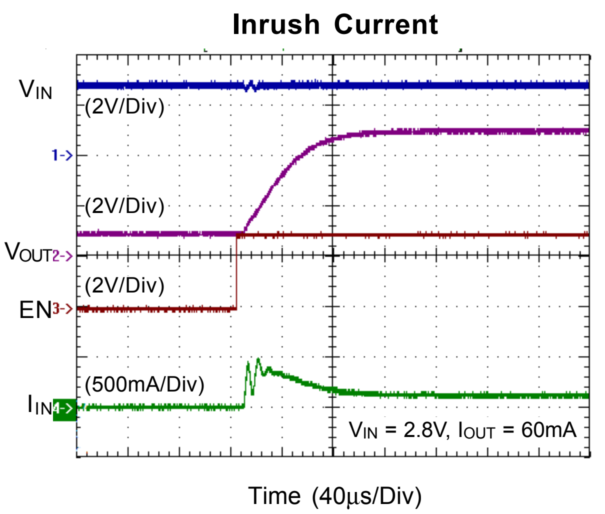


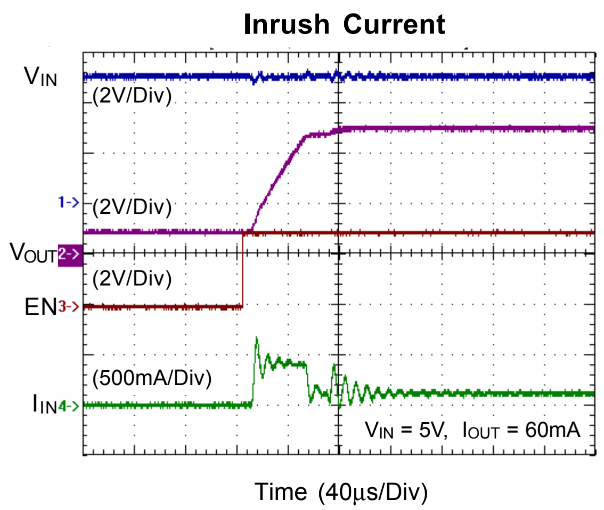

Efficiency vs. Output Curent
Efficiency (%)
Output Curent (mA)
VIN = 3V
VIN = 3.4V
VIN = 4.2V


Efficiency vs. Input Voltage
Efficiency (%)
Input Voltage (V)
IOUT = 10mA
IOUT = 20mA
IOUT = 30mA
IOUT = 40mA
IOUT = 50mA
IOUT = 60mA

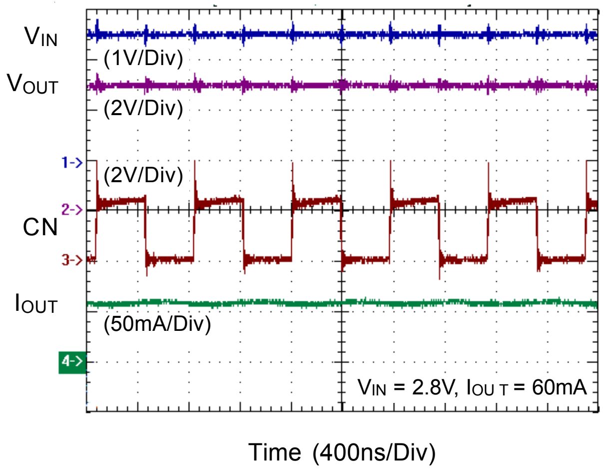

VIH vs. Input Voltage
VIH (V)
Input Voltage (V)
TA = -40°C
TA = 25°C
TA = 85°C


VIL vs. Input Voltage
VIL (V)
Input Voltage (V)
TA = -40°C
TA = 25°C
TA = 85°C

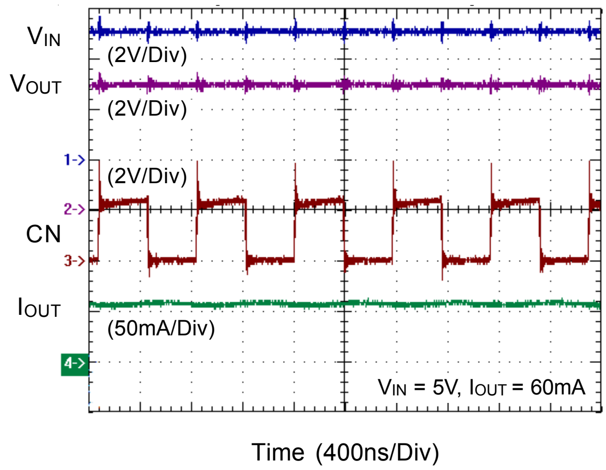

Inrush Current
VIN
(2V/Div)
VOUT
(2V/Div)
EN
(2V/Div)
IIN
(500mA/Div)
VIN = 2.8V, IOUT = 60mA
Time (40μs/Div)


Inrush Current
VIN
(2V/Div)
VOUT
(2V/Div)
EN
(2V/Div)
IIN
(500mA/Div)
VIN = 5V, IOUT = 60mA
Time (40μs/Div)

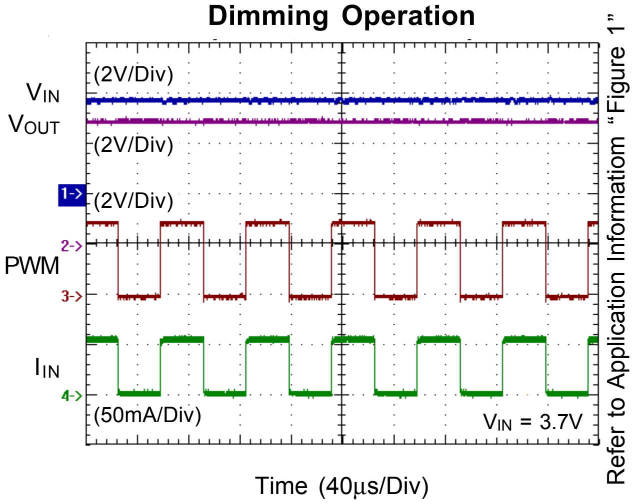
Normal Operation



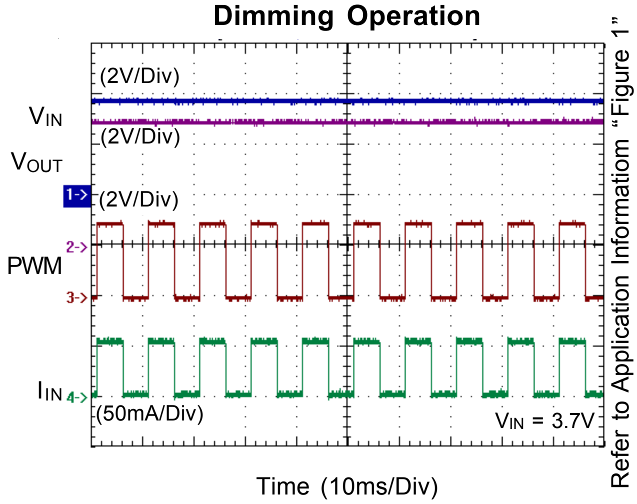
Normal Operation



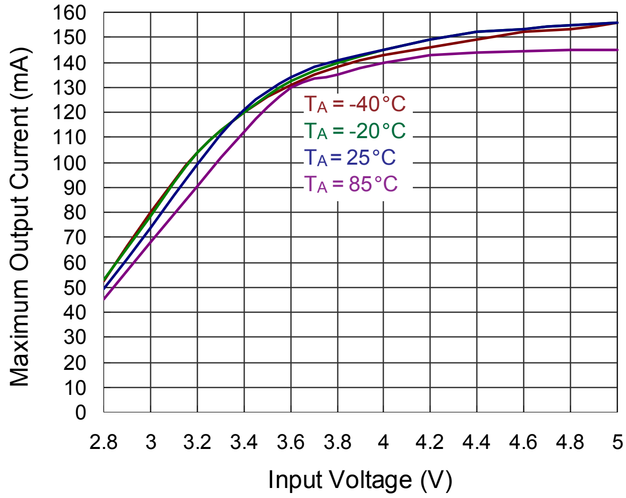
Dimming Operation



Dimming Operation



Maximum Output Current vs. Input Voltage



Application Information

Capacitor Selection

Careful selection of the three external capacitors C_{IN}, C_{OUT} and C_{PUMP} is very important because they will affect ramp-up time, output ripple and transient performance. Optimum performance will be obtained when low ESR (<100mΩ) ceramic capacitors are used for C_{IN} and C_{OUT} and C_{PUMP}. In general, low ESR may be defined as less than 100mΩ. In all cases, X7R or X5R dielectric are recommended. For particular application, low ESR Tantalum capacitors may be substituted; however optimum output ripple performance may not be realized. Aluminum electrolytic capacitors are not recommended for using with the RT9361A/B due the their inherent high ESR characteristic.

In general, lower values for C_{IN}, C_{OUT} and C_{PUMP} may be utilized for light load current applications (<60mA). Drawing a load current of 60mA or less may use a C_{IN} and C_{OUT} capacitor value as low as 2.2µF and a C_{PUMP} value of 0.22µF. C_{IN} and C_{OUT} may range from 1µF for light loads to 10µF for heavy output load conditions (<110mA). C_{PUMP} may range from 0.22µF for light loads to 1µF for heavy output load conditions. If C_{PUMP} is increased, C_{OUT} should also be increased by the same ratio to minimize output ripple. As a basic rule, the ratio between C_{IN}, C_{OUT} and C_{PUMP} should be approximately 10 to 1. Lowering the C_{IN}, C_{OUT} and C_{PUMP} value can decrease the ramp-up time of V_{OUT}, but it will increase the output ripple oppositely.

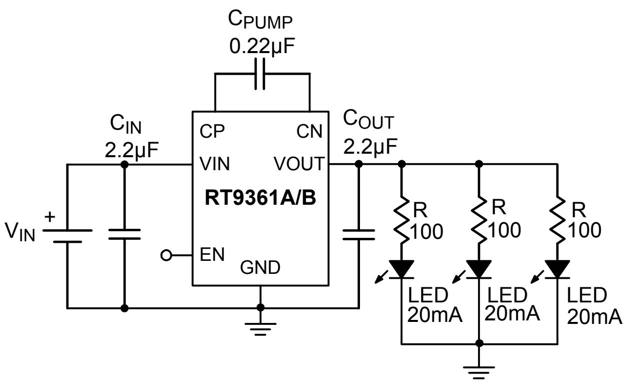


Figure 1. Application Circuits for Backlight Dimming

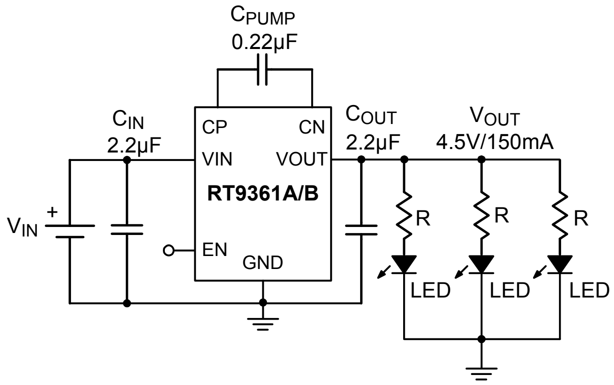


Figure 2. Application Circuits for Flash LEDs

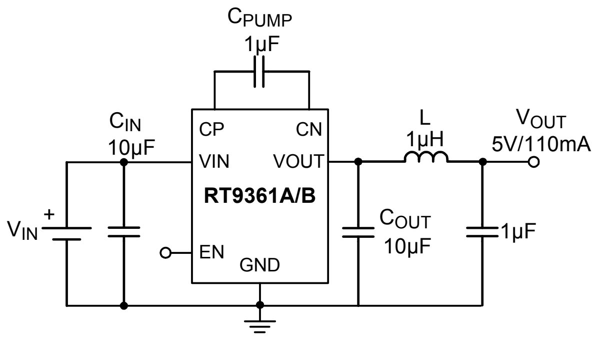


Figure 3. Application Circuits for Constant Load

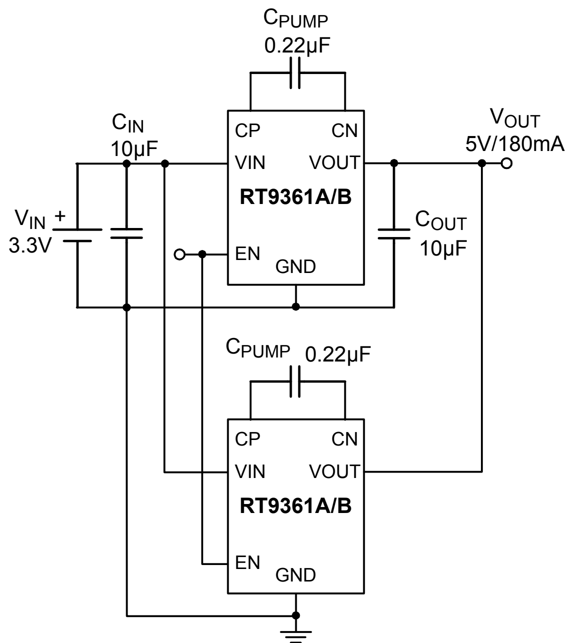


Figure 4. Application Circuits for Doubling the Output Current

Efficiency

The efficiency of the charge pump regulator varies with the output voltage version, the applied input voltage, the load current, and the internal operation mode of the device.

The approximate efficiency is given by :

$$\text{Efficiency (\%)} = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times 2I_{OUT}} \times 100$$

$$= \frac{V_{OUT}}{2V_{IN}} \times 100 --- (\times 2 \text{ Charge Pump Operating Mode})$$

For a charge pump with an output of 5 volts and a nominal input of 3 volts, the theoretical efficiency is 83.33%. Due to internal switching losses and IC quiescent current consumption, the actual efficiency can be measured as 82.72%.

Thermal Considerations

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9361, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the operated ambient temperature. The junction to ambient thermal resistance θ_{JA} for T/SOT-23-6 is 250°C/W and WDFN-6L 2x2 is 165°C/W on the standard JEDEC 51-3 single layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / 250°C/W = 0.4W for T/SOT-23-6 packages

$P_{D(MAX)}$ = (125°C − 25°C) / 165°C/W = 0.606W for WDFN-6L 2x2 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9361 packages, the Figure 5 of de-rating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

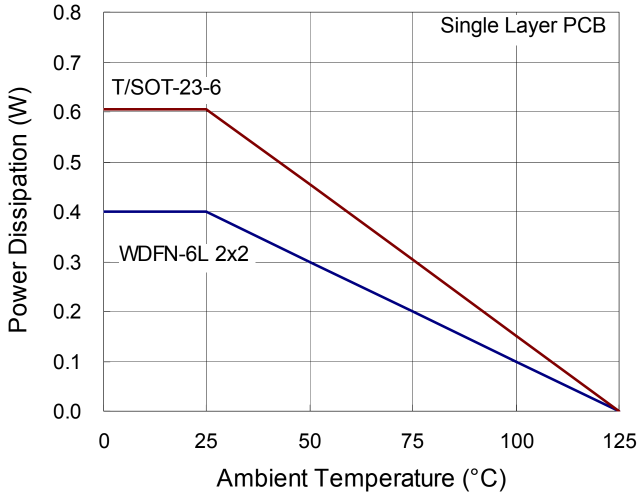


Figure 5. Derating Curves for RT9361 Packages

PCB Board Layout

The RT9361A/B is a high-frequency switched-capacitor converter, and therefore large transient currents will flow in V_{IN} and V_{OUT}. For best performance and to minimize ripple, place all of the components as close to IC as possible. Besides a solid ground plane is recommended on the bottom layer of the PCB. The ground of C_{IN} and C_{OUT} should be connected together and as close to the IC as possible. Figure 6 and Figure 7 shows the typical PCB layout of RT9361A/B EVB board.

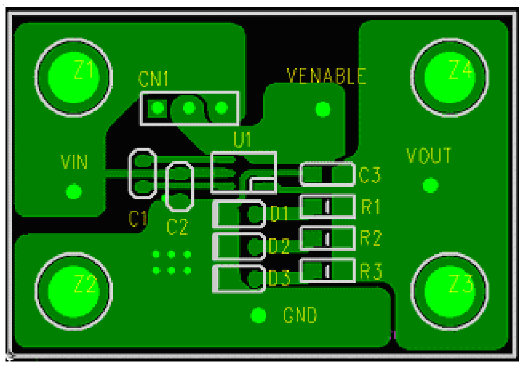


Figure 6

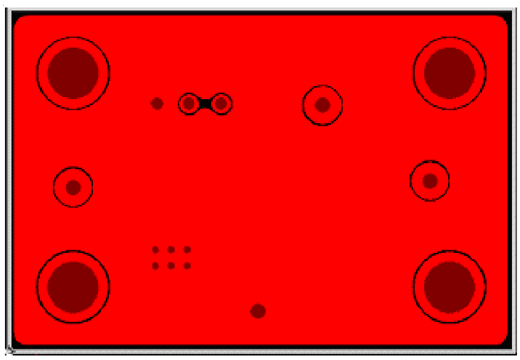
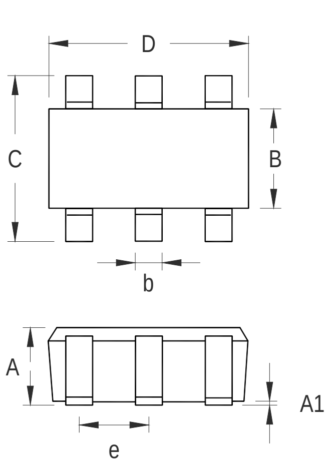


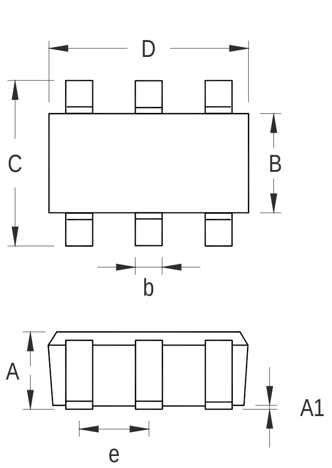
Figure 7

Outline Dimension



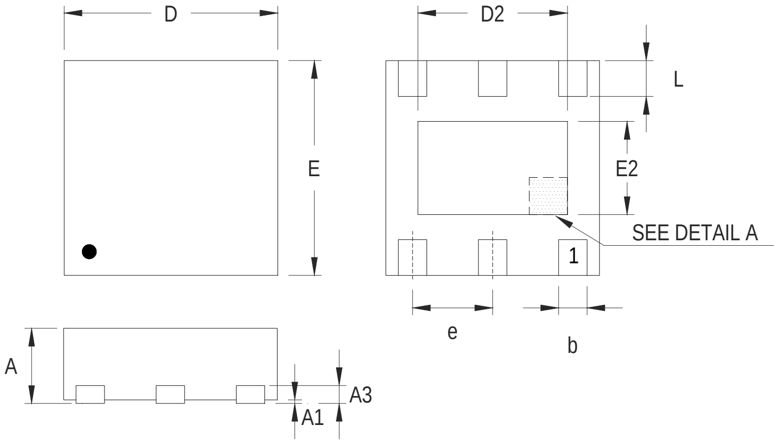
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

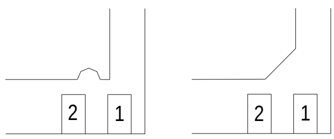
SOT-23-6 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-6 Surface Mount Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

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