DA7210 ULTRA LOW POWER STEREO AUDIO CODEC WITH TRUE-GND HEADPHONE DRIVER

DESCRIPTION

The DA7210 is a high fidelity audio codec with integrated true-ground capless headphone driver suitable for a variety of low power, digital portable audio products.

Featuring a high efficiency headphone amplifier and supporting economic single supply voltages down to 1.8V, the ultra-low 2.5mW power consumption extends music playback time for battery operated equipment.

Eight analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimize dynamic range prior to digitisation. This allows a diverse variety of analogue audio sources such as mobile TV, WiFi and FM radio to be managed. Input and output mixers with stereo to mono conversion directly support mono headsets. The acoustic components for baseband voice are routed via an independent differential up- and downlink. A dedicated voice mode for the TX and RX path combined with a digital sidetone engine provides the complete audio feature set required for mobile phones and telephony applications.

DA7210 provides simultaneous connection to stereo headphone, stereo line outputs, and a mono differential output. Stereo line outputs can be differential or singe-ended. Both stereo outputs have volume control from -54dB to +15dB.

Filtering and gain control is performed digitally including 5-band EQ and a digital input AGC with programmable attack and decay parameters. A configurable signal processing engine allows various enhancements and effects on the digital audio signal like acoustic filtering, wind noise suppression and 3D sound.

The multislot I2S/PCM interface supports all common sample rates between 8-96kHz in master and slave modes. The integrated PLL supports a large range of input and output frequencies. Sample Rate Measurement (SRM) allows a seamless connection with non clock synchronized audio streams. This is in addition to standard mobile phone/USB system clock frequencies - enabling audio data synchronization even in applications with dynamic master clocks.

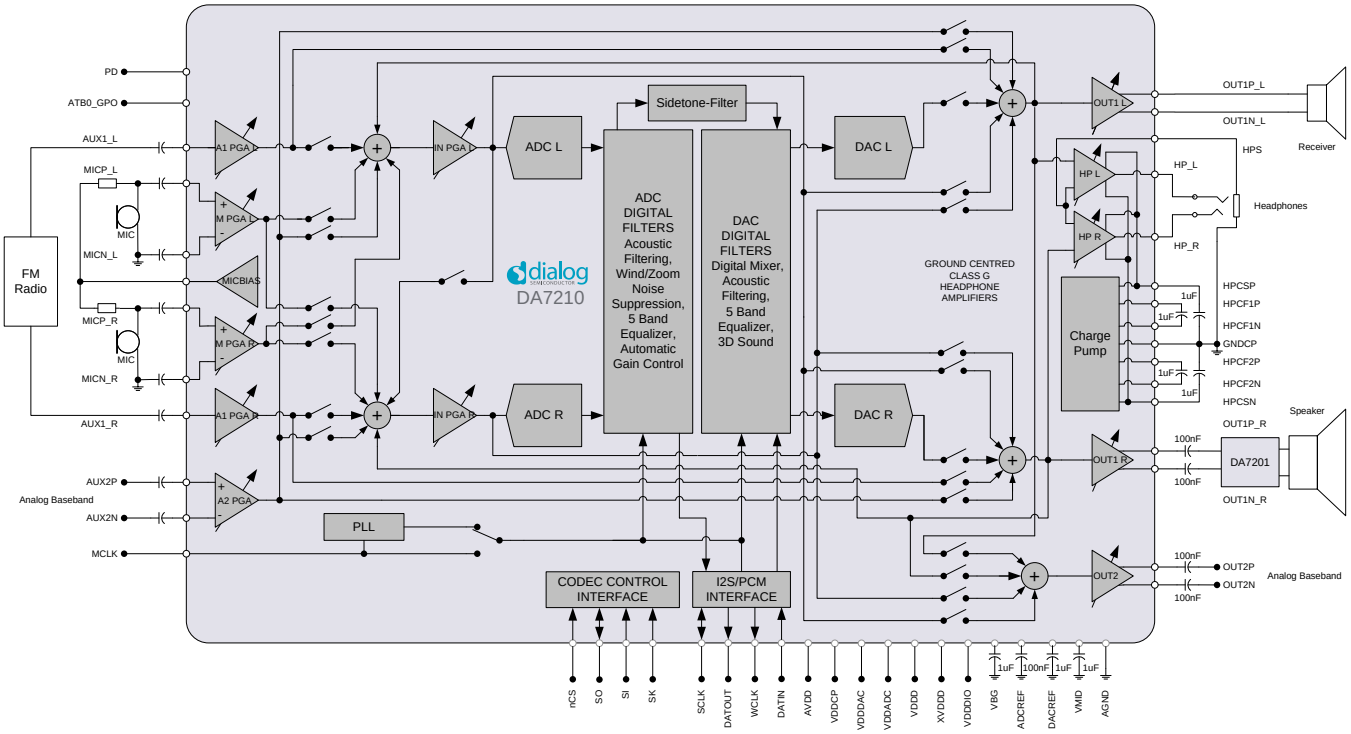
KEY FEATURES

- Stereo Multi-bit Delta Sigma DAC with SNR 100dB ('A' weighted @ 48kHz)
- Stereo Multi-bit Delta Sigma ADC with SNR 96dB ('A' weighted @ 48kHz)
- Ultra low power Stereo Headphone Driver with
  - Stereo DAC to HP playback power: 2.5mW
  - 2x58mW Output Power (16Ω)
  - 'Capless' output via GND centred signals
  - Four level charge pump with continuous tracking of audio signal (Class G)
  - Short circuit protection
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 and 96 kHz sample rates
- On-chip PLL with Signal Shaper and Audio Sample Rate Measurement
- Wide range of external clocks including industry standard 256xFs, system clock 12, 13, 24, 26 or 27MHz and low power 32kHz mode
- Audio Serial Data Bus supports I2S, left/right-justified, DSP and TDM modes
- Stereo or Mono Differential Microphone Interface
- Programmable Ultra-low-noise Bias Supply for electret microphones
- Volume controlled Stereo Auxiliary Inputs and Outputs supporting FM-Radio and fixed gain Speaker Amplifiers
- Fully differential Voice Link for analogue baseband connections
- Multi-mode Audio Routing and Mixers
- Pop & Click suppression circuitry
- ASSP DSP filter engine for digital audio enhancements (acoustic filtering, wind noise suppression, 5-band-equalizer, 3D sound, automatic gain control)
- Supports supply from single voltage (1.8/2.5V) with embedded VDDD voltage regulator
- Extensive modular power control
- Package: **49 bump WLCSP - 0.4mm pitch**

APPLICATIONS

- Smart phones, PNDs and PDAs
- Portable multimedia player and camcorder

SYSTEM OVERVIEW



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General

DA7210 is an ultra low power audio CODEC with a true ground headphone, mixing capability and a programmable ASSP filter engine. It offers HiFi audio quality with class leading power consumption for portable media applications.

Featuring a high efficiency headphone amplifier and minimum supply voltage of 1.8V, the ultra-low 2.5mW power consumption extends music playback time for battery operated equipment. The integrated PLL uses a FRACT-N PLL architecture that supports a large range of input and output frequencies. This is in addition to standard mobile phone/USB system clock frequencies - enabling audio data synchronization when no master clock is readily available.

Eight analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimize dynamic range prior to digitisation. This allows a diverse variety of analogue audio sources such as baseband voice, mobile TV, WiFi and FM radio to be managed.

Input and output mixers with stereo-to- mono conversion also support mono configurations such headset/baseband line outputs.

3 output drivers are designed in the output stage of the DA7210. One output driver will directly drive standard 3-wire 16ohm headphones whilst the other two provide two adjustable fully differential stereo lineout channels.

POWER SUPPLY BLOCKS

Audio Parametrics

Test conditions: VDDD=2.5V, Ta=25oC, fs=48kHz, 24 bit audio data unless specified otherwise

Microphone Bias

PARAMETER	SYMBOL	TEST CONDITIONS	Min	Typ	Max	UNIT
Bias Voltage	V_{BIAS}	No load, AVDD = 2.5V No load, AVDD = 1.8V	2.2 1.5	pro-grammable	2.3 1.6	V
Maximum Current	I_{BIAS}	Voltage drop < 50mV		2		mA
Power Supply Rejection Ratio	PSRR[4] with respect to AVDD	20Hz -200Hz >2kHz	70 50			dB
Output Noise Voltage	V_N			5		μV_{RMS}
Capacitive Load		I_{BIAS} < 100uA, 100uA < I_{BIAS} < 2mA		100 200		pF

[4] PSRR is the level difference of output signal against the voltage of a sine wave ripple voltage on VDD

Input Mixing Units						
(MICP_L, MICN_L, AUX_L, AUX2 to DC L, MICP_R, MICN_R, AUX2 to ADR R)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale Input Signal	V_{MAX}	single ended differential M/Ax-PGA=0dB, IN-PGA=0dB		0.8*AVDD 1.6*AVDD		V_{PP}
Input resistance	R_{IN}	Mic, meas. single ended A1 A2	12 6 24	15 variable 30	18 40 36	kΩ
Frequency Response		+/- 0.5dB	20		20k	Hz
Amplitude Ripple		20Hz – 20kHz	-0.5		0.5	dB
Programmable Gain[5]		M-PGA A1-PGA A2-PGA IN-PGA	-6 -48 -6 -4.5		24 21 12 18	dB
Programmable Gain Step Size		M-PGA, A2-PGA A1-PGA, IN-PGA		6 1.5		dB
Absolute Gain Accuracy		$0dB_{m0}$ @ 1kHz	-1.0		1.0	dB
Input Gain L/R-Mismatch		20Hz – 20kHz	-0.1		0.1	dB
Input Gain Step Error		20Hz – 20kHz	-0.1		0.1	dB
Input Noise Level	V_{NOISE}	Inputs connected to GND A-weighting input referred, measured @ ADC output Mic (Gain = 42dB) A1 (Gain = 21dB) A2 (Gain = 18dB)		5 6.5 8.8		μV_{RMS}
Power Supply Rejection Ratio	PSRR[4] with respect to AVDD	20Hz -2kHz 20kHz, single ended input	80 70			dB
		20Hz -2kHz 20kHz, differential input	90 70			dB

[5] The gain describes the ratio of in- and output signal level at the related amplifier stage (independent whether the connection is single ended or differential)

Analogue to Digital Converter (ADC)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale Input Signal	V_{MAX}	Corresponding digital level 0 dBFS		1.6*VDDADC		V_{PP}
Signal to Noise Ratio	SNR[6]	A-weighting, no input selected		96		dB
Total Harmonic Distortion Plus Noise	THD+N[7]	-1dBFS		-89		dB
Channel separation				90		dB
Pass band	B_{PASS}				0.45*fs	kHz
Stop band	B_{STOP}	fs ≤ 48kHz fs = 88.2/96kHz	0.56*fs		7*fs 3.5*fs	kHz
Pass band Ripple		Voice mode Music Mode			+/-0.3 +/-0.1	dB
Stop band Attenuation		Voice mode Music Mode	70 55			dB
Group delay		Voice mode Music Mode[8] Fs=fs = 88.2/96kHz		4.3/fs 18/fs 9/fs	600	µs
Group delay mismatch		Between left and right channel			2	µs
Power Supply Rejection Ratio	PSRR[4] with respect to VDDADC	20Hz -2kHz 20kHz	80 70			dB

[6] SNR is a measure of the level difference between full scale output and the output with no signal applied
[7] THD+N is a ratio of noise+distortion against signal
[8] with 5-band-equalizer disabled

Digital to Analogue Converter (DAC)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale Output Signal	V_{MAX}	Corresponding digital level 0 dBFS		1.6*VDDDAC		V_{PP}
Signal to Noise Ratio	SNR[6]	A-weighting		102		dB
Total Harmonic Distortion Plus Noise	THD+N[7]	-1dBFS		-90		dB
Total Harmonic Distortion Plus Noise	THD+N[7]	-1dBFS, 32kHz PLL mode		-80		dB
Channel separation				90		dB
Pass band	B_{PASS}				0.45*fs	kHz
Stop band	B_{STOP}	fs ≤ 48kHz fs = 88.2/96kHz	0.5556*fs		7.5*fs 3.5*fs	kHz
Pass band Ripple		Voice mode Music ModeAudio Mode			+/-±0.153 +/-±0.105	dB
Stop band Attenuation		Voice mode Music ModeAudio Mode	705 55			dB
Group delay		Voice mode Music Mode[8]Audio Mode[9] Fs=fs = 88.2/96kHz		4.8/fs 18.5/fs 9/fs	650	µus
Group delay variation		20Hz to 20kHz[7]			1	µus
Group delay mismatch		Between left and right channel			2	µus
Power Supply Rejection Ratio	PSRR[4] with respect to VDDDAC	20Hz -2kHz 20kHz	70 60			dB

[9] MCLK signal can be applied as a CMOS input relative to VDDDIO or as an AC signal directly (excluding 32kHz mode) from an oscillator output (~300mV) triangle, sine or square wave.

Line Out and Receiver Amplifier (OUT1P_L, OUT1N_L, OUT1P_R, OUT1N_R)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale Output Signal	V_{MAX}	No load, single ended No load, differential		0.8*AVDD 1.6 *AVDD		V_{PP}
Load Impedance		single ended output mode	500	2k	 1 200	Ω µH pF
		differential output mode	25	32	 1 200	Ω µH pF
Frequency Response		+/- 0.5dB	20		20k	Hz
Amplitude Ripple		20Hz – 20kHz	-0.5		0.5	dB
Programmable Gain			-54		15	dB
Mute Attenuation				100		dB
Programmable Gain Step Size				1.5		dB
Absolute Gain Accuracy		$0dB_{m0}$ @ 1kHz	-0.8		0.8	dB
Input Gain L/R-Mismatch		20Hz – 20kHz	-0.1		0.1	dB
Input Gain Step Error		20Hz – 20kHz	-0.1		0.1	dB
Signal to Noise Ratio	SNR[6]	A-weighting		102		dB
Output Noise Level	V_{NOISE}	20 -20kHz, unweighed Gain gain < -15dB Singlesingle ended Differential		 <5.5 <4.5		µV
Total Harmonic Distortion Plus Noise	THD+N[7]	-1dBFS, 44.1kHz slave mode non A-weighting		-90		dB
Power Supply Rejection Ratio	PSRR[4] with respect to AVDD	20Hz -2kHz 20kHz single ended ouput	70 47			dB
Power Supply Rejection Ratio	PSRR[4] with respect to AVDD	20Hz -2kHz 20kHz, differential ouput	90 70			dB

Line Out Amplifier (OUT2P, OUT2N)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale Output Signal	V_{MAX}	No load		1.6*AVDD		V_{PP}
Load Impedance			25	32	 1 200	Ω µH pF
Frequency Response		+/- 0.5dB	20		20k	Hz
Amplitude Ripple		20Hz – 20kHz	-0.5		0.5	dB
Programmable Gain			-18		6	dB
Programmable Gain Step Size				6		dB
Input Gain L/R-Mismatch		20Hz – 20kHz	-0.1		0.1	dB
Input Gain Step Error		20Hz – 20kHz	-0.2		0.2	dB
Signal to Noise Ratio	SNR[6]	A-weighting, gain = 0dB		102		dB
Output Noise Level	V_{NOISE}	20 -20kHz, unweighed Gain < -15dB, gain ≤ -12dB		<5		µV
Total Harmonic Distortion Plus Noise	THD+N[7]	-1dBFS , A-weighting		-90		dB
Power Supply Rejection Ratio	PSRR[4] with respect to AVDD	20Hz -2kHz 20kHz	90 70			dB

Dynamic charge pump (HPCSP, HPCSN)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Positive dynamic supply voltage	VDDCSP	VDDCP/3/4 can optionally be enabled if two flying caps are available		VDDCP VDDCP/2 (VDDCP/3, VDDCP/4)		
Negative dynamic supply voltage	VDDCSN	-VDDCP/3/4 can optionally be enabled if two flying caps are available		-VDDCP -VDDCP/2 (-VDDCP/3, -VDDCP/4)		
Floating capacitors		one (two)		1.0		µF
Storage capacitors		two		1.0		µF

Headphone Amplifier (HPL, HPR)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale Output Signal	V_{MAX}	No load		1.6*VDDCP		V_{PP}
DC output offset				100		µV
Output Power per channel	P_{MAX}	VDDCP = 1.8V, THD < 0.1%, R_L=16Ω, 1kHz		28		mW_{RMS}
		VDDCP = 2.5V, THD < 0.1%, R_L=16Ω, 1kHz		58		mW_{RMS}
Dynamic internal supply voltages		VDD/3 or VDD/4 can optionally be selected if two flying caps are available		±VDD ±VDD/2 (±VDD/3 (±VDD/4)		
Quiescent current per channel	IQ	from VDDCP		100		uA
Load Impedance		13 < R_L < ∞	13	16	400 500	Ω µH pF
Frequency Response		+/- 0.5dB	20		20k	Hz
Amplitude Ripple		20Hz – 20kHz	-0.5		0.5	dB
Programmable Gain			-54		15	dB
Mute Attenuation				100		dB
Programmable Gain Step Size				1.5		dB
Absolute Gain Accuracy		$0dB_{m0}$ @ 1kHz	-0.8		0.8	dB
Input Gain L/R-Mismatch		20Hz – 20kHz	-0.1		0.1	dB
Input Gain Step Error		20Hz – 20kHz	-0.1		0.1	dB
Signal to Noise Ratio	SNR[6]	A-weighting, gain = 0dB		100		dB
Output Noise Level	V_{NOISE}	20 -20kHz, unweighed Gain, gain < -15dB		<4.5		µVrms
Total Harmonic Distortion Plus Noise	THD+N[5]	VDDCP = 1.8V, -5dBFS, R_L=16Ω		-80		dB
Power Supply Rejection Ratio	PSRR[4] with respect to VDDCP	20Hz -2kHz 20kHz	70 50			dB

Phase Lock Loop (MCLK)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Input Jitter		cycle to cycle			35	Ps
		rms			100	Ps
Input Impedance		DC impedance > 10 MΩ	300 0.5	 1	 2	Ω pF
Interface mode (MCLK is 256 Fs, PLL off)						
Input frequency	F_{in}	256 Fs 128 Fs (96kHz)	11.289		12.288	MHz
Oscillator mode (MCLK from standard oscillator, PLL on)						
Input frequency	F_{in}	12.0, 13.0, 13.5, 14.4, 19.2, 19.68 MHz (x 1, 2 or 4) 32 kHz mode	10	 32.768	80	MHz kHz
I2S tracking range (SRM)		Maximum mismatch of I2S word-clock			4	%
I2S clock drift		Maximum frequency drift of I2S word clock			50	ppm/s
MCLK Shaper range[9]	$V_{IN\ AC}$	For AC coupling with internal clock shaping	300	500	1000	mV_{PP}

SIGNALS AND PACKAGING

Pin Description

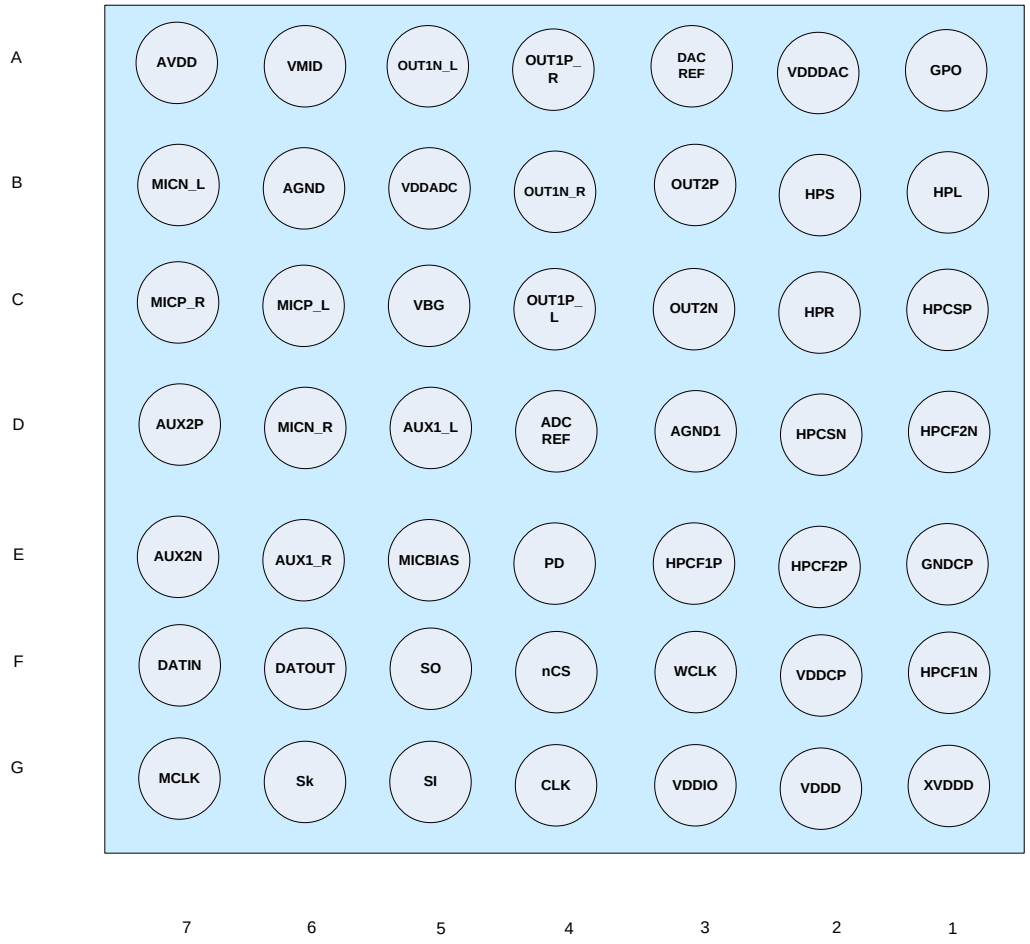


Figure 1: DA7210 pad arrangement for WLCSP version (Bottom view ball side up)

Below is a pin description for the DA7210. In the type column the following abbreviations have been used

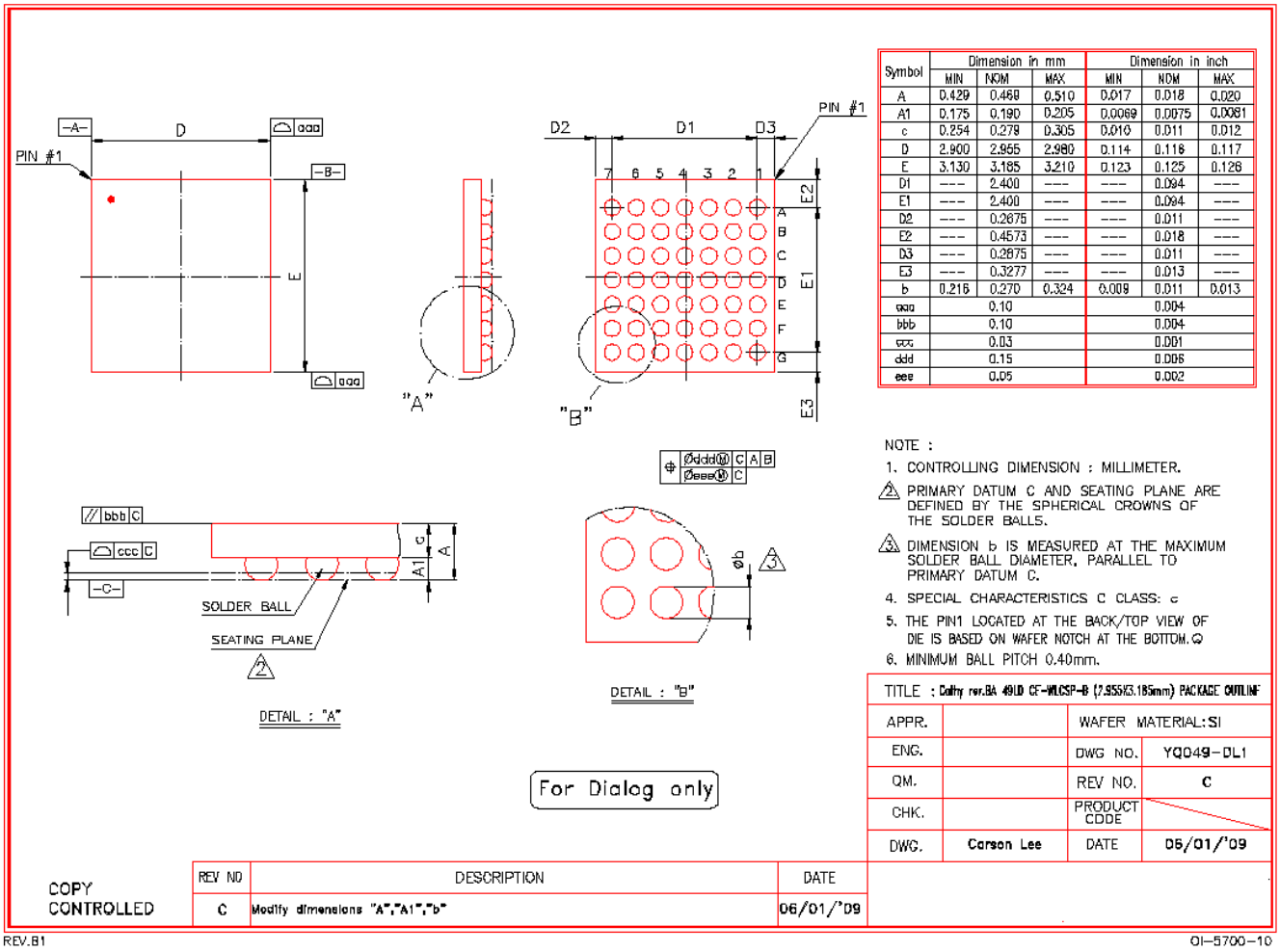
- PS, VSS Power Supply
- DI, DO, DIO Digital Input, Output, Input/Output
- AI, AO, AIO Analogue Input, Output, Input/Output

BUMP	NAME	TYPE	DESCRIPTION
Supplies and references			
7A	AVDD	PS	**Analogue supply (PLL, bias, etc)**
2A	VDDDAC	PS	**DAC and line output supplies**
5B	VDDADC	PS	**Mic input and ADC supplies**
2F	VDDCP	PS	**Charge pump supply**
1G	XVDDD	PS	**Digital supply (regulator input)**
2G	VDDD	PS	**Digital supply (1.5V, if on-chip regulator is active)**

3G	VDDDIO	PS	**Digital supply for I/O**
3A	DACREF	AI	**Decoupling capacitor for DAC**
4D	ADCREF	AI	**Decoupling capacitor for ADC**
6A	VMID	AI	**Decoupling capacitor for VMID**
5C	VBG	AI	**Decoupling capacitor for VBG**
5E	MICBIAS	AO	**Current supply for microphone (2mA max)**
1A	GPO	AIO	**General Purpose Output**
6B	AGND	VSS	**Analogue GND**
3D	AGND1	VSS	**Analogue GND**
1E	GNDCP	VSS	**Digital and charge pump ground, attached to paddle**
Control			
5F	SO	DO	**4-WIRE Data output**
5G	SI	DIO	**4-WIRE Data input/2-WIRE bidirectional Data**
6G	SK	DI	**4-WIRE/2-WIRE Clock**
4F	nCS	DI	**4-WIRE Chip select**
4E	PD	DI	**Power down signal (power down when high)**
2B	HPS	AIO	**Headphone Ground Sense**
Digital Audio Interface			
4G	CLK	DIO	**Digital Audio bit clock**
3F	WCLK	DIO	**Digital Audio left/right clock**
7F	DATIN	DI	**Digital Audio Data input**
6F	DATOUT	DO	**Digital Audio Data output**
7G	MCLK	DI	**Master clock input**
Audio In-/Outputs			
6C	MICP_L	AI	**Left channel differential microphone +ve input**
7B	MICN_L	AI	**Left channel differential microphone –ve input**
7C	MICP_R	AI	**Right channel differential microphone +ve input**
6D	MICN_R	AI	**Right channel differential microphone –ve input**
5D	AUX1_L	AI	**Left channel single-ended auxiliary input**
6E	AUX1_R	AI	**Right channel single-ended auxiliary input**
7D	AUX2P	AI	**2nd channel differential auxiliary +ve input**
7E	AUX2N	AI	**2nd channel differential auxiliary –ve input**
4C	OUT1P_L	AO	**Differential or single ended +ve line out left**
5A	OUT1N_L	AO	**Differential –ve line out left**
4A	OUT1P_R	AO	**Differential or single ended +ve line out right**
4B	OUT1N_R	AO	**Differential –ve line out right**
3C	OUT2N	AO	**2nd channel differential auxiliary -ve output**
3B	OUT2P	AO	**2nd channel differential auxiliary +ve output**
1B	HP_L	AO	**Left head phone amp output**
2C	HP_R	AO	**Right head phone amp output**
Charge pump			
3E	HPCF1P	PS	**Head phone amp charge pump floating cap1 +ve**
1F	HPCF1N	PS	**Head phone amp charge pump floating cap1 –ve**
2E	HPCF2P	PS	**Head phone amp charge pump floating cap2 +ve**
1D	HPCF2N	PS	**Head phone amp charge pump floating cap2 –ve**
1C	HPCSP	PS	**Head phone amp charge pump storage cap +ve**
2D	HPCSN	PS	**Head phone amp charge pump storage cap –ve**

PACKAGE DETAILS

Package Outline Drawings



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.429	0.469	0.510	0.017	0.018	0.020
A1	0.175	0.190	0.205	0.0069	0.0075	0.0081
c	0.254	0.279	0.305	0.010	0.011	0.012
D	2.900	2.955	2.980	0.114	0.116	0.117
E	3.130	3.185	3.210	0.123	0.125	0.126
D1	---	2.400	---	---	0.094	---
E1	---	2.400	---	---	0.094	---
D2	---	0.2675	---	---	0.011	---
E2	---	0.4573	---	---	0.018	---
D3	---	0.2875	---	---	0.011	---
E3	---	0.3277	---	---	0.013	---
b	0.216	0.270	0.324	0.009	0.011	0.013
aaa		0.10			0.004	
bbb		0.10			0.004	
ccc		0.03			0.001	
ddd		0.15			0.006	
eee		0.05			0.002	

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: c
5. THE PIN1 LOCATED AT THE BACK/TOP VIEW OF DIE IS BASED ON WAFER NOTCH AT THE BOTTOM.
6. MINIMUM BALL PITCH 0.40mm.

TITLE : Dolfin rev.BA 49LD CF-WLCSP-B (7.955X3.185mm) PACKAGE OUTLINE			
APPR.		WAFER MATERIAL: SI	
ENG.		DWG NO.	YQ049-DL1
QM.		REV NO.	C
CHK.		PRODUCT CODE	
DWG.	Carson Lee	DATE	06/01/'09

COPY CONTROLLED	REV NO	DESCRIPTION	DATE
	C	Modify dimensions "A","A1","b"	06/01/'09

REV.B1 OI-5700-10

This package is a 49 bump WLCSP 0.4mm pitch

ORDERING INFORMATION

Part Number	Package	Shipment Form	Pack quantity
DA7210-00UC6	49-bump CSP Pb-free/green	Waffle pack	900 pcs.
DA7210-00UC2	49-bumo CSP Pb-free/green	T&R	2,000 pcs.

Data Sheet Status Definitions

The Data Sheet version consists of two characters, a numeral followed by a lower-case alphabetic character. The numeral indicates Product Status (see table below), and the alphabetic character indicates the document revision level.
Notes:

Version	Data Sheet Status	Product Status	Definition
1a – 1z	Draft	Development	Version 1 Data Sheets contain pre-tapeout information from the objective design specification. Dialog reserves the right to change the specification in any manner without notice
2a – 2z	Preliminary	Qualification	Version 2 data sheets contain information on post-tapeout and pre-volume production products. Dialog reserves the right to change the specification in any manner without notice, in order to supply the best possible product by improvements to the design. Relevant changes will be communicated via Dialog's Sales and Marketing departments
3a – 3z	Released	Production	Version 3 Data Sheets contain information on volume production products. Dialog reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notification

1. To avoid confusion, the following alphabetic characters shall not be used in document version references: **i, j, l, o**.
2. Please consult the latest issued version of the data sheet before initiating or completing a design.
3. The product status of the device may have changed since this data sheet was published.
Please contact Dialog for the latest information.

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