ANALOG DEVICES

ADE9153A Technical Reference Manual

UG-1247

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Functionality and Features of the ADE9153A Energy Metering IC with Autocalibration

SCOPE

This reference manual provides a detailed description of the ADE9153A functionality and features. This reference manual must be used in conjunction with the ADE9153A data sheet.

Note that, throughout this reference manual, multifunction pins, such as ZX/DREADY/CF2, are referred to either by the entire pin name or by a single function of the pin, for example, CF2, when only that function is relevant.

FUNCTIONAL BLOCK DIAGRAM AND APPLICATION CIRCUIT

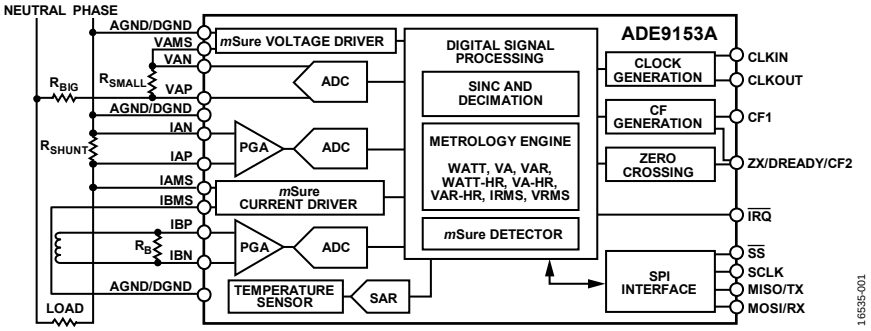

Figure 1.

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REVISION HISTORY

2/2018—Revision 0: Initial Version

ANALOG-TO-DIGITAL CONVERTER (ADC)

OVERVIEW

The ADE9153A incorporates three independent, second-order, sigma delta (Σ-Δ) ADCs that sample simultaneously. Each ADC is 24 bits; Current Channel A supports a pseudo differential input with the signal on the IAP pin, Current Channel B supports a fully differential signal, and the voltage channel supports a pseudo differential signal. The ADE9153A includes a low noise, low drift, internal band gap reference. Set EXT_REF (Bit 15 in the CONFIG1 register) if using an external voltage reference. The Current Channel A ADC contains a programmable gain amplifier (PGA) that allows gain values of 16, 24, 32, or 38.4. Current Channel B allows gain values of 1, 2, or 4.

ANALOG INPUT CONFIGURATION

Current Channel A Inputs

Current Channel A supports a pseudo differential input with the signal on the IAP pin. If, for layout purposes, it is easier to have the signal on the IAN pin, clear the AI_SWAP bit in the AI_PGAGAIN register to 0. The input signals on the IAP pin and the IAN pin must not exceed 0.1125 V, relative to the analog ground reference (AGND). The maximum allowed common-mode voltage at the IAP pin and the IAN pin must not exceed ±0.05 V.

Figure 3 shows the maximum input signal with pseudo differential signals, similar to those obtained when sensing the mains current signal through a shunt current sensor.

The following conditions must be met for the input signals with a gain value of 16:

- |IAP and IAN| ≤ 0.1125 V.
- |IAP − IPN| ≤ (1/AI_PGAGAIN) V peak = 0.0625 V peak (where AI_PGAGAIN is 16×).

Voltage Channel Inputs

The voltage channel is a pseudo differential input with the signal on the VAP pin. Short the VAMS pin directly to the VAN pin; this creates a common-mode voltage of 0.8 V on VAN, which is necessary for *m*Sure® functionality on the voltage channel. The voltage on the VAP pin has a full-scale level of ±0.5 V, with a 0.8 V common-mode voltage on this channel, resulting in a maximum value of 1.3 V. Do not connect the VAP pin or the VAN pin to AGND or DGND.

Figure 5 shows the maximum input signal with pseudo differential signals, similar to those obtained when sensing the mains voltage signal through potential divider.

The following conditions must be met for the input signals with a gain value of 1:

- 0 V ≤ |VAP and VAN | ≤ +1.35 V.
- |VAP − VAN| ≤ +0.5 V peak.

Current Channel B Inputs

Current Channel B has fully differential inputs. The input signals on the IBP pin and the IBN pin must not exceed 1.45 V or go below 0.35 V, relative to AGND.

The differential full-scale input range of the ADC is ±1 V peak (0.707 V rms), and the common-mode voltage on Current Channel B is set internally by the IC. Do not connect the IBP pin or the IBN pin to AGND or DGND.

Figure 2 and Figure 3 show two common types of input signals for an energy metering application. Figure 2 shows the maximum input allowed with differential antiphase signals. A current transformer with burden resistors generates differential, antiphase signals. Current Channel B is connected in such a configuration. Figure 3 shows the maximum input signal with pseudo differential signals, similar to those obtained when sensing the neutral current using a Rogowski coil current sensor.

The following conditions must be met for the input signals with a gain value of 1:

- 0.3 V ≤ |IBP and IBN | ≤ +1.5 V.
- |IBP − IBN| ≤ +1 V peak.

Current Channel B contains a PGA that allows a gain value of 1, 2, or 4. The ADC produces full-scale output codes with an input of ±1 V. With a gain of 1, this full-scale output corresponds to a differential antiphase input of 0.707 V rms, as shown in Figure 2. At a gain of 2, full-scale output codes are produced with an input of 0.353 V rms, as shown in Figure 3. At a gain of 4, full-scale output codes are generated with a 0.1765 V rms input signal. Note that the voltages on the IBP pin and the IBN pin must be within 0.35 V and 1.45 V, as specified in the ADE9153A data sheet.

Write to the BI_PGAGAIN register to configure the PGA gain for Current Channel B.

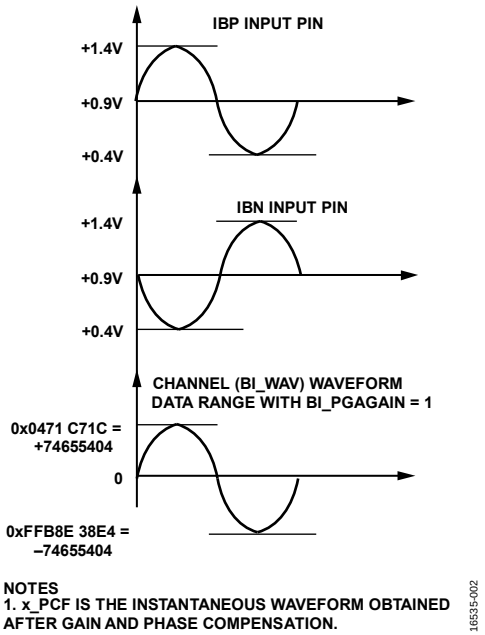

Figure 2. Maximum Input Signal with Differential Antiphase Input, Internal Common-Mode Voltage = 0.9 V, Gain = 1

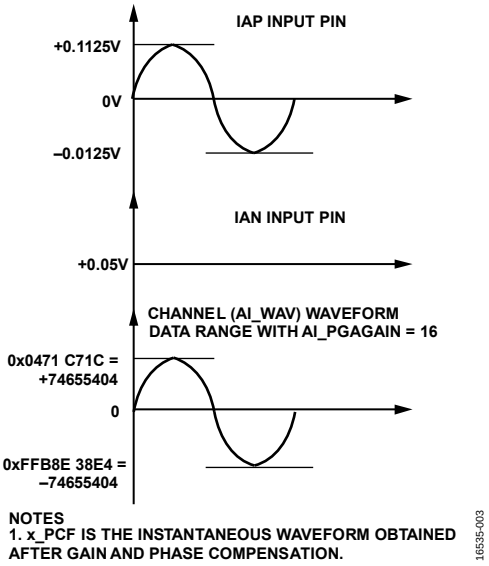

Figure 3. Maximum Input Signal with Pseudo Differential Input, Common-Mode Voltage = 0.05 V, Gain = 1

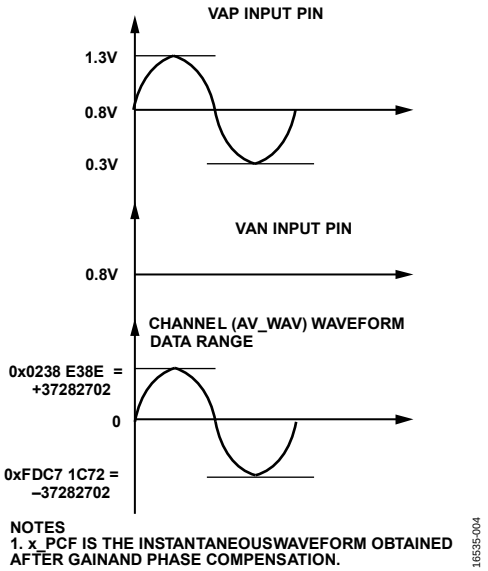

Figure 4. Maximum Input Signal with Pseudo Differential Input, Internal Common-Mode Voltage = 0.8 V, Gain = 1

The ADC on Current Channel A contains a PGA that allows gain values of 16, 24, 32, or 38.4. The ADC produces full-scale output codes with an input of ±0.707 V rms. With a gain of 16, this full-scale input corresponds to a pseudo differential input of 0.044 V rms. At a gain of 38.4, full-scale output codes are produced with an input of 0.018 V rms. Write the AI_GAIN bits in the AI_PGAGAIN register to configure the gain for each channel.

Interfacing to Current and Voltage Sensors

Figure 5 and Figure 6 show the typical circuits to connect to shunt and current transformer sensors. Figure 7 shows the typical interface circuit to measure the mains voltage. The antialiasing filter is not shown.

The antialiasing filter corner is chosen around 10 kHz to provide sufficient attenuation of out of band signals near the modulator clock frequency. The same RC filter corner is also used on voltage channels to avoid phase errors between the current and voltage signals.

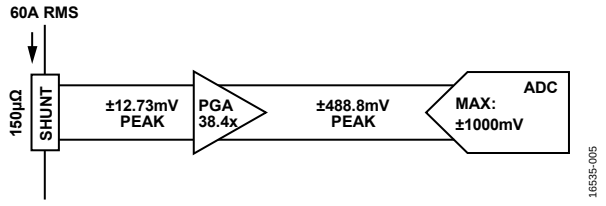

Figure 5. Application Circuit with a Shunt Current Sensor on Current Channel A

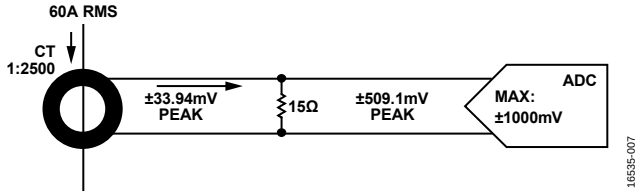

Figure 6. Application Circuit with a Current Transformer Current Sensor on Current Channel B

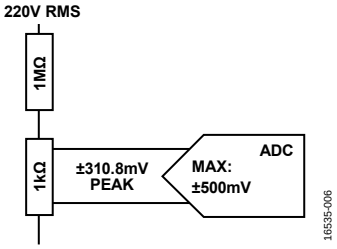

Figure 7. Application Circuit with Voltage Sensed Through a Resistor Divider

For proper function of the *m*Sure features on Current Channel A and Current Channel B, the resistance of the traces, wires, and shunt must be less than 2 Ω. For proper function of the *m*Sure features on the voltage channel, the total resistance of the voltage divider must be greater than 900 kΩ. The *m*Sure feature is only accurate when the line voltage is less than 440 V rms; therefore, if this voltage is exceeded, do not run *m*Sure on the voltage channel.

INTERNAL RF IMMUNITY FILTER

Energy metering applications require the meter to be immune to external radio frequency fields of 30 V/m, from 80 MHz up to 10 GHz, according to IEC 61000-4-3. The ADE9153A has internal antialiasing filters to improve performance in this testing because it is difficult to filter these signals externally. The second-order, internal low-pass filter has a corner frequency of 10 MHz. Note that external antialiasing filters are required to attenuate frequencies above 10 kHz, as described in the Interfacing to Current and Voltage Sensors section.

OUTPUT DATA RATES AND FORMAT

When a conversion is complete, the DREADY bit of the status register is set to 1. For the ADE9153A, the modulator sampling rate (MODCLK) is fixed at 1.024 MHz (CLKIN/12 = 12.288 MHz/12). The output data rate of the sinc4 filter is 16 kHz (SINC_ODR = MODCLK/64), whereas the low-pass filter/decimator stage yields an output rate four times slower than the sinc4 filter output rate. Figure 8 shows the digital filtering, which takes the 1.024 MHz ADC samples and creates waveform information at a decimated rate of 16 kHz or 4 kHz.

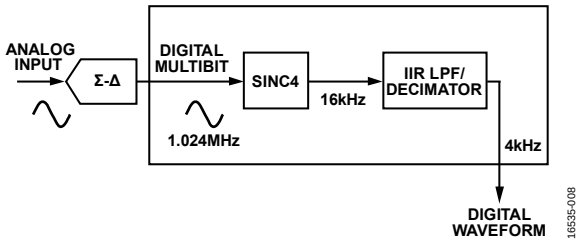

Figure 8. Datapath Following the ADC Stage

The output data rates are summarized in Table 1.

Table 1. Output Data Rates

Parameter	Output Data Rate
CLKIN Frequency	12.288 MHz
ADC Modulator Clock, MODCLK	1.024 MHz
Sinc Output Data Rate, SINC_ODR	16 kHz
Low-Pass Filter Output Data Rate	4 kHz
3 dB Bandwidth	0.672 kHz

VOLTAGE REFERENCE

The ADE9153A supports a 1.25 V internal reference. The temperature drift of the reference voltage is ±5 ppm/°C typical, ±30 ppm/°C maximum. An external reference can be connected between the REFIN pin and the AGND pin. To disable the internal reference buffer, set the EXT_REF bit of the CONFIG1 register when using an external voltage reference.

CRYSTAL OSCILLATOR AND EXTERNAL CLOCK

The ADE9153A contains a crystal oscillator. Alternatively, a digital clock signal can be applied at the CLKIN pin of the ADE9153A.

When a crystal is used as the clock source for the ADE9153A, attach the crystal and the ceramic capacitors, with capacitances of C_{L1} and C_{L2}, as shown in Figure 9. It is not recommended to attach an external feedback resistor in parallel to the crystal.

When a digital clock signal is applied at the CLKIN pin, the inverted output is available at the CLKOUT pin. This output is not buffered internally and cannot drive any other external devices directly.

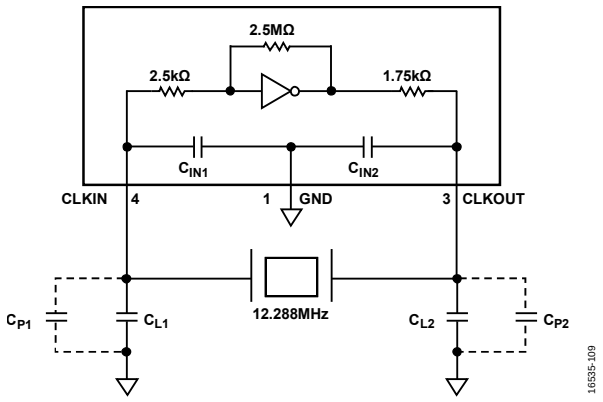

Figure 9. Crystal Application Circuit

Crystal Selection

The transconductance of the crystal oscillator circuit in the ADE9153A, g_m, is provided in the ADE9153A data sheet. It is recommended to have three to five times more g_m than the calculated critical value, $g_{m\ CRITICAL}$, for the crystal.

The following equation shows how to calculate $g_{m\ CRITICAL}$ for the crystal from information given in the crystal data sheet:

$$g_{m\ CRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2 \times \pi \times f_{CLK})^2 \times (C0 + C_L)^2$$

where:

$g_{mCRITICAL}$ is the minimum gain required to start the crystal, expressed in mA/V.
ESR_{MAX} is the maximum effective series resistance (ESR), expressed in ohms.
f_{CLK} = 12.288 MHz, expressed in Hz as 12.288×10^6.
$C0$ is the maximum shunt capacitance, expressed in farads.
C_L is the load capacitance, expressed in farads.

Crystals with low ESR and smaller load capacitance have a lower $g_{m\ CRITICAL}$ value and are easier to drive.

The evaluation board of the ADE9153A uses a crystal manufactured by Abracon (ABLS2-12.288MHZ-D4Y-T), which has a maximum ESR of 50 Ω, a load capacitance of 18 pF, and a maximum shunt capacitance of 7 pF, resulting in $g_{mCRITICAL}$ = 0.75 mA/V, as follows:

$$g_{m\ CRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2 \times \pi \times f_{CLK})^2 \times (C0 + C_L)^2$$

$$g_{m\ CRITICAL} = 4 \times 40 \times 1000 \times (2 \times \pi \times 12.288 \times 10^6)^2 \times (7 \times 10^{-12} + 8 \times 10^{-12})^2 = 0.86$$

The gain of the crystal oscillator circuit in the ADE9153A (g_m) provided in the data sheet is more than 5× $g_{m\ CRITICAL}$; therefore, there is sufficient margin to start up this crystal.

Load Capacitor Calculation

Crystal manufacturers specify the combined load capacitance across the crystal, C_L. The capacitances in Figure 9 are described as follows:

- C_{P1} and C_{P2} are parasitic capacitances on the clock pins formed due to printed circuit board (PCB) traces.
- C_{IN1} and C_{IN2} are internal capacitances of the CLKIN pin and CLKOUT pin, respectively.
- C_{L1} and C_{L2} are selected load capacitors to obtain the correct combined C_L value for the crystal.

C_{IN1} and C_{IN2} are 4 pF each, as shown in the ADE9153A data sheet. To find the values of C_{P1} and C_{P2}, measure the capacitance on each of the clock pins of the PCB, CLKIN and CLKOUT, respectively, with respect to the AGND pin. If the measurement is performed after soldering the IC to the PCB, subtract the 4 pF internal capacitance of the clock pins to find the actual value of the parasitic capacitance on each crystal pin.

To select the appropriate capacitance value for the ceramic capacitors, calculate C_{L1} and C_{L2} from the following equation:

$$C_L = [(C_{L1} + C_{P1} + C_{IN1}) \times (C_{L2} + C_{P2} + C_{IN2})]/(C_{L1} + C_{P1} + C_{IN1} + C_{L2} + C_{P2} + C_{IN2}) \quad (1)$$

Select C_{L1} and C_{L2} such that the total capacitance on each clock pins is

$$C_{L1} + C_{P1} + C_{IN1} = C_{L2} + C_{P2} + C_{IN2} \quad (2)$$

Calculate the values of C_{L1} and C_{L2} using Equation 1 and Equation 2.

Load Capacitor Calculation Example

If a crystal with a load capacitance specification of 18 pF is selected and the measured parasitic capacitances from the PCB traces are $C_{P1} = C_{P2}$ = 2 pF, Equation 1 implies that

$$C_L = [(C_{L1} + C_{P1} + C_{IN1}) \times (C_{L2} + C_{P2} + C_{IN2})]/(C_{L1} + C_{P1} + C_{IN1} + C_{L2} + C_{P2} + C_{IN2})$$

$$18\ pF = [(C_{L1} + 2\ pF + 4\ pF) \times (C_{L2} + 2\ pF + 4\ pF)]/(C_{L1} + 2\ pF + 4\ pF + C_{L2} + 2\ pF + 4\ pF)$$

Assuming that $C_{L1} = C_{L2}$, to satisfy Equation 2,

$$18\ pF = [(C_{L1} + 6\ pF) \times (C_{L1} + 6\ pF)]/(C_{L1} + 6\ pF + C_{L1} + 6\ pF)$$

$$18\ pF = [(C_{L1} + 6\ pF) \times (C_{L1} + 6\ pF)]/[2 \times (C_{L1} + 6\ pF)]$$

$$18\ pF = (C_{L1} + 6\ pF)/2$$

Therefore, $C_{L1} = C_{L2}$ = 30 pF.

Based on this example, 30 pF ceramic capacitors are selected for C_{L1} and C_{L2}.

POWER MANAGEMENT

POWER-ON SEQUENCE

After power is applied to the VDD pin of the ADE9153A, the power-on sequence is initiated. If the $\overline{\text{RESET}}$ pin is high, the AVDD, DVDD, and VDDOUT2P5 low dropout regulators (LDOs) are turned on when VDD reaches 2.4 V to 2.6 V. If the $\overline{\text{RESET}}$ pin is low, the LDOs are not turned on. The LDOs are arranged sequentially and a clamp limits the current used to charge the AVDD, DVDD, and VDDOUT2P5 LDOs to 23 mA per LDO. The AVDD LDO powers up first, then the DVDD LDO powers up 1 ms later, and lastly, the VDDOUT2P5 LDO powers up 1 ms later.

When AVDD, DVDD, and VDDOUT2P5 are all above 1.3 V to 1.5 V, and VDD is above 2.4 V to 2.6 V, a 20 ms timer starts and allows additional time for the supplies to achieve their normal potentials (with VDD between 2.97 V and 3.63 V, AVDD at 1.9 V, DVDD at 1.7 V, and VDDOUT2P5 at 2.5 V). After this timer elapses, the crystal oscillator starts.

The RSTDONE interrupt is triggered 26 ms after the crystal oscillator starts, bringing the $\overline{\text{IRQ}}$ pin low and setting the RSTDONE bit in the status register. The RSTDONE bit being set indicates to the user that the ADE9153A finished the power-up sequence. The user can then configure the IC via the serial peripheral interface (SPI). After configuring the device, write the run register to start the DSP so that it starts making measurements. Note that Address 0x000 through Address 0x0FF and Address 0x200 through Address 0x61A are restored to their default values during power-on. Address 0x200 through Address 0x3FF are cleared within 500 µs from when the run register value changes from 0x0000 to 0x0001.

BROWNOUT DETECTION

Power-on reset (POR) circuits monitor the VDD, AVDD, DVDD, and VDDOUT2P5 supplies. If AVDD, DVDD, or VDDOUT2P5 drops below 1.3 V to 1.5 V, or if VDD drops below 2.4 V to 2.6 V, the IC is held in reset and the power-on sequence begins again, waiting until AVDD, DVDD, and VDDOUT2P5 are above 1.3 V to 1.5 V and VDD is above 2.4 V to 2.6 V before starting the 20 ms POR timer. An RSTDONE interrupt on the $\overline{\text{IRQ}}$ pin indicates when the ADE9153A can be reinitialized via the SPI.

RESET

If the $\overline{\text{RESET}}$ pin goes low for 1 µs, or if the SWRST bit is set in the CONFIG1 register to initiate a software reset, the AVDD, DVDD, and VDDOUT2P5 LDOs are turned off. The power-on sequence resumes from the point where the AVDD, DVDD, and VDDOUT2P5 LDOs are turned on (see the Power-On Sequence section for details).

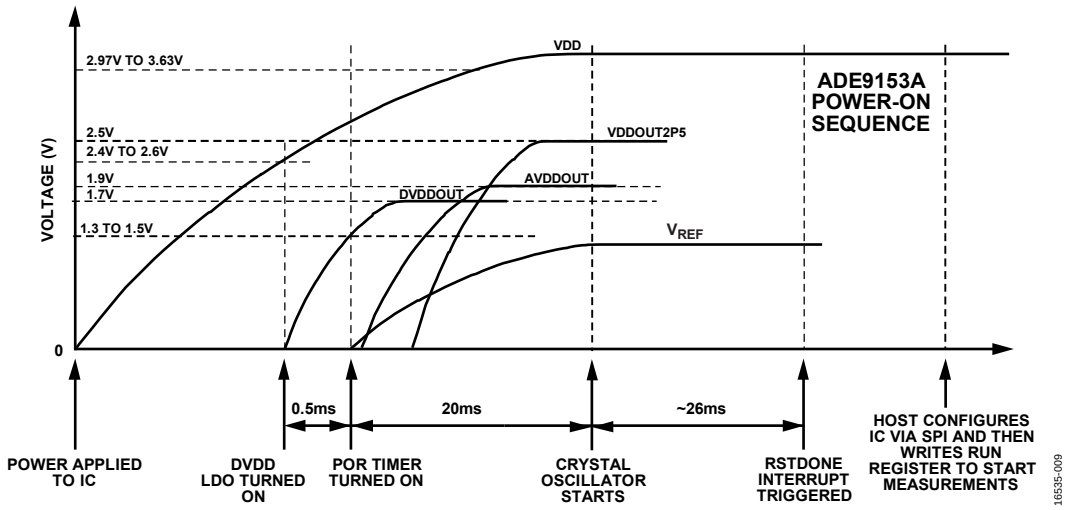

Figure 10. ADE9153A Power-On Sequence

*m*SURE ENABLED FEATURES

The ADE9153A offers *m*Sure autocalibration, enabling the meter to perform calibration on the currents and voltage channels automatically without the use of a reference meter. Autocalibration features two main components explained in this section that dictate the performance: absolute accuracy and the speed of convergence. Use the information in this section together with the information in the ADE9153A data sheet.

*m*SURE TERMINOLOGY

Speed of Convergence

The speed of convergence is the time it takes for *m*Sure to reach a certain level of accuracy. This speed, or time required, is logarithmically proportional to the required accuracy. In other words, if a greater accuracy is required in the *m*Sure autocalibration, the time required increases logarithmically.

Similarly, the speed is related to the power mode in which *m*Sure is being run; the lower the power mode, the slower the speed of convergence. The speed of convergence determines the time it takes to complete the autocalibration reaching a certain specified accuracy.

Absolute Accuracy

Absolute accuracy takes into account the accuracy of the *m*Sure reference . The speed of convergence to reach this accuracy depends on the time of an *m*Sure autocalibration run. The longer the time of an *m*Sure autocalibration run, the greater the accuracy.

Certainty of Estimation (CERT)

The certainty of the *m*Sure estimation, CERT, which is also referred to as certainty, is a metric of the precision of the *m*Sure measurement. This certainty is displayed as a percentage; the lower the value, the more confidence there is in the estimation value.

Conversion Constant (CC)

The conversion constant (CC) is the value that *m*Sure returns when estimating the transfer function of the sensor and front end. This value is in units of A/code or V/code, depending on which channel the estimation occurs.

AUTOCALIBRATION USING *m*SURE

The ADE9153A performs autocalibration of the meter when an accurate source or reference meter is not required. Because the *m*Sure technology is able to find the CC of each channel, the meter can be gain calibrated with the only requirement being that the meter is powered.

After the meter is powered, the autocalibration feature can be run on each channel sequentially using the MS_ACAL_CFG register to enable a run on one channel at a time. Each channel can then be run for a set amount of time. After the runs on each channel are finished, the certainty of the measurements are confirmed with the MS_ACAL_xCERT registers. Then, the MS_ACAL_xCC register can be used to calculate an xGAIN value to calibrate the meter.

Use the following procedure to properly run *m*Sure autocalibration on a channel (ensure that the meter is properly set up with all default values before performing a run):

1. Check the MS_SYSRDYP bit in the MS_STATUS_CURRENT register. This bit is set if the system is ready to run. Do not run the system if this bit is not set.
2. Configure the MS_ACAL_CFG register with the correct channel and power mode in which to run.
   a. Set only one bit from the AUTOCAL_AI, AUTOCAL_BI, or AUTOCAL_AV registers, depending on the channel being checked.
   b. Set ACALMODE_AI and ACALMODE_BI based on the power mode being run; normal mode is recommended.
   c. Set ACAL_RUN and ACAL_MODE to tell the system to run with the settings previously described.
3. Either wait for a set amount of time based on the specifications in the ADE9153A data sheet, or monitor the appropriate MS_ACAL_xCERT register until it drops to an appropriate level. This CERT register gives a value in ppm based on the absolute uncertainty in the CC measurement. The MS_READY bit in the MS_STATUS_IRQ register indicates when the CC and CERT registers update during a run of *m*Sure.
4. When the time or desired certainty is met, stop the run by writing MS_ACAL_CFG to 1.
5. Read the results from the MS_ACAL_xCC and MS_ACAL_xCERT registers to obtain the CC of that channel and the certainty in that reading.
6. Repeat Step 1 through Step 5 for all channels that must be calibrated.
7. Before starting another run on any channel, ensure that either the MS_SYSRDYP bit in the MS_STATUS_CURRENT register is set, or the MS_SYSRDY bit in the MS_STATUS_IRQ register is triggered to indicate that a new run is ready to start.
8. After autocalibration runs on the desired channels, take the MS_ACAL_AICC, MS_ACAL_BICC, and MS_ACAL_AVCC values and find the scale factor between the measured CC values and the target CC for the meter. Then, apply that scale factor to the xGAIN register for the appropriate channel.

MEASUREMENTS

CURRENT CHANNEL MEASUREMENT UPDATE RATES

Table 2 indicates the registers that hold current channel measurements and the rate at which they update.

Table 2. Current Channel Measurement Update Rates

Register Name	Description	Update Rate
AI_WAV	Instantaneous current on Current Channel A	f_{DSP} = 4 kSPS
BI_WAV	Instantaneous current on Current Channel B	f_{DSP} = 4 kSPS
AIRMS	Filter-based total rms of IA	f_{DSP} = 4 kSPS
BIRMS	Filter-based total rms of IB	f_{DSP} = 4 kSPS
IPEAK	Peak current channel sample; see the Peak Detection section	f_{DSP} = 4 kSPS
ANGL_x_x	Voltage to current or current to current phase angle; see the Angle Measurement section	CLKIN/24 = 512 kSPS

The current channel ADC waveforms can be sampled at 4 kSPS, following a sinc4 filter and an infinite impulse response (IIR), low-pass filter. Gain and phase compensation are applied, creating the AI_WAV and BI_WAV instantaneous current waveforms that update at 4 kSPS. The AI_WAV and BI_WAV waveforms are used for total active power, IRMS, VA, and fundamental VAR calculations. Angle measurements indicate the time between the current channel zero crossings and the voltage channel zero crossings, with the results being updated at 512 kHz in the ANGL_AV_AI and ANGL_AI_BI registers.

Current Channel Gain, AIGAIN and BIGAIN

There are many sources of gain error in an energy metering system. The current sensor (current transformer, burden resistors, and shunts) may introduce some gain error. There is device to device gain error in the ADE9153A device itself and the voltage reference may have some variation (see the ADE9153A data sheet for the device specifications).

The ADE9153A provides a current gain calibration register so that each metering device has the same current channel scaling.

The current channel gain varies with xIGAIN, as shown in the following equation:

$$Current\ Channel\ Gain = \left(1 + \frac{xIGAIN}{2^{27}}\right)$$

Use this equation to calculate the xIGAIN value for a given current channel gain:

$$xIGAIN = \text{round}((Current\ Channel\ Gain - 1) \times 2^{27})$$

The current channel gain can be positive or negative.

For example, to gain the current channel up by 10% to 1.1,

$$xIGAIN = \text{round}((1.1 - 1) \times 2^{27} = 13421773 = 0x00CC\_CCCD$$

To gain the current channel down by 10% to 0.9,

$$xIGAIN = \text{round}((0.9 - 1) \times 2^{27} = -1 \times 10^{7} = 0xFF33\_3333$$

It is also possible to use the current channel gain register to change the sign of the current channel, which can be useful if the current sensor is installed backwards. To compensate for this backward installation, use a current channel gain value of −1.

$$xIGAIN = \text{round}((-1 - 1) \times 2^{27} = -268435456 = 0xF000\_0000$$

For a given phase,

$$|Current\ Channel\ Gain \times Voltage\ Channel\ Gain \times Power\ Gain| \leq 3.75$$

High-Pass Filter (HPF)

A high-pass filter (HPF) is provided to remove dc offsets for accurate rms and energy measurements.

The ADE9153A HPF on the current channel and voltage channel is enabled by default. Disable the filter by writing Bit 0 (HPFDIS) in the CONFIG0 register to one.

It is recommended to leave the HPF enabled to achieve the metering performance listed in the specifications in the ADE9153A data sheet.

The HPF corner is selectable using the HPF_CRN bits in the CONFIG2 register (see Table 3).

Table 3. HPF Corner Gain with 50 Hz Input Signal

HPF_CRN	$f_{-3\ dB}$ (Hz)	HPF Gain	Settling Time to 1% for DC Step (sec)	Settling Time to 0.1% for DC Step (sec)
0	38.695	0.8	0.0178	0.0268
1	19.6375	0.94	0.0363	0.0544
2	9.895	0.99	0.0731	0.1097
3	4.9675	1.00	0.1468	0.2202
4	2.49	1.00	0.2942	0.4412
5	1.2475	1.00	0.5889	0.8833
6 (Default)	0.625	1.00	1.1784	1.7675
7	0.3125	1.00	2.3573	3.5359

Digital Integrator

A digital integrator is included to allow interfacing to a di/dt current sensor, also known as a Rogowski coil. The integrator is only available on Current Channel B and no *m*Sure features are available for use with a Rogowski coil as the current sensor.

The di/dt sensor output increases by 20 dB/decade over the frequency range. To compensate for this increase, the digital integrator applies −20 dB/decade gain with a phase shift of approximately −90°.

A second-order antialiasing filter is required to avoid noise aliasing back in the band of interest when the ADC is sampling.

To enable the digital integrator on Current Channel B, set the INTEN_BI bit in the CONFIG0 register.

Phase Compensation

The ADE9153A phase compensation uses a digital filter to achieve a phase adjustment of ±0.001°. This high resolution improves the total active energy and reactive energy performance at low power factors. Both Current Channel A and Current Channel B have a phase compensation register to correct for phase error.

The phase calibration range is −15° to +4.5° at 50 Hz.

To achieve this phase compensation, the voltage channel is delayed by one 4 kSPS sample, 4.5° at 50 Hz.

$$Voltage\ Channel\ Delay\ (\text{Degrees}) = \left(\frac{f_{LINE}}{f_{DSP}} \times 360\ ^\circ\right)$$

$$Voltage\ Channel\ Delay\ (\text{Degrees}) = \left(\frac{50}{4000} \times 360^\circ\right) = 4.5^\circ$$

The current channel is then delayed by a digital filter, according to the value programmed in the APHASECAL register. The resulting phase correction depends on the value in the APHASECAL register. The following equation gives the phase correction between the input current and voltage after the combined voltage and current delays. In the following formula, phase correction is positive to correct a current that lags the voltage, and phase correction is negative to correct a situation in which the current leads the voltage, a scenario commonly seen with a current transformer:

$$Phase\ Correction\ (\text{Degrees}) =$$

$$\arctan\left(\frac{-\sin\omega}{xPHASECAL \times 2^{-27} + \cos\omega}\right)$$

$$-\arctan\left(\frac{-xPHASECAL \times 2^{-27} \times \sin\omega}{1 + xPHASECAL \times 2^{-27} + \cos\omega}\right)$$

where $\omega = 2 \times \pi \times f_{LINE}/f_{DSP}$.

Calculate the xPHASECAL register value from the desired phase correction according to the following equation:

$$xPHASECAL = \left(\frac{\sin(\varphi - \omega) + \sin\omega}{\sin(2 \times \omega - \varphi)}\right) \times 2^{27}$$

For example, if f_{LINE} = 50 Hz, f_{DSP} = 4 kHz, and the current leads the voltage by 0.1°, then phase correction = −0.1°. Write xPHASECAL = 0xFFE9 7889 to correct for this phase difference.

$\omega = 2 \times \pi \times 50/4000 = 0.07854$

$$xPHASECAL = \left(\frac{\sin(Radians(-0.1) - 0.07854) + \sin 0.07854}{\sin(2 \times 0.07854 - Radians(-0.1))}\right) \times 2^{27} =$$

−1476471 = 0xFFE9_7889

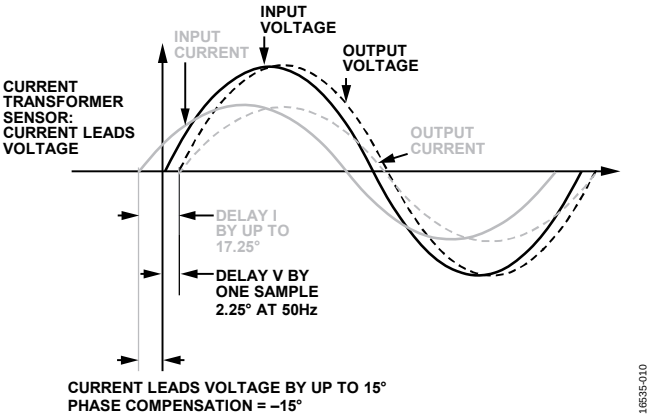

Figure 11. Phase Compensation Example for a Current Transformer Where the Current Leads the Voltage

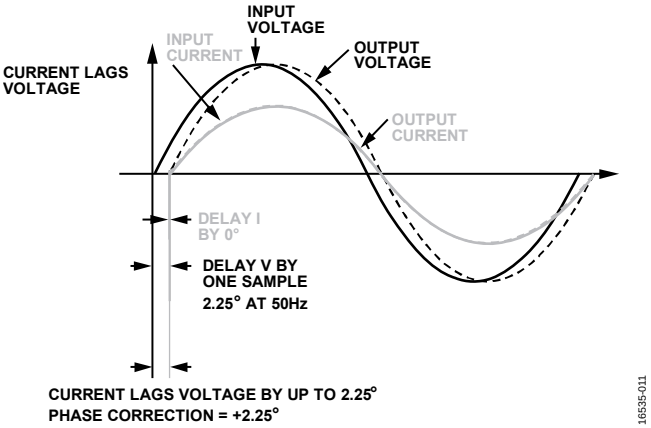

Figure 12. Phase Compensation Example for a Current Transformer Where the Current Lags the Voltage

Using the following equation, it can be seen that at 60 Hz, the voltage channel delay is 5.4°:

$$Voltage\ Channel\ Delay\ (\text{Degrees}) = \left(\frac{60}{4000} \times 360^\circ\right) = 5.4^\circ$$

This result leads to a phase calibration range of −15° to +5.4° at 60 Hz.

Voltage Channel Measurements

Table 4 indicates the registers that hold voltage channel measurements and the rate at which they update.

Table 4. Voltage Channel Measurement Update Rates

Register Name	Description	Update Rate
AV_WAV	Instantaneous voltage on the voltage channel	f_{DSP} = 4 kSPS
AVRMS	Filtered-based total rms of the voltage channel	f_{DSP} = 4 kSPS
VPEAK	Peak current channel sample; see the Peak Detection section	f_{DSP} = 4 kSPS
APERIOD	Line period measurement on the voltage channel	f_{DSP} = 4 kSPS
ANGL_Ax_xI	Voltage to current or current to current phase angle; see the Angle Measurement section	CLKIN/24 = 512 kSPS

Voltage Channel Gain

The AVGAIN register calibrates the voltage channel of each phase. The AVGAIN register has the same scaling as the AIGAIN register. See the Current Channel Gain, AIGAIN and BIGAIN section for the relevant equation.

FULL-SCALE CODES

Table 5 provides the expected codes when the ADC inputs are at full scale with the PGA gain set to 1.

Table 5. Full-Scale ADC Codes

Parameter	Output Code
AV_WAV at 4 kSPS	74,565,404
IRMS	52,725,703
VRMS	26,362,852
Total WATT and VA	10,356,306
Fundamental VAR	10,356,306
Fast IRMS½	52,725,703
Fast VRMS½	26,362,852

POWER AND FILTER-BASED RMS MEASUREMENT ALGORITHMS

Filter-Based Total RMS

The ADE9153A offers current and voltage rms measurements calculated by squaring the input signal, low-pass filtering, and then taking the square root of the result.

The low-pass filter, LPF2, extracts the rms value, attenuating harmonics of a 50 Hz or 60 Hz fundamental by at least 64 dB so that, at full scale, the variation in the calculated rms value is small (±0.064% error). The rms reading variation increases as the input signal decreases because the noise in the measurement increases.

Note that the xRMS register does not read 0 with the IAx, IBx, and VAx inputs shorted together.

The filter-based rms has a bandwidth of 1.6 kHz.

The rms calculations, one for each channel (AIRMS, BIRMS, and AVRMS) are updated every 4 kSPS.

The xIRMS value at full scale is 52,725,703 (decimal). The AVRMS value at full scale is 26,362,852 (decimal). The full scale is a function of the PGA gain on the current channels.

$$Full\ Scale = \frac{Full - Scale\ Input}{x\_PGAGAIN}$$

For high performance at small input signals below 3000:1, it is recommended to calibrate the offset of this measurement using the xRMS_OS register. It is recommended to calibrate the offset at the smallest input signal that requires good performance; do not calibrate this measurement with zero input signal.

The following equation indicates how the xRMS_OS register value modifies the result in the xRMS register.

$$xxRMS = \sqrt{xxRMS_0{}^2 + 2^{15} \times xxRMS\_OS}$$

where $xxRMS_0$ is the initial xRMS register value before offset calibration.

For example, if the expected AIRMS at 1000:1 is 52,725,703/1000 = 52,725 (decimal), and the AIRMS register reading is 53280 (decimal), the offset calibration register is

$$AIRMSOS = \frac{52725^2 - 53280^2}{2^{15}} = -1795\text{d} = 0\text{xFFFF8FD}$$

Table 6 shows the rms settling time to 99% of full scale for a 50 Hz signal.

Table 6. RMS Settling Time

Configuration	RMS Settling Time, Full Scale = 99% (sec)
Integrator On (Current Channel B), HPF On, and LPF2 On	1.09
Integrator Off, HPF On, and LPF2 On	0.96

Total Active Power

Total active power is commonly used for billing purposes and includes power on the fundamental and on the harmonics.

The total active power on each phase is calculated by first multiplying the xI_WAV and xV_WAV waveforms. Then, the result is low-pass filtered, unless the DISAPLPF bit in the CONFIG0 register is equal to 1. Finally, the APGAIN is applied to perform a gain correction and the AWATT_OS value is applied to correct the watt offset.

Figure 13 shows the relationship between the current (I) and voltage (V) input signals, as well as the instantaneous active power and low-pass filtered active power, assuming that I and V are at full scale with only the fundamental present and a power factor of 1.

If the DISAPLPF bit in the CONFIG0 register is equal to 1, AWATT reflects the instantaneous active power; if DISAPLPF is equal to 0, AWATT reflects the low-pass filtered active power, assuming APGAIN = 0 and AWATTOS = 0 (see Figure 13).

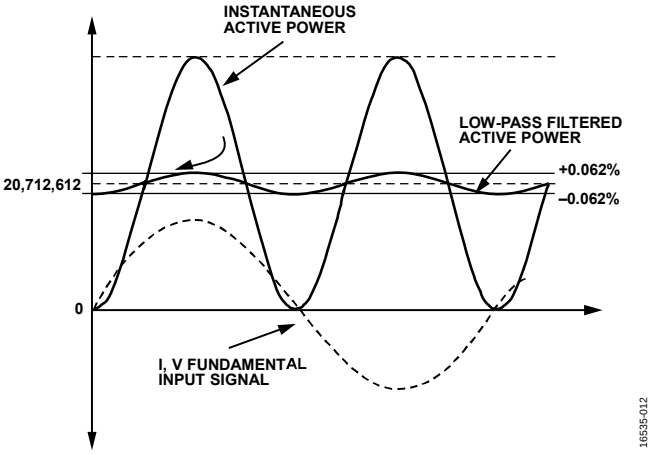

Figure 13. Instantaneous Active Power and Low-Pass Filtered Active Power at a Power Factor of 1

The low-pass filter, LPF2, extracts the total active power, attenuating harmonics of a 50 Hz or 60 Hz fundamental by 64 dB so that, at full scale, the variation in the low-pass filtered active power is very small, ±0.062%.

The resulting AWATT signal has an update rate of 4 kSPS and a bandwidth of 1.6 kHz.

The APGAIN register has the same scaling as the AIGAIN register. AWATT_OS has the same scaling as AWATT. AWATT can be calibrated using the energy or power registers. When using the power registers, AWATT_OS is calculated using the following equation:

$$AWATT\_OS = AWATT_{EXPECTED} - AWATT_{MEASURED}$$

The AWATT value with full-scale inputs and no gain is 10,356,306. Note that AFVAR and AVA have the same scaling; therefore, the same equation can be used for all three offsets.

$$AWATTOS = \frac{1}{\frac{AWATT\_FULL\_SCALE}{x}}$$

where:

AWATT_FULL_SCALE is the nominal AWATT value with full-scale inputs, 10,356,306.

x is the smallest power level to calibrate. For example, to calibrate the energy at 10,000 from full scale, x = 10,000.

$$AWATTOS = \frac{1}{\frac{20{,}712{,}612}{10{,}000}} = 0.05\%$$

Then, each bit in the AWATTOS register can correct an error of 0.05% at 10,000:1. In most applications, the total active power performance with small inputs is sufficient with AWATTOS at zero.

Table 7 shows the settling times for total active power for a 50 Hz signal.

Table 7. Total Active Power Settling Time

	Total Active Power Settling Time (sec)	
Configuration	**Full Scale = 99%**	**Full Scale = 99.90%**
HPF On and LPF2 On	0.85	1.2
HPF On and LPF2 Off	0.06	0.66

Fundamental Reactive Power

Fundamental reactive power gives only the reactive power at the fundamental frequency of the signal. The current channel, AI_WAV, is shifted by 90° at the fundamental. This signal is then multiplied by the voltage waveform, AV_WAV. The result is then low-pass filtered, unless the DISRPLPF bit in the CONFIG0 register is set to 1. Finally, the APGAIN value is applied to perform a gain correction, and the AFVAR_OS value is applied to correct the VAR offset. In most applications, the fundamental reactive power performance with small inputs is sufficient with AFVAR_OS at zero. AFVAR_OS has the same scaling as AFVAR; see the Total Active Power section to understand how to calculate this register value. Table 8 shows the settling times for total reactive power for a 50 Hz signal.

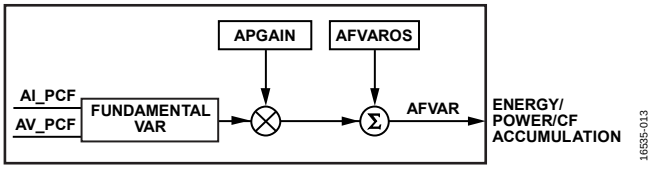

Figure 14. Fundamental Reactive Power, AFVAR

Table 8. Fundamental Reactive Power Settling Time

	Total Reactive Power Settling Time (sec)	
Configuration	**Full Scale = 99%**	**Full Scale = 99.90%**
HPF On and LPF2 On	0.86	1.11

For this fundamental measurement to work correctly, initialization of the network frequency and of the nominal voltage measured in the voltage channel is required. The SELFREQ bit in the ACCMODE register selects whether the system is 50 Hz or 60 Hz. For a 50 Hz system, clear the SELFREQ bit; for a 60 Hz system, set the SELFREQ bit to 1. The SELFREQ selection must be made prior to writing the run register to 1.

The VLEVEL register indicates the nominal value of the voltage channel. Calculate VLEVEL according to the following equation:

$$VLEVEL = x \times 1{,}114{,}084$$

where *x* is the dynamic range of the nominal input signal with respect to full scale.

After configuring these two parameters, SELFREQ and VLEVEL, the ADE9153A tracks the fundamental line frequency within ±5 Hz of the 50 Hz or 60 Hz frequency selected in SELFREQ. If a larger frequency range than ±5 Hz is required in the application, monitor the line period, xPERIOD, and change the SELFREQ selection accordingly. The run register must be set to zero before changing the SELFREQ setting and must then be set to one again.

The fundamental reactive power at a power factor of 0 has a similar ripple to the total active power at a power factor of 1 (see Figure 13).

The resulting AFVAR signal has an update rate of 4 kSPS and a bandwidth of 1.6 kHz.

Total Apparent Power

Apparent power is generated by multiplying the current rms measurement, AIRMS, by the corresponding voltage rms, AVRMS, and then applying a gain correction, APGAIN. The result is stored in the AVA register. Note that the offset of the total apparent power calculation is performed by calibrating the AIRMS and AVRMS measurements, using the AIRMS_OS and AVRMS_OS registers; see the Filter-Based Total RMS section for more information on the rms calculation.

The resulting AVA signal has an update rate of 4 kSPS and a bandwidth of 1.6 kHz.

In some applications, if there is a tamper detected on the voltage channel inputs, it is desirable to accumulate the apparent energy assuming that the voltage is at a nominal level. The ADE9153A offers a register, VNOM, that can be set to a value to correspond to, for example, 240 V rms. If the VNOMA_EN bit in the CONFIG0 register is set, VNOM is multiplied by AIRMS when calculating AVA.

Table 9 shows the settling times for total apparent power for a 50 Hz signal.

Table 9. Total Apparent Power Settling Time

Configuration	Total Apparent Power Settling Time, Full Scale = 99% (sec)
HPF On and LPF2 On	0.96

ENERGY MEASUREMENTS OVERVIEW

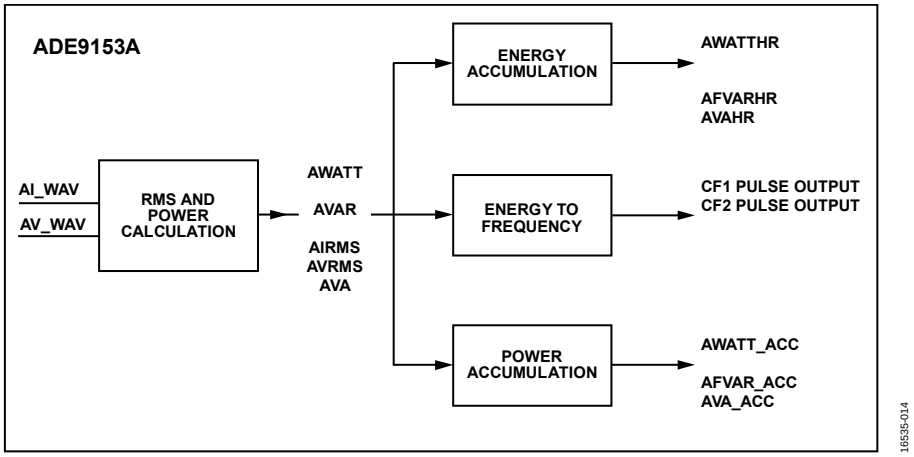

Figure 15. Power and Energy Calculations from the AI_WAV and AV_WAV Waveforms

Figure 15 shows how AI_WAV and AV_WAV are used to calculate rms and power calculations and how these results are accumulated into the AWATTHR and AWATT_ACC registers, as well as the CFx pulse outputs.

Energy Measurements Update Rate

Instantaneous power measurements, including AWATT, AVA, and AFVAR, update at a rate of f_{DSP} = 4 kSPS.

These measurements are accumulated into power measurements in the AWATT_ACC register, which updates at a user defined interval of up to 1 sec, depending on the selection in the PWR_TIME register.

Energy measurements update every f_{DSP} = 4 kSPS by default and can store up to 106 sec of accumulation at full scale. Alternatively, these registers can be set into a different accumulation mode in which they update after a user defined number of line cycles or samples.

The power factor measurement updates every 4096/4 kSPS = 1.024 sec.

The RMS_OC measurements update every ½ line cycle (10 ms at 50 Hz).

The SELFREQ bit in the ACCMODE register defines the network being used.

Table 10. Watt Related Register Update Rates

Register Name	Description	Update Rate
AWATT	Low-pass filtered total active power	4 kSPS
AWATT_ACC	Accumulated total active power	After the PWR_TIME 4 kSPS samples, from 500 µs to 2.048 sec
AWATTHR	Accumulated total active energy	According to the settings in EP_CFG and EP_TIME; holds up to 211 sec of energy at full scale
APF	Power factor[1]	Every 1.024 sec

[1] See the Power Factor section.

ENERGY ACCUMULATION

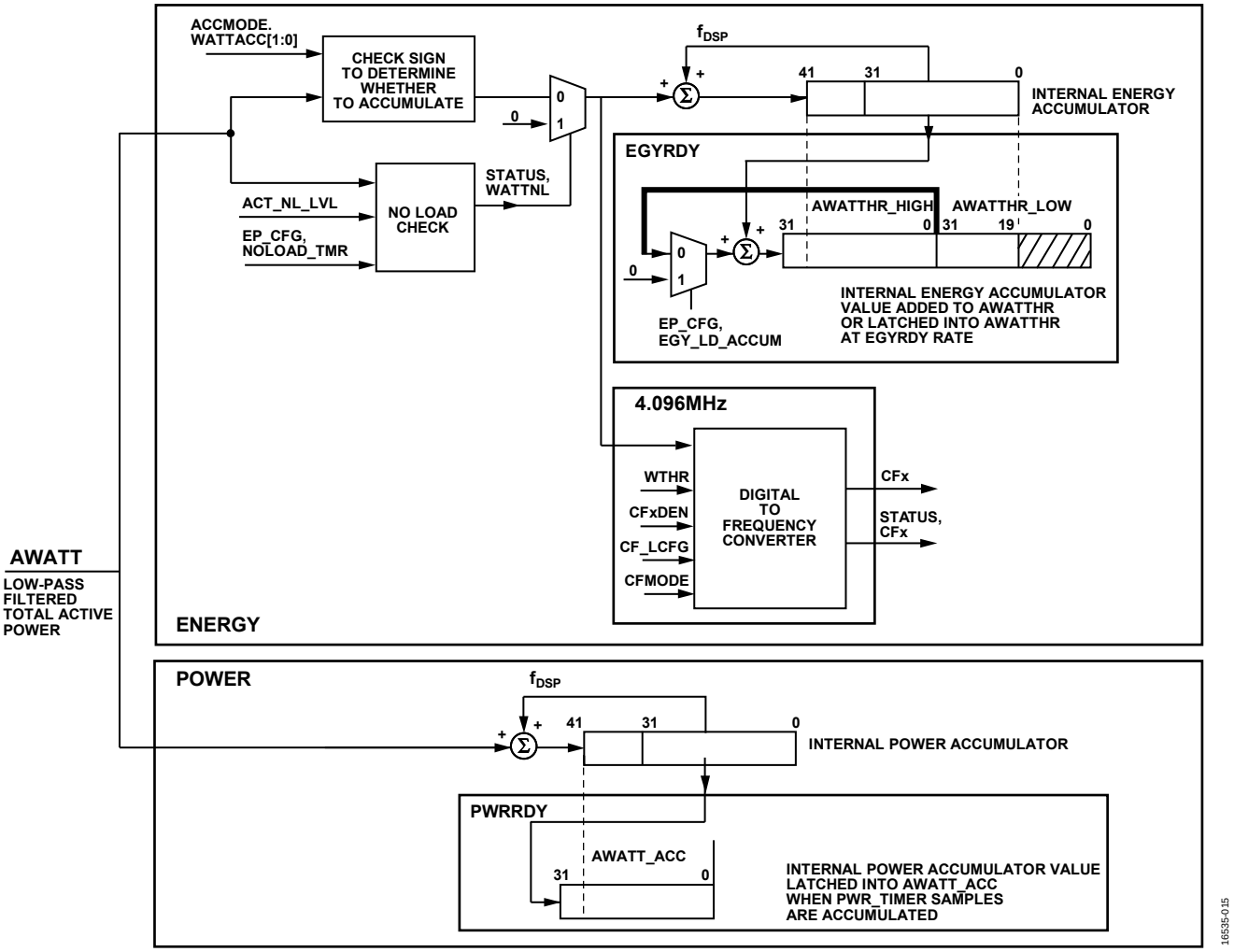

Figure 16. AWATT Accumulation into Energy and Power, Using No Load Threshold and with Signed Accumulation Mode

Figure 16 shows how AWATT is accumulated in the AWATTHR_HI, AWATTHR_LO, and AWATT_ACC registers. A no load threshold is applied and the energy is checked to determine whether to accumulate the AWATT sample into the internal energy accumulator. The internal energy accumulator is either added to the AWATTHR register or overwrites it at a EGYRDY rate. Set the EGY_PWR_EN bit in the EP_CFG register to run the energy and power accumulator.

Signed Energy Accumulation Modes

Total Active Energy Accumulation Modes

In some installations, it is desirable to bill for only positive total active energy. The ADE9153A offers a way to do this using the WATTACC[1:0] bits in the ACCMODE register. To set the total active energy accumulation and any corresponding CFx pulse output for positive energy only, write WATTACC, Bits[1:0], to 10.

If WATTACC, Bits[1:0], is equal to zero, the energy accumulation is signed. The MSB of the AWATTHR_HI register indicates whether the accumulated energy is negative or positive.

Other accumulation modes include absolute accumulation mode with WATTACC, Bits[1:0], equal to 01 (where the absolute value of AWATT is accumulated), and negative only accumulation mode with WATTACC, Bits[1:0], equal to 11 (where only negative active energy is accumulated).

Reactive Energy Accumulation Modes

In some applications, because reactive energy can change frequently between positive and negative values with inductive and capacitive loads, it is desirable to bill for the absolute value of reactive energy. The ADE9153A offers a way to do this using the VARACC[1:0] bits in the ACCMODE register. To set the fundamental reactive energy register and any corresponding CFx pulse output to accumulate the absolute value of reactive energy, write VARACC[1:0] to 01.

If VARACC[1:0] is equal to zero, the fundamental reactive energy accumulation is signed. The MSB of the AFVARHR_HI register indicates whether the energy is negative or positive.

Other accumulation modes offered include positive only accumulation mode with VARACC[1:0] equal to 10 and negative only accumulation mode (where only negative reactive energy is accumulated) with VARACC[1:0] equal to 11.

No Load Detection

No load detection prevents energy accumulation due to noise when the input currents are below a given meter start current.

To determine if a no load condition is present, the ADE9153A evaluates if the accumulated energy is below a user defined threshold over a user defined time period. This no load detection is performed on a per datapath and per energy basis.

The NOLOAD_TMR bits, Bits[7:5] in the EP_CFG register, determine whether to evaluate the no load condition over 64 samples to 4096 samples, 64/4 kSPS= 16 ms to 1024 ms, by writing to the bits in the EP_CFG register (see Table 11). No load detection is enabled by default, over the minimum time of 64/4 kSPS = 16 ms. No load detection is disabled when the NOLOAD_TMR bits, Bits[7:5] in the EP_CFG register, are equal to 111 (binary).

Table 11. No Load Condition Evaluation Time

NOLOAD_TMR, Bits[7:5]	Samples Over Which to Evaluate a No Load Condition	Time Over Which No Load Detection is Evaluated
0	64	16 ms
1	128	32 ms
2	256	64 ms
3	512	128 ms
4	1024	256 ms
5	2048	512 ms
6	4096	1024 ms
7	No load disabled	No load disabled

The user defined no load thresholds are written to the ACT_NL_LVL, REACT_NL_LVL, and APP_NL_LVL registers. The ACT_NL_LVL register sets the no load threshold for the total active energy. Correspondingly, the REACT_NL_LVL register sets the no load threshold for the fundamental reactive energy, and the APP_NL_LVL register sets the no load threshold for the total apparent energy.

The no load thresholds are calculated according to the following equation:

$$x\_NL\_LVL = \left(\frac{AWATT\_FULL\_SCALE \times 64}{x} \right)$$

where:
AWATT_FULL_SCALE is the nominal AWATT value with full-scale inputs, 10,356,306. Note that FVAR and VA have the same scaling; therefore, the same value can be used for all three thresholds.
x is the desired no load input power level. For example, to set the no load threshold to zero out energy below 50,000 from full scale, x = 50,000 in the previous equation.

Then, for a 50,000:1 no load threshold level, x_NL_LVL is 0x6790.

$$x\_NL\_LVL = \left(\frac{20{,}712{,}612 \times 64}{50000} \right) = 26{,}512 = 0x6790$$

When a phase is in no load, every f_{DSP} = 4 kSPS, and zero energy is accumulated into the energy registers and CFx accumulation.

Note that the x_ACC registers are not affected by no load detection. Even when in no load, any power calculated in the respective AWATT, AFVAR, and AVA registers is accumulated into the corresponding x_ACC register every f_{DSP} = 4 kSPS.

No Load Indications

The PHNOLOAD register indicates whether each phase of energy is in no load. For example, the AWATTNL (Bit 0), AVANL (Bit 1), and AFVARNL (Bit 2) bits in the PHNOLOAD register indicate whether the total active energy, total apparent energy, or fundamental reactive energy are in no load. If a bit is set, it indicates that the energy is in no load; if it is clear, the phase is not in no load.

The user can enable an interrupt to occur when one of the energy no load status changes, either going into or out of no load. There is an interrupt enable bit for each type of energy. Set the FVARNL bit, VANL bit, and WATTNL bit in the status register to enable an interrupt on $\overline{\text{IRQ}}$ when fundamental VAR, total VA, and total watt no load changes status.

Figure 17 shows what occurs when the AWATT, low-pass filtered watt value goes above the user configured no load threshold and then back down below it again. The same concept applies to all of the energy values (fundamental VAR and total VA) with the corresponding REACT_NL_LVL and APP_NL_LVL no load thresholds.

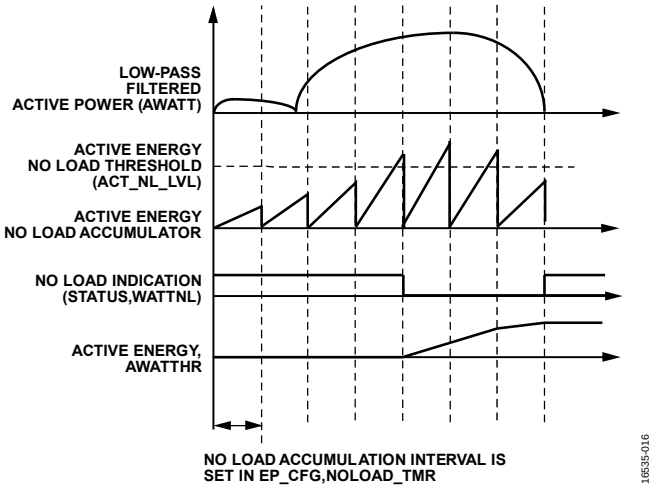

Figure 17. No Load Detection and Indication

Energy Accumulation Details

Internal Energy Register Overflow Rate

There are 42-bit, internal signed energy accumulators for each energy accumulation, as shown in Figure 16. These accumulators update at a rate of f_{DSP} = 4 kSPS. The following equation shows how to calculate the time until the internal accumulator overflows with full-scale inputs and all digital gain and offset factors at zero, where AWATT_AT_FULL_SCALE refers to the nominal AWATT value with full-scale inputs.

Maximum Internal Energy Accumulator Time (sec) =

$$\left(\frac{2^{41}}{AWATT\_AT\_FULL\_SCALE \times f_{DSP}}\right)$$

For example, with AIGAIN, AVGAIN, APGAIN, and AWATTOS all equal to zero, the Phase A total active energy has a digital gain of 1. Then, the Phase A total active energy accumulated in the internal accumulator overflows in 26.5 sec with the nominal full-scale AWATT value of 10,356,306.

Maximum Internal Energy Accumulator Time (sec) =

$$\left(\frac{2^{41}}{20{,}712{,}612 \times 4000}\right) = 26.5 \text{ sec}$$

User Energy Register Update Rate, EGYRDY

As shown in Figure 16, the internal energy accumulator is latched onto a user accessible energy register, or is added to the user accessible register at a rate of EGYRDY. Figure 18 further describes how the EGYRDY update rate is generated.

The EGYRDY update rate occurs after EGY_TIME + 1 f_{DSP} samples or EGY_TIME + 1 half line cycles, according to the EGY_TMR_MODE bit in the EP_CFG register.

If EGY_TMR_MODE is zero, the internal energy register accumulates for EGY_TIME + 1 samples at 4 kSPS. This mode is called sample-based accumulation.

Internal Energy Accumulation Time (sec) =

$$\left(\frac{EGY\_TIME + 1}{f_{DSP}}\right)$$

The EGY_TIME[12:0] register allows up to (8191 + 1) = 8192 samples to be accumulated, which corresponds to 8192/4000 = 2.048 sec if EGY_TMR_MODE is equal to zero.

Internal Energy Accumulation Time (sec) =

$$\left(\frac{8191+1}{4000}\right) = 2.048 \text{ sec}$$

If EGY_TMR_MODE is 1, the internal energy register accumulates for EGY_TIME + 1 half line cycles at 4 kSPS. This mode is called half line cycle-based accumulation. In this mode, the zero-crossing source to monitor is set by the ZX_SEL bits in the ZX_LP_SEL register, as shown in Figure 18.

Internal Energy Accumulation Time (sec) =

$$\left(\frac{EGY\_TIME + 1}{Zero - Crossing\ Rate}\right)$$

With a 50 Hz line frequency, the zero-crossing interrupt rate is 100 Hz; therefore, the maximum accumulation time is 81.92 sec with EGY_TIME equal to 0x1FFF, 8191 (decimal):

Internal Energy Accumulation Time (sec) =

$$\left(\frac{8191 + 1}{100}\right) = 81.92 \text{ sec}$$

Note that the internal energy register overflows in 13.3 sec with full-scale inputs; therefore, EGY_TIME must be set lower than 1329 (decimal) to prevent overflow when EGY_TMR_MODE is 1.

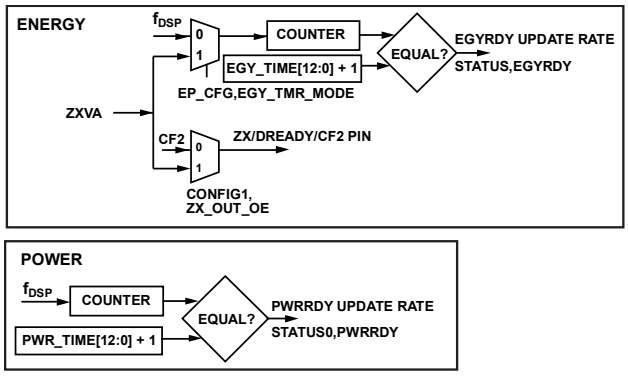

Figure 18. EGYRDY and PWRRDY Update Rate

Reloading or Accumulating the User Energy Register

When the EGYRDY event occurs, the internal energy accumulation is either directly loaded into the AWATTHR_x register or is added to the existing accumulation based on the state of the EGY_LD_ACCUM bit in the EP_CFG register. The internal energy register is reset and starts counting again from zero.

If EGY_LD_ACCUM = 0, the internal energy register is added to the user accessible energy register. If EGY_LD_ACCUM = 1, the internal energy register overwrites the user accessible energy register.

User Energy Register Overflow Rate

The energy registers in the ADE9153A are signed and 45 bits wide, split between two 32-bit registers, as shown in Figure 19. These accumulators update at a rate according to EGYRDY, as described in the User Energy Register Use Models section. The following equation shows how to calculate the time until the user accessible accumulator overflows with full-scale inputs and all digital gain and offset factors at zero, where AWATT_AT_FULL_SCALE refers to the nominal AWATT value with full-scale inputs. For this example, assume that the internal energy register is updating at every f_{DSP} = 4 kSPS sample.

$$\textit{Maximum Internal Energy Accumulator Time}\ (\text{sec}) = \left(\frac{2^{44}}{AWATT\_AT\_FULL\_SCALE \times f_{DSP}}\right)$$

For example, with AIGAIN, AVGAIN, APGAIN, and AWATTOS all equal to zero, the Phase A total active energy has a digital gain of 1. Then, the total active energy accumulated in the user accessible accumulator overflows in 212 sec with the nominal full-scale AWATT value of 10,356,306.

$$\textit{Maximum Internal Energy Accumulator Time}\ (\text{sec}) = \left(\frac{2^{44}}{20{,}712{,}612 \times 4000}\right) = 212\ \text{sec}$$

Accessing the User Energy Registers

Each 45-bit user accessible signed energy accumulator is divided into two registers: a register containing the 32 most significant bits, AWATTHR_HI, and a register containing the 13 least significant bits, AWATTHR_LO, as shown in Figure 19.

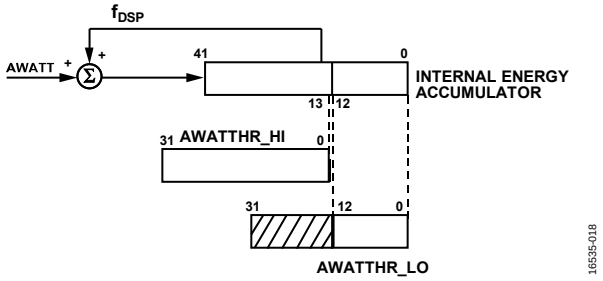

Figure 19. Internal Energy Register to AWATTHR_HI and AWATTHR_LO

The expected user energy accumulation can be calculated according to the following equation, based on the average AWATT value:

$$\textit{User Energy Accumulation} = AWATT \times (EGY\_TIME + 1)$$

Then, AWATTHR_HI contains the 32 most significant bits, which can be calculated by rounding the following equation down to the nearest whole number:

$$AWATTHR\_HI = \text{round down}(\textit{User Energy Accumulation} \times 2^{-13})$$

The 13 LSBs of the user energy accumulation are stored in the AWATTHR_LO register.

Read User Energy Register with Reset

If the RD_RST_EN bit is set in the EP_CFG register, its contents are reset when a user accessible energy register is read.

For example, if AWATTHR_HI is read, the AWATTHR_HI register value goes to zero. The AWATTHR_LO register contents are not modified.

User Energy Register Use Models

There are three main use models for energy accumulation:

- Read energy register with reset.
- Accumulate energy over a defined number of line cycles.
- Accumulate energy over a defined number of samples.

To read the energy register with reset, use the following settings:

- Configuration register settings:
  - EP_CFG register, EGY_LD_ACCUM bit = 0.
  - EP_CFG register, EGY_TMR_MODE bit = 0.
  - EP_CFG register, RD_RST_EN bit = 1.
  - EP_CFG register, EGY_PWR_EN bit = 1.
  - EGY_TIME register = 1.
- For the output, use only the AWATTHR_HI register, which has enough resolution for most applications. The AWATTHR_LO register is maintained and accumulated and does not need to be read by the user.
- The maximum time before reading AWATTHR_HI to prevent overflow with full-scale inputs is 212 sec.

To accumulate energy over a defined number of half line cycles, use the following configuration register settings:

- EP_CFG register, EGY_LD_ACCUM bit = 1.
- EP_CFG register, EGY_TMR_MODE bit = 1.
- EP_CFG register, RD_RST_EN bit = 0.
- EP_CFG register, EGY_PWR_EN bit = 1.
- EGY_TIME register = desired number of half line cycles.

To accumulate energy over a defined number of half line cycles, use the following output settings:

- The AWATTHR_HI register has enough resolution for most applications.
- To maintain perfect synchronization with the CFx pulse output, the AWATTHR_LO register must be read as well, because it is cleared at every EGYRDY cycle.

The maximum time before reading AWATTHR_HI to prevent overflow with full-scale inputs is 26.5 sec.

To accumulate energy over a defined number of samples, use the following configuration register settings:

- EP_CFG register, EGY_LD_ACCUM bit = 1.
- EP_CFG register, EGY_TMR_MODE bit = 0.
- EP_CFG register, RD_RST_EN bit = 0.
- EP_CFG register, EGY_PWR_EN bit = 1.
- EGY_TIME register = desired number of samples.

To accumulate energy over a defined number of samples, use the following output settings:

- The AWATTHR_HI register has enough resolution for most applications.
- To maintain perfect synchronization with the CFx pulse output, the AWATTHR_LO register must be read as well, because it is cleared at every EGYRDY cycle.

The maximum time before reading AWATTHR_HI to prevent overflow with full-scale inputs is 26.5 sec.

Digital to Frequency Conversion—CFx Output

Many electricity meters are required to provide a pulse output proportional to the energy being accumulated, with a given pulse per kW meter constant.

The ADE9153A includes two pulse outputs that are proportional to the energy accumulation, in the CF1 and CF2 output pins.

Energy and Phase Selection

The CFxSEL[2:0] bits in the CFMODE register select the type of energy to output on the CFx pins, including total watt, fundamental VAR, and total VA. Then, the TERMSELx bits in the COMPMODE register select which energies to include in the CF output.

For example, with the CFMODE register, CF1SEL[2:0] bits = 000 and the COMPMODE register, TERMSEL1[2:0] bits = 111, CF1 indicates the total watt output.

Configuring the Maximum CFx Pulse Output Frequency

It is recommended to leave xTHR at the default value of 0x0010_0000. CFxDEN can range from 2 to 65535. Configure CFxDEN to tune the CFx frequency output. The relationship between the xTHR, CFxDEN, and AWATT values is given in the following equation:

$$CFx\,(\text{Hz}) = \left(\frac{f_{DTOF} \times AWATT}{xTHR \times 512 \times CFxDEN} \right)$$

Then, the maximum recommended CFx pulse output frequency is 79.012 kHz.

$$Maximum\ CFx\ Pulse\ (\text{Hz}) = \left(\frac{4.096 \times 10^6 \times 20{,}712{,}612}{0x0010\_0000 \times 512 \times 2} \right) =$$

79.012 kHz

where:
f_{DTOF} is 4.096 MHz.
AWATT is the value at full scale, 10,356,306.
xTHR is 0x0010_0000.
CFDEN is 2.

Configuring the CFx Pulse Width

The pulse width is determined by the CFx_LT bit in the CF_LCFG register and the CF_LTMR register value.

With CFx_LT = 0, the active low pulse width is set at 80 ms for frequencies lower than 1/(2 × 80 ms) = 6.25 Hz. For higher frequencies, the duty cycle is 50% if CFxDEN is even or (1 + 1/CFxDEN) × 50% if CFxDEN is odd.

If CFx_LT is set to 1, the CF active low pulse width is CF_LTMR × 6/CLKIN. The maximum CF_LTMR is 327680 = 0x0005_0000, which results in a 327,680/(6/CLKIN) = 80 ms pulse. CF_LTMR must be greater than zero.

Table 12. CF Active Low Pulse Width and Duty Cycle Based on CFx_LT and CF_LTMR

CFx_LT	Active Low Pulse Width for Low Frequencies (ms)	Active Low Pulse Width for High Frequencies When CFxDEN Is Even	Active Low Pulse Width for High Frequencies When CFxDEN Is Odd	Behavior When Entering No Load
0	80	50%	(1 + 1/CFxDEN) × 50%	If CFx is low, finish current pulse, then return high
1	CF_LTMR × 6/CLKIN × 1000	50%	(1 + 1/CFxDEN) × 50%	If CFx is low, keep CFx low until no load state is finished

CFx Pulse Sign

Some applications must record positive and negative energy usage separately. To facilitate this requirement, the CFxSIGN bits in the PHSIGN register indicate whether the sum of the energy in the last CFx pulse is positive or negative. CFxSIGN = 0 if the sum of the energy in the CFx pulse is positive, and CFxSIGN = 1 if the sum of the energy is negative.

Furthermore, the REVPCFx bits in the status register and the EVENT_STATUS register indicate if the CFx polarity changed sign. For example, if the last CF2 pulse represents positive reactive energy, and the next CF2 pulse represents negative reactive energy, the REVPCF2 bit in the status and EVENT_STATUS registers is set. This event can be enabled to generate an interrupt on $\overline{\text{IRQ}}$.

Clearing the CFx Accumulator

It may be desirable to clear out a partial CFx accumulation, for example, during the power-up and initialization process. To clear the accumulation in the digital to frequency converter and CFDEN counter, write the CF_ACC_CLR bit in the CONFIG1 register to 1. The CF_ACC_CLR bit automatically clears itself.

Disabling the CFx Pulse Output and CFx Interrupt

To disable the CFx pulse output and keep the CFx output high, write a 1 to the CFx_DIS bit in the CFMODE register. If the CFx output is disabled, the CFx bit in the status register is not set when a new CFx pulse is ready. Note that the REVPCFx bits, which indicate if CF pulses were positive or negative, are not affected by the CFx_DIS setting.

POWER ACCUMULATION

Figure 16 shows how AWATT, low-pass filtered, active power samples are accumulated to provide an accurate active power value in the AWATT_ACC register. The sign of the total active power accumulation is monitored in the REVAPA status bit, and interrupts can be enabled if the power changes sign. There are corresponding x_ACC accumulations for each power on each phase and REVx status bits in the status register to indicate if the power changes sign.

Power Accumulation Details

Figure 16 shows how AWATT values are accumulated into an internal power accumulator and then are latched into the xWATT_ACC register at a rate of PWRRDY.

PWRRDY is set after PWR_TIME + 1 samples at 4 kSPS accumulate. Calculate the power accumulation time according to the following equation:

$$\textit{Internal Power Accumulator Time}\ (\text{sec}) = \left(\frac{PWR\_TIME + 1}{4000}\right)$$

The PWR_TIME[12:0] register allows up to (8191 + 1) = 8192 samples to be accumulated, which corresponds to 8192/4000 = 2.048 sec:

$$\textit{Internal Energy Accumulation Time}\ (\text{sec}) = \left(\frac{8191 + 1}{4000}\right) = 2.048\ \text{sec}$$

The internal power accumulator overflows at the same rate as the internal energy accumulator (see the Internal Energy Register Overflow Rate section).

Accessing the User Power Registers

Each 42-bit, user accessible, signed power accumulator is divided into a register containing the 32 most significant bits, x_ACC, as shown in Figure 20.

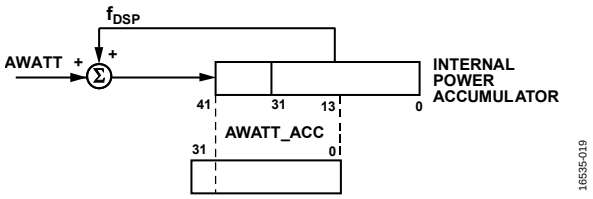

Figure 20. Internal Power Register to AWATT_ACC

The expected user power accumulation can be calculated according to this formula, based on the average AWATT value:

$$\textit{User Power Accumulation} = AWATT \times (PWR\_TIME + 1)$$

Then, expected data in the 32-bit power accumulation registers (xWATT_ACC, xVAR_ACC, and xVA_ACC) can be calculated as follows:

$$\textit{Power accumulation register} = \text{round down}(\textit{User Power Accumulation} \times 2^{-13})$$

For example, if 4000 samples of AWATT are accumulated at 4 kSPS with full-scale inputs, the expected value of AWATT_ACC is 0x009B_0003:

$$\textit{User Power Accumulation} = 20{,}712{,}612 \times (3999 + 1) = 41425224691$$

$$AWATT\_ACC = \text{round down}(41425224691 \times 2^{-13}) = 5056790 = 0x004D\_2916$$

To determine the consumption in watts, multiply xWATT_ACC by the W/code constant: xWATT_ACC × W/code.

Note that W/code varies with the PWR_TIME accumulation time.

Power Sign Detection

The REVRPA bit and REVAPA bit in the status register allow the user to monitor if the active or reactive power on any phase changed sign.

The AWSIGN and AVARSIGN bits in the PHSIGN register indicate whether the total WATT and fundamental VAR are positive or negative.

The power signs are updated at the same time as the xWATT_ACC register and xFVAR_ACC register and correspond to the sign of these registers. Note that the power registers and signs are updated after the number of f_{DSP} = 4 kSPS samples configured in the PWR_TIME register elapses, from 500 µs to 2 sec. The power sign change indication in the REVxPx bits are updated at the same time; see the Power Accumulation Details section for more information.

The ADE9153A allows the user to accumulate total watt and fundamental VAR powers into separate positive and negative registers: PWATT_ACC and NWATT_ACC, PVAR_ACC and NVAR_ACC. This accumulation is performed by evaluating the AWATT, low-pass filtered, active power every 4 kSPS. If the AWATT value is positive, it is added to the PWATT_ACC accumulation. If the AWATT value is negative, the absolute value is added to the NWATT_ACC accumulation. A new accumulation from zero begins when the power update interval set in PWR_TIMER elapses. The positive and negative total watt and total VAR from all three phases are added into the positive/negative watt and VAR accumulations.

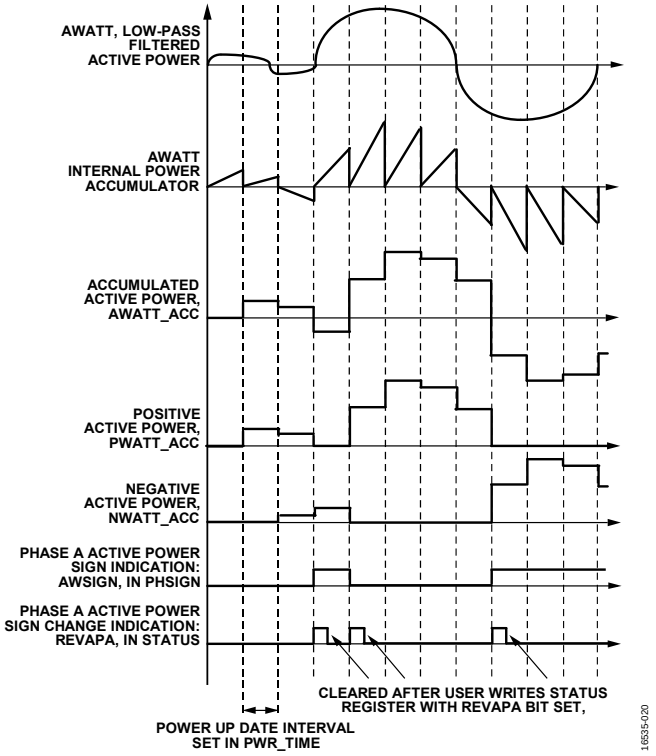

Figure 21. Power Accumulation and Power Sign

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE9153A offers zero-crossing detection on the VA, IA, and IB input signals. The zero-crossing circuit is used as the time base for line period, angle measurements, and energy accumulation using line cycle accumulation mode. AV_WAV and xI_WAV are the voltage and current channel waveforms processed by the DSP.

The ZX_SRC_SEL bit in the CONFIG0 register sets whether data going into the zero-crossing detection circuit arrives before or after the high-pass filter and phase compensation. By default, the data after phase compensation is used. Note that the high-pass filter has a settling time (see Table 3) with a step change in the input; therefore, for a fast response, it is recommended to set ZX_SRC_SEL to search for a zero crossing before the high-pass filter. If a high-pass filter is disabled with the HPFDIS bit in the CONFIG0 register equal to 1, or if the ZX_SRC_SEL bit in the CONFIG0 register is equal to 1, a dc offset on the input may cause the time between the negative to positive and positive to negative zero crossings (and positive to negative and negative to positive zero-crossings) to change, indicating that the zero-crossing detection does not have a 50% duty cycle.

The current and voltage signals are low-pass filtered to remove harmonics. The low-pass filter, LPF1, has a corner frequency of 85 Hz and the equation is as follows:

$$H(z) = \frac{2^{-3}}{1-(1-3)z^{-1}}$$

The low-pass filter settling time is 51 samples, 51/4 kSPS, which equals 12.75 ms.

Figure 22 shows the delay between the detected zero-crossing signal and the input. Note that there is a 4.3 ms delay between the input signal zero-crossing and the zero-crossing indication, with a 50 Hz input signal. Zero crossings are generated on both negative to positive and positive to negative transitions.

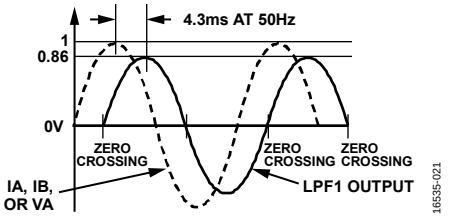

Figure 22. Zero-Crossing Detection on the Voltage and Current Channels

To provide protection from noise, the voltage channel zero-crossing events (ZXVA) are not generated if the absolute value of the LPF1 output voltage is smaller than the threshold, ZXTHRSH. The current channel zero-crossing detection outputs (ZXIA and ZXIB) are active for all input signals levels.

The zero-crossing threshold, ZXTHRSH, can be calculated from the following equation:

$$ZXTHRSH = \frac{(AV\_WAV\ at\ Full\ Scale) \times (LPF1\_ATTENUATION)}{x \times 32 \times 2^8}$$

where:
AV_WAV at Full Scale is ±74,565,404 (decimal).
x is the dynamic range that the zero-crossing under which the zero crossing must be blocked.
LPF1_ATTENUATION is 0.86 at 50 Hz and 0.81 at 60 Hz, the gain attenuation of the LPF1 filter.

For example, to prevent signals 100 times lower than full scale from generating a zero-crossing output, set ZXTHRSH to 78 (decimal):

$$ZXTHRSH = \frac{(74{,}565{,}404) \times (0.86)}{100 \times 32 \times 2^8} = 78\text{d}$$

Additionally, to prevent false zero crossings, after a zero crossing is generated, 1 ms must elapse before the next zero crossing can be output.

Zero-Crossing Output Rates

There are three zero-crossing detection circuits that monitor IA, IB, and VA. The zero-crossing detection circuits have two different output rates: 4 kSPS and 512 kSPS. The 4 kSPS zero-crossing signal is used to calculate the line period, sent to the ZXx bits in the status register, and is monitored by the zero-crossing timeout, phase sequence error detection, resampling, and energy accumulation functions. The 512 kSPS signal is used for angle measurements and is output on the ZX/DREADY/CF2 pin if the ZX_OUT_OE bit in the CONFIG1 register is equal to 1.

Table 13 indicates which zero-crossing edges (negative to positive and positive to negative) are used for each function and indicates what happens if a zero crossing is blocked because the input signal is below the user configured ZXTHRSH threshold.

The ZX/DREADY/CF2 output pin goes from low to high when a negative to positive transition is detected and from high to low when a positive to negative transition occurs. The ZX_SEL[1:0] bits in the ZX_LP_SEL register select the zero-crossing output used for line cycle energy accumulation and the ZX output pin.

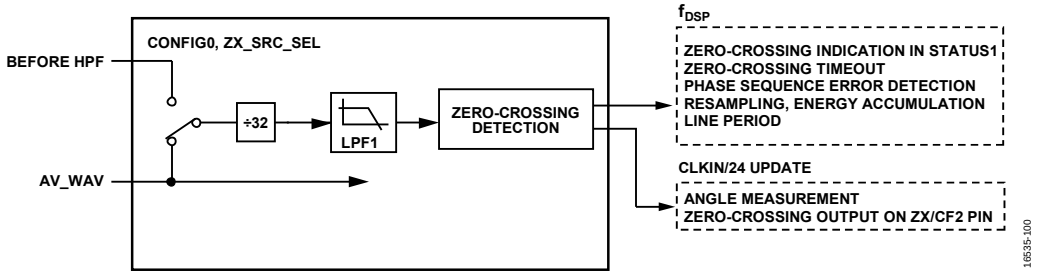

Figure 23. Zero-Crossing Output Rates

Table 13. Zero-Crossing Use in Other Functions

Functions Using Zero-Crossing	Zero-Crossing Transitions Used	Corresponding Status Register Bits	Effect if Zero Crossing Does Not Occur
Zero-Crossing Indication in the Status Register	Negative to positive and positive to negative	ZXIA, ZXIB, ZXVA	ZXx bit is latched in the status register. If cleared, it is not set again. ZXx interrupt does not occur.
Zero-Crossing Timeout	Negative to positive and positive to negative	ZXTOVA	Zero-crossing timeout is indicated by the ZXTOUT bit in the status register and an interrupt can be enabled to occur.
Energy Accumulation	Negative to positive and positive to negative	Not applicable	Line cycle accumulation does not update.
Line Period Measurement	Negative to positive	Not applicable	Coerced to default value: 0x00A0_0000 if the SELFREQ bit in the ACCMODE register = 0, for a 50 Hz network; 0x0085_5554 if the SELFREQ bit in the ACCMODE register = 1, for a 60 Hz network.
RMS½	None	Not applicable	If the selected line period is invalid because zero crossings are not detected, or if the calculation results in a value outside the 40 Hz to 70 Hz range, the line period used for the calculation is coerced to the default line period: 0x00A0_0000 if the SELFREQ bit in the ACCMODE register = 0, for a 50 Hz network; 0x0085_5554 if the SELFREQ bit in the ACCMODE register = 1, for a 60 Hz network.
Angle Measurements	Negative to positive	Not applicable	Does not update; keeps last value.
ZX Output on ZX/DREADY/CF2 Pin	Negative to positive and positive to negative	Not applicable	Remains at current state (high or low).

Zero-Crossing Timeout

The zero-crossing timeout feature alerts the user if a zero-crossing event is not generated after a user configured amount of time. If a zero-crossing on is not received after ZXTOUT 4 kSPS clocks, the corresponding ZXTOx bit in the status register is set. For example, if ZXTOUT is equal to 4000, if a zero crossing is not then received on Phase A for 4000/4 kSPS = 1 sec, the ZXTOA bit is set in the status register. The maximum value that can be written to the ZXTOUT register is 0xFFFF/4000 = 16.38 sec.

Line Period Calculation

The ADE9153A line period measurement is performed by taking the values low-pass filtered by LPF1, as described in the Zero-Crossing Detection section, and then using the two values (POS1 and POS 2 in Figure 24) near the positive to negative zero crossing to calculate the exact zero crossing point using linear interpolation. This information is used to precisely calculate the line period, which is stored in the APERIOD register.

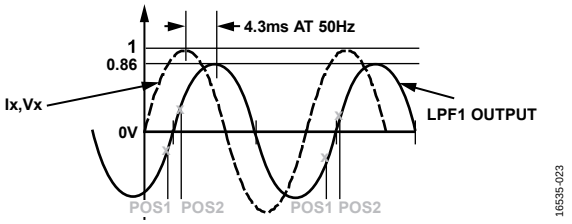

Figure 24. Line Period Calculation Using Zero-Crossing Detection and Linear Interpolation

Calculate the line period (T_L) the xPERIOD register according to the following equation:

$$T_L = \frac{APERIOD + 1}{4000 \times 2^{16}} (\text{sec})$$

Similarly, calculate the line frequency from the APERIOD register using the following equation:

$$f_L = \frac{4000 \times 2^{16}}{APERIOD + 1} (\text{Hz})$$

With a 50 Hz input, the APERIOD register is 0x0050_0000, 5242880 (decimal), and with 60 Hz, it is 0x0042_AAAA, 4369066 (decimal).

If the calculated period value is outside the range of 40 Hz to 70 Hz, or if the negative to positive zero crossings for that phase are not detected, the APERIOD register is coerced to correspond to 50 Hz or 60 Hz, according to the setting of the SELFREQ bit in the ACCMODE register. With SELFREQ equal to 0 for a 50 Hz network, the APERIOD register is coerced to 0x0050_0000. If SELFREQ is 1, indicating a 60 Hz network, the APERIOD register is coerced to 0x0042_AAAA.

The line period is calculated for the voltage channel and stored in the APERIOD register.

The user period selection can help in applications in which the user has another algorithm to determine the line frequency, or if it is preferred to always assume a certain line frequency when resampling or calculating a fast rms measurement. USER_PERIOD, Bits[31:0] has the same scaling as the APERIOD register. Write USER_PERIOD, Bits[31:0] to 0x0050_0000 for 50 Hz and 0x0042_AAAA for 60 Hz.

Angle Measurement

The ADE9153A measures the time between zero crossings on each phase.

The times between positive to negative zero crossings are measured using a CLKIN/12 = 12.288/24 = 512 kHz clock. The time between the zero crossing on the Phase A voltage and current is stored in the ANGL_Ax_xI registers. The resolution of the ANGL_Ax_xI register is (1/(512 × 1000))/20 ms × 360° = 0.03515625° at 50 Hz.

The angle in degrees can be calculated from the following equation with a 50 Hz line period:

$$Angle\ (\text{degrees}) = ANGL\_Ax\_xI \times 0.03515625/\text{LSB}$$

The current to current zero crossings are also measured. The time between the zero crossing on Phase A and Phase B is stored in the ANGL_AI_BI register.

The voltage to current phase angles are measured as well. These angles can be used to determine the power factor at the fundamental. ANGL_AV_AI reflects the phase angle between the Phase A voltage and current, as shown in Figure 25.

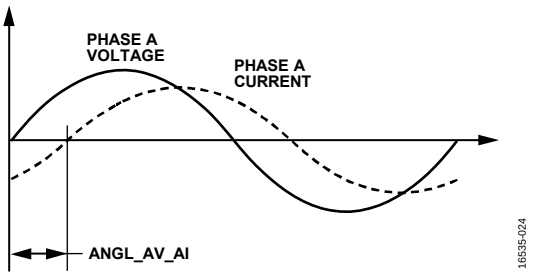

Figure 25. Voltage to Current Phase Angles

If the magnitude of the voltage channel is below the user configured zero-crossing threshold, the zero-crossing output for that phase is not generated. In this event, the corresponding ANGL_Ax_xI measurements are not updated; the last value remains in the register. The current channel does not have these thresholds. With a low input signal level, spurious zero-crossing events may be generated on the current channel, which results in ANGL_Ax_xI readings that are not meaningful.

Fast RMS½ Measurements

RMS½ is an rms measurement done over one line cycle, updated every half cycle.

This measurement is provided for voltage and current on all phases plus the neutral current. All the half cycle rms measurements are performed over the same time interval and update at the same time, as indicated by the RMS_OC_RDY bit in the status register. The results are stored in the AIRMS_OC, BIRMS_OC, and AVRMS_OC registers.

By default, the number of samples used in the calculation varies with measured line frequency. The voltage channel zero crossing is used to set the number of samples used in the rms½ measurement.

Alternatively, the user can set the number of samples used in the calculation by setting the UPERIOD_SEL bit in CONFIG2; where the user configured the USER_PERIOD register is used instead of the selected line period measurement. For more information about USER_PERIOD and the line period measurements, see the Line Period Calculation section.

The samples used for the rms½ calculation can come before the high-pass filter or after the high-pass filter, as selected in the RMS_OC_SEL bit in the CONFIG0 register.

Because the high-pass filter has a significant settling time associated with it, it is recommended to use the data from before the high-pass filter for the fastest response time.

An offset correction register is provided for even better performance with small input signal levels, xRMS_OC_OS.

The xIRMS_OC register reading with full-scale inputs is 52,725,703 (decimal). The AVRMS_OC register reading with full-scale inputs is 26,362,852 (decimal).

Dip/Swell Indication

Dip indicates if the voltage goes below a specified threshold for a user configured number of cycles. Conversely, swell indicates if the voltage goes above a threshold for a specified number of cycles.

Set the DIP_LVL register to correspond to the rms½ value to trigger the dip event, according to this equation:

$$DIP\_LVL = AVRMS\_OC \times 2^{-5}$$

Configure the number of cycles to observe the rms½ value over in the DIP_CYC register.

The rms½ voltage on Phase A is compared to the DIP_LVL over the specified DIP_CYC. If the rms½ voltage is low for the specified number of DIP_CYC, the dip event occurred on that phase and the corresponding DIPA bit is set in the EVENT_STATUS register. The dip event can be configured to generate an interrupt on the $\overline{\text{IRQ}}$ pin.

The dip event can be configured to generate an event on the $\overline{\text{IRQ}}$ pin, if the corresponding bits are set in the mask register.

The minimum rms½ value measured during the dip is stored in the DIPA register.

Similarly, the swell indication has a SWELL_LVL register to set the swell threshold, according to this equation:

$$SWELL\_LVL = AVRMS\_OC \times 2^{-5}$$

There is also a SWELL_CYC register. The maximum rms½ voltage value measured during the swell is stored in the SWELLA register. If the DIP_SWELL_IRQ_MODE bit is set to 0 in the CONFIG1 register, an interrupt is generated every DIP_CYC/SWELL_CYC cycles. If DIP_SWELL_IRQ_MODE is set to 1, one interrupt is generated when dip/swell mode is entered and another interrupt is generated on exit. The mode is changed after DIP_CYC cycles. Note that if DIP_CYC/SWELL_CYC = 1, an extra interrupt is generated on exit of the dip/swell condition, and the dip/swell value, DIPx/SWELLx, is updated at that time, which exceeds the DIP_LVL/SWELL_LVL value.

Overcurrent Indication

Overcurrent indication monitors the rms½ current measurements. If an RMS½ current is greater than the user configured OI_LVL, the overcurrent threshold, this is indicated in the OI bit in the EVENT_STATUS register.

$$OI\_LVL = xIRMS\_OC \times 2^{-5}$$

The OCx_EN bits in the CONFIG3 register select which phases to monitor for overcurrent events.

The OIx bits in the EVENT_STATUS register indicate which current channels had rms½ measurements greater than the threshold.

If a phase is enabled with the corresponding OIx_EN bit set in the CONFIG3 register and rms½ is current greater than the threshold, the OIx status bit is set, and the rms½ value is stored in the corresponding OIx register. If a phase is disabled, or an overcurrent event does not occur on that phase, the OIx register keeps the last value.

Peak Detection

The ADE9153A records the peak value measured on the current and voltage channels, from the xI_WAV and AV_WAV waveforms. The PEAKSEL bits, Bits[1:0] in the CONFIG3 register, allow the user to select which phases to monitor. Set PEAKSEL (Bit 1) for Current Channel B, and PEAKSEL (Bit 0) for Current Channel A and the voltage channel. Set PEAKSEL (Bits[1:0]) = 11 (binary) to monitor all channels.

The IPEAK register stores the peak current value in IPEAKVAL, Bits[23:0], and indicates which phase current(s) reached the value in the IPPHASE bits, Bits[2:0]. IPEAKVAL is equal to xI_WAV/2^5.

IPPHASE (Bit 1) indicates Phase B, and IPPHASE (Bit 0) indicates Phase A.

Similarly, VPEAK stores the peak voltage value in VPEAKVAL, Bits[23:0]. VPEAKVAL is equal to xV_WAV/2^5.

When the user reads the IPEAK register, its value is reset. The same is true for reading VPEAK.

Power Factor

The total active power and total apparent power are accumulated over 1.024 sec. Then, the power factor is calculated on each phase according to this equation:

$$APF = \frac{AWATT\ accumulated\ over\ 1.024\ \text{sec}}{AVA\ accumulated\ over\ 1.024\ \text{sec}}$$

The sign of the Channel A power factor (APF) calculation follows the sign of the AWATT register.

To determine which quadrant the energy is in, look at the sign of the total or fundamental reactive energy in that phase along with the sign of the APF or AWATT value, as indicated in the ADE9153A data sheet. Quadrant I and Quadrant III have capacitive power factors, and Quadrant II and Quadrant IV have inductive power factors. Note that, for most applications, the watts are received (imported) from the grid, and therefore, the watt and VAR stay within Quadrant I and Quadrant IV.

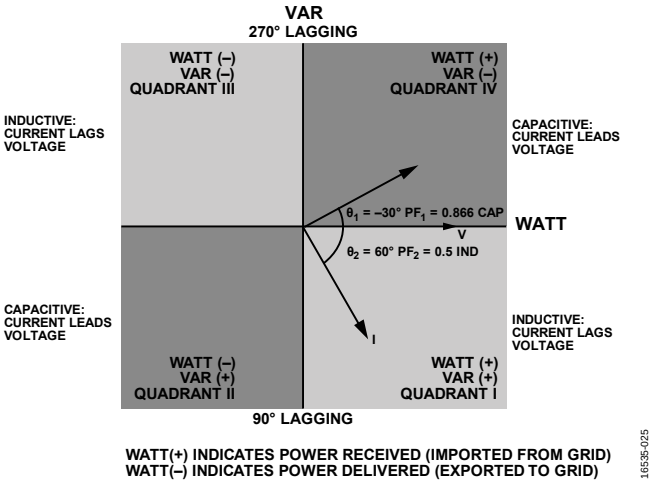

Figure 26. Watt and VAR Sign for Capacitive and Inductive Loads

The power factor results are stored in 5.27 format. The highest power factor value is 0x07FF_FFFF, which corresponds to a power factor of 1. A power factor of −1 is stored as 0xF800_0000. To determine the power factor from the xPF register value, use this equation:

$$Power\ Factor = APF \times 2^{-27}$$

TEMPERATURE

The ADE9153A includes a temperature measurement unit that uses a temperature sensor in conjunction with a 12-bit successive approximation register (SAR) ADC.

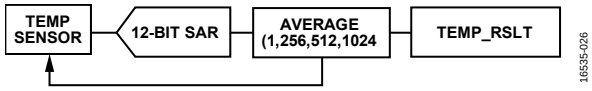

Figure 27. Temperature Measurement Block Diagram

Enable the temperature sensor by setting the TEMP_EN bit in the TEMP_CFG register. TEMP_TIME, Bits[1:0], allow 1, 256, 512, or 1024 temperature readings to be averaged, producing a result after 1.25 ms to 1.3 sec. A temperature acquisition cycle is started by setting the TEMP_START bit in the TEMP_CFG register. The result is available in the TEMP_RSLT register. The TEMP_START bit is self clearing. Set the TEMP_START bit to obtain a new reading. Set the TEMP_RDY bit in the MASK0 register to receive an interrupt when a new temperature measurement is available.

The temperature reading offset and gain is measured during production test and stored in the TEMP_TRIM register. To convert the temperature readings in TEMP_RSLT into a temperature in degrees Celsius, use this equation:

$$Temperature\ (°C) = TEMP\_RSLT \times (-TEMP\_GAIN/2^{17}) + (TEMP\_OFFSET/2^{5})$$

ACCESSING ON-CHIP DATA

SPI PROTOCOL OVERVIEW

The ADE9153A has a serial peripheral interface (SPI)-compatible interface, consisting of four pins: SCLK, MOSI, MISO, and $\overline{SS}$. The ADE9153A is always an SPI slave; it never initiates SPI communication. The SPI interface is compatible with 16-bit and 32-bit read/write operations.

Figure 28 shows the connection between the ADE9153A SPI and a master device that contains an SPI interface.

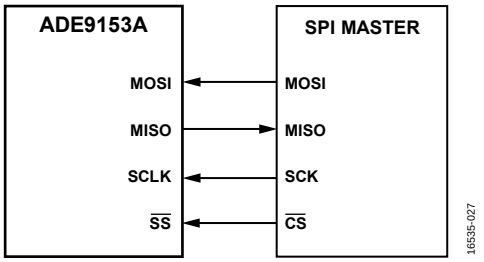

Figure 28. Connecting the ADE9153A Slave SPI Port to a Master SPI Device

The $\overline{SS}$ pin is the chip select input. It is used to start the SPI communication with the ADE9153A.

There are three parts to the ADE9153A SPI protocol. First, a 16-bit command is sent, which indicates whether a read or write operation is to be performed and which register to access. This command is followed by the 16-bit or 32-bit data to be written, in the case of an SPI write, or the data read from the register, in the case of an SPI read operation. Finally, in the case of an SPI read operation, a cyclic redundancy check (CRC) of the register data follows, unless the address is in a region that supports burst reading, in which case, the data from the next register follows (see the SPI Burst Read section for more information).

The $\overline{SS}$ input must stay low for the entire SPI transaction. Bringing $\overline{SS}$ high during a data transfer operation aborts the transfer. A new transfer can be initiated by returning the $\overline{SS}$ logic input low. It is not recommended to tie $\overline{SS}$ to ground because the high to low transition on $\overline{SS}$ starts the ADE9153A SPI transaction.

Data shifts into the device at the MOSI logic input on the falling edge of SCLK, and the device samples the input data on the rising edge of SCLK. Data shifts out of the ADE9153A at the MISO logic output on the falling edge of SCLK and must be sampled by the master device on the rising edge of SCLK. The most significant bit of the word is shifted in and out first.

MISO has an internal weak pull-up resistor of 100 kΩ, making the default state of the MISO pin high. It is possible to share the SPI bus with multiple devices, including multiple ADE9153A devices, if desired.

The ADE9153A is compatible with the following microcontroller SPI port clock polarity and phase settings: CPOL = 0 and CPHA = 0 (typically Mode 0), or CPOL = 1 and CPHA = 1 (typically Mode 3).

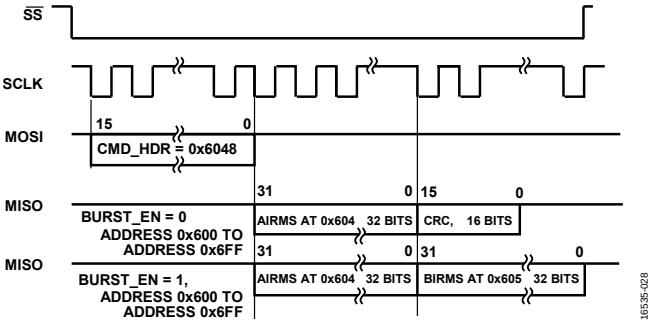

Figure 29. SPI Read Protocol Example—CRC or Next Data Can Follow

The default state of the MOSI pin depends on the master SPI device. Here, it is assumed to be high (Logic 1).

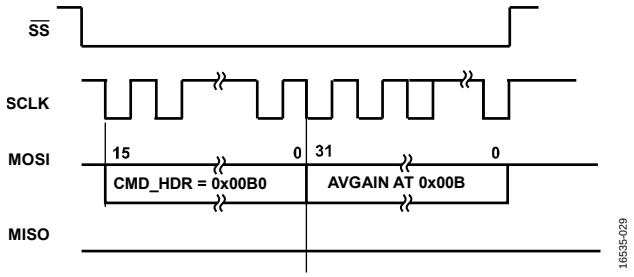

Figure 30. SPI Write Protocol Example

The maximum serial clock frequency supported by this interface is 10 MHz.

The SPI read/write operation starts with a 16-bit command (CMD_HDR), which contains the following information:

- CMD_HDR[15:4], the 12 most significant bits of the command header, contains the address of the register (ADDR[11:0]) to be read or written.
- CMD_HDR[3] is the bit that specifies if the current operation is read/write. Set this bit to 1 for read and 0 for write.
- CMD_HDR[2:0] are bits that are required for internal chip timing and can be 1s or 0s. Note that these bits are read back as 000 in the LAST_CMD register.

Figure 31 shows the information contained in the command header.

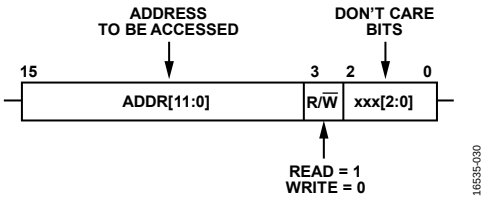

Figure 31. Command Header, CMD_HDR [15:0]

SPI WRITE

A write operation using the SPI interface of the ADE9153A is initiated when the $\overline{SS}$ pin goes low and the ADE9153A receives a 16-bit command header (CMD_HDR) with CMD_HDR[3] equal to 0.

The 16-bit or 32-bit data to be written follows the command header, with the most significant bit first.

After the last bit of data has been clocked out, the master must bring the $\overline{SS}$ line high to release the SPI bus. It is recommended to have the SCLK line idle high.

SPI READ

A read operation using the SPI interface of the ADE9153A is initiated when the $\overline{SS}$ pin goes low and the ADE9153A receives a 16-bit command header (CMD_HDR) with CMD_HDR[3] equal to 1.

The 16-bit or 32-bit data from the register follows the command header, with the most significant bit first.

The CRC of the register data is appended if

- BURST_EN = 0 and the address is within the range of 0x000 to 0x6FF.

The ADE9153A provides an SPI burst read functionality: instead of sending the CRC, the following data is from the next address if the following conditions apply (see the SPI Burst Read section for more information):

- BURST_EN = 1, and the address is within the range of 0x600 to 0x61A.

If none of these cases apply and extra clocks are sent, the original read data is resent.

Table 14 summarizes the data that is sent after the data from the register addressed in the CMD_HDR; it varies based on the address being accessed and the BURST_EN selection.

Table 14. Data Clocked Out After Addressed Data in SPI Read Operation

Address	BURST_EN = 0	BURST_EN = 1
0x000 to 0x4FF	CRC	Same data is resent
0x600 to 0x6FF	CRC	Next address

The $\overline{SS}$ line can be brought high before clocking out the CRC if this information is not needed in the application.

After the last bit of data, or CRC, has been clocked out, the master must bring the $\overline{SS}$ line high to release the SPI bus. Then the ADE9153A stops driving MISO and enables a 100 kΩ weak pull-up. It is recommended to have the SCLK line idle high.

An example of what happens when reading the AVGAIN register, Address 0x002, when BURST_EN = 0 and 1, is shown in Figure 32.

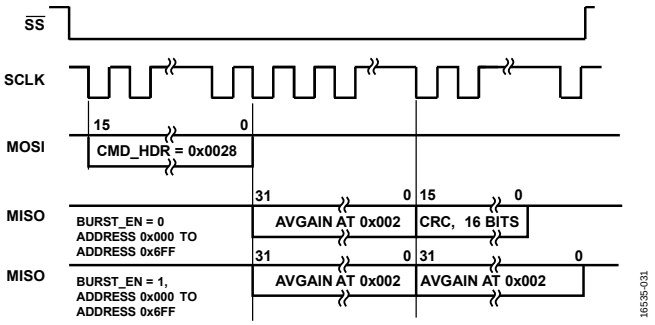

Figure 32. SPI Read Protocol Example Where the Following Data Is the CRC or the Initial Data Is Repeated

SPI BURST READ

SPI burst read allows multiple registers to be read after sending one CMD_HDR. After the register data is clocked out, the ADE9153A auto-increments the address and starts clocking out the data from the next register address.

SPI burst read access is available on registers with addresses ranging from 0x600 to 0x6FF. SPI burst read is not available on other register addresses. An SPI burst read operation occurs for the options in Table 14 where next address is shown.

To enable burst read functionality on the registers from 0x600 to 0x6FF, set the BURST_EN bit in the CONFIG1 register to 1.

A burst read operation using the SPI interface of the ADE9153A is initiated when the $\overline{SS}$ pin goes low and the ADE9153A receives a 16-bit command header (CMD_HDR) with CMD_HDR[3] equal to 1, which meets the criteria in Table 14 where the next address is shown.

Following the command header, ADE9153A sends the register data for the register addressed in the command. After the last bit of the first register value is received, the ADE9153A auto-increments the address and starts clocking out the data from the next register address. If the initial address is in the Address 0x600 to Address 0x61A and the SPI is clocked beyond Address 0x61A, the address wraps back to the initial address. This process continues until the master sets the $\overline{SS}$ line high. Then, the ADE9153A stops driving MISO and enables a 100 kΩ weak pull-up. It is recommended to have the SCLK line idle high. An example of an SPI burst read operation is shown in Figure 29, when BURST_EN = 1.

SPI PROTOCOL CRC

The ADE9153A SPI port calculates a CRC of the data sent out on its MOSI pin so that the integrity of the data received by the master can be checked. The CRC of the data sent out on the MOSI pin during the last register read is offered in a 16-bit register, CRC_SPI, and can be appended to the SPI read data as part of the SPI transaction.

The CRC_SPI register value is appended to the 16-bit/32-bit data read from the register addressed in the CMD_HDR for the cases in Table 14 where CRC is written (see the SPI Read section for more information).

The CRC result can always be read from the CRC_SPI register directly.

There is no CRC checking as part of the SPI write register protocol. To ensure the data integrity of the SPI write operation, read the register back to verify that the value is written to the ADE9153A correctly.

ADE9153A CRC Algorithm

The CRC algorithm implemented within the ADE9153A is based on the CRC-16-CCITT algorithm. The data output on MISO is introduced into a linear feedback shift register (LFSR)-based generator one byte at a time, most significant byte first, without bit reversal, as shown in Figure 33 and Figure 34. The 16-bit result is written in the CRC_SPI register.

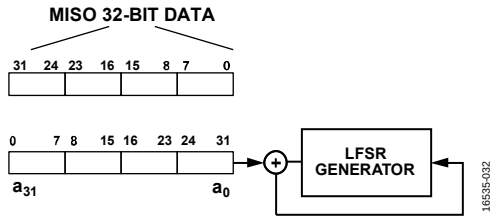

Figure 33. CRC Calculation of 32-Bit SPI Data

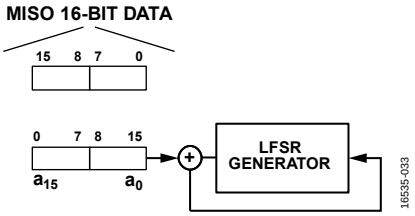

Figure 34. CRC Calculation of 16-Bit SPI Data

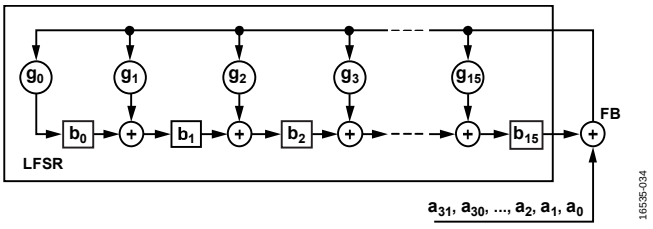

Figure 35. LFSR Generator Used for CRC_SPI Calculation

Figure 35 shows how the LFSR works. The MISO 32-bit data forms the [a_{31}, a_{30}, …, a_0] bits used by the LFSR. Bit a_0 is Bit 24 of the first MISO 32-bit data to enter the LFSR, and the last data to enter the LFSR, Bit a_{31}, corresponds to Bit 7 transmitted on MISO. The formulas that govern the LFSR are as follows.

$b_i(0) = 1$, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant bit.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm as follows:

$$G(x) = x^{16} + x^{12} + x^5 + 1 \quad (3)$$

$$g_0 = g_5 = g_{12} = 1 \quad (4)$$

All other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (5)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (6)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots, 15 \quad (7)$$

Equation 5, Equation 6, and Equation 7 must be repeated for j = 1, 2, …, 32. The value written into the CRC_SPI register contains Bit $b_i(32)$, i = 0, 1, …, 15.

A similar process is followed for 16-bit data; see Figure 34 for information about how the bits are ordered into the LFSR.

ADDITIONAL COMMUNICATION VERIFICATION REGISTERS

The ADE9153A includes three registers that allow SPI operations to be verified. The LAST_CMD (Address 0x4AE), LAST_DATA_16 (Address 0x4AC), and LAST_DATA_32 (Address 0x423) registers record the received CMD_HDR and last read/transmitted data. The LAST_DATA_16 register contains the last data read or written during the last 16-bit transaction, and the LAST_DATA_32 register holds the data read or written during the last 32-bit transaction.

The LAST_CMD register is updated after the CMD_HDR is received. If a command to read the LAST_CMD, LAST_DATA_16, or LAST_DATA_32 registers is received, these three registers are not updated. Note that LAST_CMD[2:0] always reads back as 000.

During an SPI read operation, the LAST_DATA_16 and LAST_DATA_32 registers are updated within two master clocks after the CMD_HDR is received. If a command to read the LAST_CMD, LAST_DATA_16, or LAST_DATA_32 registers is received, these three registers are not updated.

Note that the LAST_DATA_16 and LAST_DATA_32 registers are not updated after an SPI burst read operation; these are the cases in Table 14 where next address is written.

On a write operation, LAST_DATA_16 and LAST_DATA_32 are not updated until all 16 bits or 32 bits of the write data are received. Note that, on a write register operation, the addressed register is not written until all 16 bits or 32 bits are received, depending on the length of the register.

When the LAST_CMD, LAST_DATA_16, and LAST_DATA_32 registers are read, their values remain unchanged.

CRC OF CONFIGURATION REGISTERS

The configuration register CRC feature in the ADE9153A monitors many register values.

This feature runs as a background task; it takes 10.8 ms to calculate the configuration register CRC. The result is stored in the CRC_RSLT register. If any of the monitored registers change value, the CRC_RSLT changes as well, and the CRC_CHG bit in the status register is set; this can also be configured to generate an interrupt on $\overline{\text{IRQ}}$.

After configuring the ADE9153A and writing the required registers to calibrate the measurements (such as xIGAIN or AVGAIN, for example), the configuration register CRC calculation can be started by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register. When the calculation is complete, the CRC_DONE bit is set in the status register.

The method used for calculating the configuration register CRC is also based on the CRC-16-CCITT algorithm. The most significant byte of each register is introduced into the LFSR first, without bit reversal.

Each ADE9153A has a unique CRC.

The registers included in configuration register CRC are as follows:

- AIGAIN
- APHASECAL
- AVGAIN
- AIRMS_OS
- AVRMS_OS
- APGAIN
- AWATT_OS
- AFVAR_OS
- AVRMS_OC_OS
- AIRMS_OC_OS
- BIGAIN
- BPHASECAL
- BIRMS_OS
- BIRMS_OC_OS
- CONFIG0
- VNOM
- DICOEFF
- MASK
- DIP_LVL
- DIP_CYC
- SWELL_LVL
- SWELL_CYC
- ACT_NL_LVL
- REACT_NL_LVL
- APP_NL_LVL
- ZXTOUT
- ZX_CFG
- OI_LVL
- VLEVEL
- WTHR
- VARTHR
- VATHR
- TEMP_TRIM
- CHIP_ID_HI
- CHIP_ID_LO
- RUN
- CONFIG1
- CFMODE
- COMPMODE
- ACCMODE
- CONFIG3
- CF1DEN
- CF2DEN
- ZXTHRSH
- CONFIG2
- EP_CFG
- PWR_TIME
- EGY_TIME
- CF_LCFG
- AI_PGAGAIN
- TEMP_CFG
- WR_LOCK
- 24 reserved registers

UART PROTOCOL OVERVIEW

The ADE9153A has a universal asynchronous receiver transmitter (UART) interface consisting of two pins: RX and TX. This UART interface allows an isolated communication interface to be achieved using only two low cost opto-isolators. The UART interface is compatible with 16-bit and 32-bit read/write operations. When the UART is selected, the baud rate is 4800 Baud, but a faster communication rate of 115,200 Baud can also be selected. The ADE9153A baud rates are shown in Table 15.

Table 15. UART Baud Rate

Ideal Rate (Baud)	ADE9153A Actual Rate (Baud) (CLKIN = 12.288 MHz)	Error
4800	CLKIN/2560 = 4800	0.00%
115,200	CLKIN/104 = 118153.8	2.56%

If the UART is used at 4800 Baud, no action is required when the UART interface is chosen after a reset. The 115,200 Baud rate is chosen with a single write of 0x0052 to the UART_BAUD_SWITCH register. The baud rate can be switched back to 4800 baud by writing 0x000 to the UART_BAUD_SWITCH register. UART_BAUD_SWITCH is a write only register.

The UART communication is made up of 11-bit frames with one start bit, eight data bits, one odd parity bit, and one stop bit.

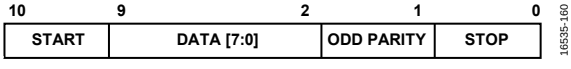

Figure 36. Frame Bits

Every UART communication starts with two command frames that contain the ADE9153A address being accessed, a read or write bit, a bit indicating whether to include the checksum, and then 00b as the lower two bits (see Figure 37).

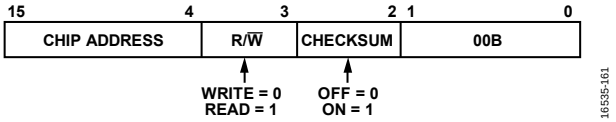

Figure 37. Command Header (CMD)

The frames are then organized with the two command header frames, followed by the data frames, and finally an optional checksum that is enabled in the command frames.

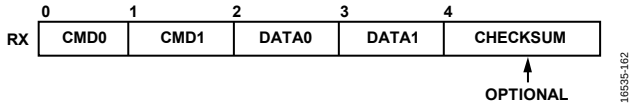

Figure 38. UART 16-Bit Write

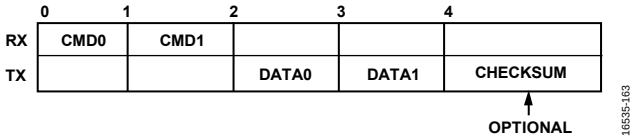

Figure 39. UART 16-Bit Read

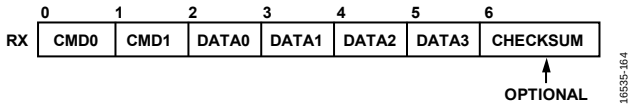

Figure 40. UART 32-Bit Write

UART Reset

The master UART can reset the UART interface on the ADE9153A by holding the TX signal low for at least 10 ms but less than 20 ms. If communication is hung up, this action can be used to reset the interface and try communication again.

UART Chip Reset

The master UART can reset the ADE9153A by holding the TX signal low for at least 20 ms; this causes a full chip reset, just like the SWRST bit in the CONFIG1 register or using the $\overline{\text{RESET}}$ pin. This way, the ADE9153A can be reset with just the UART lines crossing the isolation barrier, therefore reducing the number of isolators needed.

INTERRUPTS

The ADE9153A has two pins ($\overline{\text{IRQ}}$, and ZX/DREADY/CF2) that can be used as interrupts to the host processor. The $\overline{\text{IRQ}}$ pin goes low when an enabled interrupt occurs and stays low until the event is acknowledged by setting the corresponding status bit in the status register, respectively. The ZX/DREADY function, which is multiplexed with CF2, tracks the state of the enabled signals and goes low and high with these internal signals.

INTERRUPTS ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ pin is managed by a 32-bit interrupt mask register, mask. Each event that can generate an interrupt has a corresponding bit in the mask register and the status register.

To enable an interrupt, set the corresponding bit in the mask register to 1. To disable an interrupt, the corresponding bit in the mask register must be cleared to 0.

The status register indicates if an event that can generate an interrupt occurred. If the corresponding bit in the mask register is set, an interrupt is generated on the $\overline{\text{IRQ}}$ pin, and the pin goes low.

To determine the source of the interrupt, read the status register and identify which enabled bits are set to 1. To acknowledge the event and clear bits in the status register, write to the status register with the desired bit positions set to 1. Then, the $\overline{\text{IRQ}}$ pin goes high.

For example, if a zero crossing occurs on the Phase A voltage input, and the ZXVA bit is set in the mask register, the $\overline{\text{IRQ}}$ pin goes low, indicating that an enabled event occurred. To acknowledge the event, write a 1 to the ZXVA bit in the status register; then, the $\overline{\text{IRQ}}$ pin goes low. The ZXVA status bit is set regardless of whether the ZXVA bit is enabled in the mask register.

Interrupts on the ADE9153A are in a tiered system where it never takes more than two communications to clear an interrupt. The status register is a Tier 1 interrupt register and CHIP_STATUS, EVENT_STATUS, and MS_STATUS_IRQ are Tier 2 interrupt registers.

For the Tier 1 status register, Bits[25:0],

1. Read the status register to see which bit is set.
2. Write a 1 to the status bits that must be cleared.

For the Tier 2 status register, Bits[31:29].

1. Read the status register to see which Tier 2 register is set.
2. Read the Tier 2 register (CHIP_STATUS, EVENT_STATUS or MS_STATUS_IRQ) and the register is cleared on read.

There are a few interrupts that are nonmaskable, meaning that they are generated even if the corresponding bit in the mask register is 0. These nonmaskable interrupts include RSTDONE and CHIP_STATUS.

The meanings of the interrupt sources are provided in the related data sheet section; refer to these sections in the ADE9153A data sheet for more information.

STATUS BITS IN ADDITIONAL REGISTERS

Several interrupts are used in conjunction with other status registers.

No Load

The RFNOLOAD, VANLOAD, and ANLOAD bits in the mask register work in conjunction with additional status bits in the PHNOLOAD register.

The following bits in the mask register work with the status bits in the PHSIGN register: REVAPA, REVRPA, and REVPCFx.

Read the additional registers to obtain more information when the corresponding bits are set in the status register.

QUICK START PROCEDURE

To set up the ADE9153A, use the following procedure:

1. Wait for the RSTDONE interrupt, indicated by the $\overline{\text{IRQ}}$ pin going low.
2. Configure the PGA gain on Current Channel A and Current Channel B using the AI_PGAGAIN and BI_PGAGAIN gain registers. The default gain is 16 and 1 for Current Channel A and Current Channel B, respectively.
3. Configure CT_PHASE_DELAY with the phase delay of the CT type, 5.27 format in units of degrees. Then, calculate CT_CORNER as

   $$\tan(-CT\_PHASE\_DELAY/2^{27}) \times f_{LINE} \times 2^{27}$$

4. Set VDIV_RSMALL with the value of the small resistor in the voltage divider; for example, with a 1 MΩ to 1 kΩ divider, VDIV_RSMALL = 1000 (decimal).
5. Set COMPMODE to 0x0005.
6. It is recommended to keep the high-pass filter enabled. Set the desired corner frequency for the high-pass filter using the HPF_CRN bits in the CONFIG2 register. The default value for HPF_CRN is 6 (0.625 Hz); this is suitable for a typical application.
7. Configure the expected fundamental frequency using the SELFREQ bit (50 Hz is SELFREQ = 0; 60 Hz is SELFREQ = 1) in the ACCMODE register, and program the nominal voltage in the VLEVEL register for fundamental calculations. VLEVEL = x × 1,144,084, where x is the dynamic range that the nominal signal is at with respect to full scale.
8. Configure the zero-crossing source for zero-crossing detection. If ZX_SRC_SEL = 1 in the CONFIG0 register, data before the high-pass filter, integrator (BI only), and phase compensation is used. If ZX_SRC_SEL = 0, data after the high-pass filter, and phase compensation is used. It is recommended to have ZX_SRC_SEL = 0.
9. If energy is monitored using the CF outputs, configure the following registers. Skip this section if the CF outputs are not used.
   a. Configure the CFxSEL bits in the CFMODE register to select the energy type to monitor.
   b. Program xTHR to 0x00100000.
   c. Compute and program the corresponding CFxDEN register based on the desired impulses per kilowatt hour.
   d. Configure the CFx pulse width using the CF_LCFG register.
10. If energy is monitored using energy registers, configure the following registers:
    a. Configure the WATTACC and VARACC bits in the ACCMODE register to select amongst available accumulation modes (for example, signed, absolute, positive, or negative accumulation mode). The default accumulation mode is signed.
    b. Configure the NOLOAD_TMR bits in the EP_CFG register and set the ACT_NL_LVL, REACT_NL_LVL, and APP_NL_LVL level registers to detect no load and prevent energy accumulation of noise.
    c. Configure the EGY_TMR_MODE bit in the EP_CFG register to select sample (EGY_TMR_MODE = 0) or line cycle (EGY_TMR_MODE = 1) accumulation. Set the desired samples or half line cycles in the EGY_TIME register.
    d. Configure the EGY_LD_ACCUM bit in the EP_CFG register to add the internal energy register to the user energy register on EGYRDY (EGY_LD_ACCUM = 0), or to overwrite the user energy register with the internal energy register value (EGY_LD_ACCUM = 1).
    e. Configure the RD_RST_EN bit in the EP_CFG register to enable reset of user energy registers on read (RD_RST_EN = 1) or to disable reset of user energy registers on read (RD_RST_EN = 0).
11. The ADE9153A can provide interrupts for a variety of events on the $\overline{\text{IRQ}}$ pin. The mask and status registers manage the respective interrupt pins.
12. See the Power Quality Measurements section to configure the power quality parameters.
13. Enable the DSP by setting the run register to 1, and enable energy accumulation by setting the EGY_PWR_EN bit in the EP_CFG register to 1.
14. Note that calibration is performed once at typical operating conditions. When the calibration values are computed, write the constants to registers before enabling the DSP.
15. To prevent any changes to the ADE9153A configuration, enable write protection by writing 0x3C64 to the WR_LOCK register.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG16535-0-2/18(0)

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