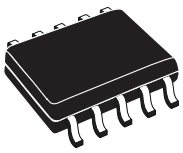
L4984D

CCM PFC controller

Datasheet - production data



SSOP10

Table 1. Device summary

Order code	Package	Packaging
L4984D	SSOP10	Tube
L4984DTR		Tape and reel

Features

- Line-modulated fixed-off-time (LM-FOT) control of CCM-operated PFC pre-regulators
- Proprietary LM-FOT modulator for nearly fixed-frequency operation
- Proprietary multiplier design for minimum THD of AC input current
- Fast “bi-directional” input voltage feedforward ($1/V^2$ correction)
- Accurate adjustable output overvoltage protection
- Protection against feedback loop failure (latched shutdown)
- Inductor saturation protection
- AC brownout detection
- Digital leading-edge blanking on current sense
- Soft-start
- 1% (at Tj = 25 °C) internal reference voltage
- - 600 / + 800 mA totem pole gate driver with active pull-down during UVLO and voltage clamp
- SSOP10 package

Applications

- PFC pre-regulators for:
  - IEC61000-3-2 and JEIDA-MITI compliant SMPS in excess of 1 KW
  - Desktop PC, server, web server

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1 Description

The L4984D is a current-mode PFC controller operating with line-modulated fixed-off-time (LM-FOT) control. A proprietary LM-FOT modulator allows fixed-frequency operation for boost PFC converters as long as they are operated in CCM (continuous conduction mode).

The chip comes in a 10-pin SO package and offers a low-cost solution for CCM-operated boost PFC pre-regulators in EN61000-3-2 and JEIDA-MITI compliant applications, in a power range that spans from few hundred W to 1 KW and above.

The highly linear multiplier includes a special circuit, able to reduce the crossover distortion of the AC input current, that allows wide-range-mains operation with a reasonably low THD, even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% at Tj = 25 °C) internal voltage reference. Loop stability is optimized by the voltage feedforward function ($1/V^2$ correction), which in this IC uses a proprietary technique that also significantly improves line transient response in the case of mains drops and surges (“bi-directional”).

The device features low consumption and includes a disable function suitable for IC remote on/off. These features allow use in applications which also comply with the latest energy saving requirements (Blue Angel, ENERGY STAR®, Energy 2000, etc.).

In addition to overvoltage protection able to keep the output voltage under control during transient conditions, the IC is also provided with protection against feedback loop failures or erroneous settings. Other onboard protection functions allow that brownout conditions and boost inductor saturation can be safely handled. Soft-start limits peak current and extends off-time to prevent flux runaway in the initial cycles.

The totem pole output stage, capable of 600 mA source and 800 mA sink current, is suitable for big MOSFETs or IGBT drive.

2 Block diagram

Figure 1. Electrical diagram

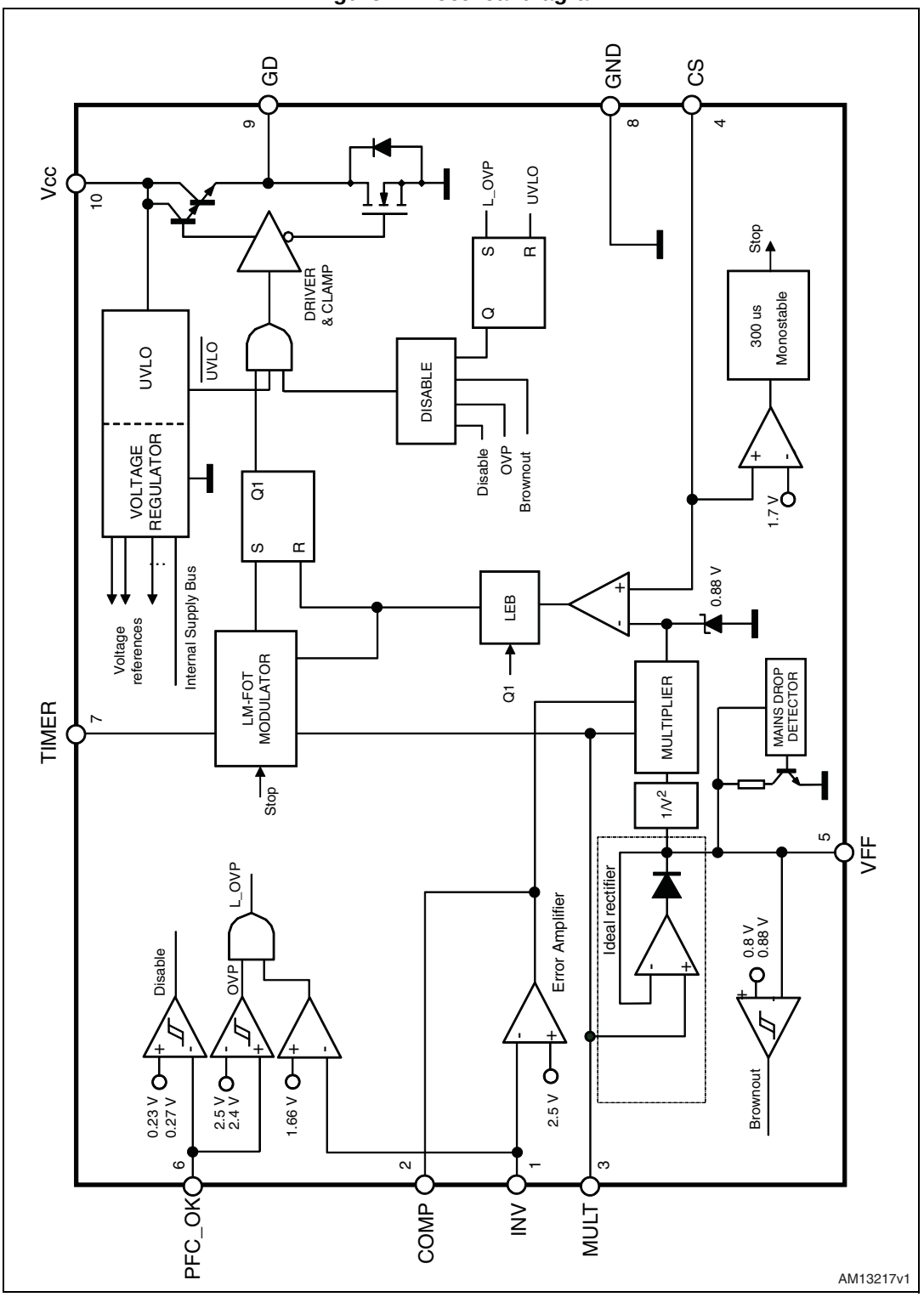


Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	10	IC supply voltage (Icc = 20 mA)	Self-limited	V
-	1, 3, 6	Max. pin voltage (I_{pin} = 1 mA)	Self-limited	V
-	2, 4, 5, 7	Analog inputs & outputs	-0.3 to 8	V
VFF pin	5	Maximum withstanding voltage range test condition: ANSI/ESDA/JEDEC JS001	+/- 1500	V
Other pins	1 to 4 6 to 10		+/- 2000	V

Figure 2. Pin connection (top view)

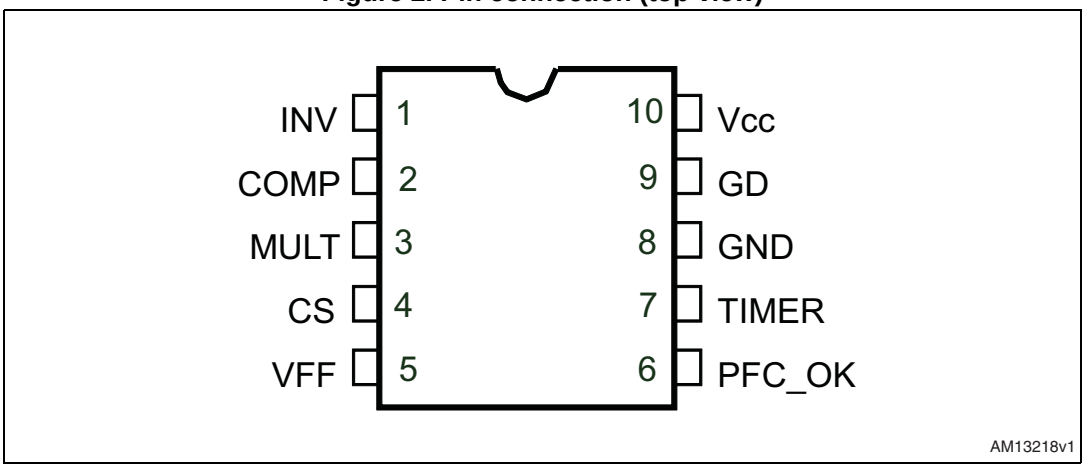


Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rth j-amb	Max. thermal resistance, junction-to-ambient	120	°C/W
Ptot	Power dissipation at T_{amb} = 50 °C	0.75	W
Tj	Junction temperature operating range	-40 to 150	°C
Tstg	Storage temperature	-55 to 150	°C

Table 4. Pin functions

N.	Name	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. The pin normally features high impedance.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin 1) to achieve stability of the voltage control loop and ensure high power factor and low THD. To avoid uncontrolled rise of the output voltage at zero load, when the voltage on the pin falls below 2.4 V the gate driver output is inhibited (burst-mode operation).

Table 4. Pin functions (continued)

N.	Name	Function
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop. The voltage on this pin is used also to derive the information on the RMS mains voltage. At startup this pin is used also to perform soft-start. This pin can also be used as a remote ON-OFF control input by means of the internal brownout comparator. In this case the IC performs the soft-start function when the pin is released.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor; the resulting voltage is applied to this pin and compared to an internal sinusoidal-shaped reference, generated by the multiplier, to determine the turn-off instant of the external Power MOSFET. The pin is equipped with about 220 ns digital leading-edge blanking for improved noise immunity. A second comparison level set at 1.7 V detects abnormal currents (e.g. due to boost inductor saturation) and, on this occurrence, activates a safety procedure that temporarily stops the converter and limits the stress of the power components.
5	VFF	Second input to the multiplier for $1/V^2$ function. A capacitor and a parallel resistor must be connected from the pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The resistor should range from 100 kΩ (minimum) to 2 MΩ (maximum). The voltage on this pin, a DC level equal to the peak voltage on pin MULT (3), compensates the control loop gain dependence on the mains voltage. This pin is also internally connected to a comparator in order to provide brownout (AC mains undervoltage) protection. A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. The IC restarts as the voltage at the pin goes above 0.88 V. Never connect the pin directly to GND.
6	PFC_OK	PFC pre-regulator output voltage monitoring/disable function. This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage on the pin exceeds 2.5 V, the IC stops switching and restarts as the voltage falls below 2.4 V. However, if at the same time the voltage on the INV pin falls below 1.66 V, a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling V_{CC}. If the voltage on this pin is brought below 0.23 V, the IC is shut down. To restart the IC the voltage on the pin must go above 0.27 V. This pin can also be used as a burst-mode control input to synchronize the burst-mode of the IC to the one of a D2D converter controller. Do not use this pin as remote ON/OFF control input because the soft-start function is performed only at the startup by PFC_OK but not on the following releases.
7	TIMER	LM-FOT modulator setting. A capacitor connected between this pin and ground is charged by an accurate internal generator during the off-time of the external Power MOSFET (i.e. while pin GD is low), therefore generating a voltage ramp. As the voltage ramp equals the voltage on the MULT pin, the off-time of the Power MOSFET is terminated, the GD pin is driven high and the ramp is reset at zero.
8	GND	Ground. Current return for both the signal part of the IC and the gate driver. Keep the PCB trace that goes from this pin to the “cold” end of the sense resistor separate from the trace that collects the grounding of the bias components (output voltage sensing divider, multiplier bias divider and LM-FOT modulator setting).

Table 4. Pin functions (continued)

N.	Name	Function
9	GD	Gate driver output. The totem pole output stage is able to drive Power MOSFETs and IGBTs. It is capable of 600 mA source current and 800 mA sink current (minimum values). The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high V_{CC}.
10	V_{CC}	Supply voltage of both the signal part of the IC and the gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND may be useful in order to get a clean bias voltage for the signal part of the IC. The voltage on the pin is internally clamped at 22.5 V min. to protect the internal circuits from excessive supply voltages.

3 Electrical characteristics

(Tj = -25 to 125 °C, V_{CC} = 12 V,[a] CTIMER = 470 pF, Co = 1 nF between pin GD and GND, C_{FF} = 1 µF and R_{FF} = 1 MΩ between pin VFF and GND; unless otherwise specified.)

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	10.3		22.5	V
V_{CCOn}	Turn-on threshold	(1)	11	12	13	V
V_{CCOff}	Turn-off threshold	(1)	8.7	9.5	10.3	V
$V_{CCrestart}$	V_{CC} for resuming from latch	OVP latched	5	6	7	V
Hys	Hysteresis		2.3		2.7	V
V_Z	Zener voltage	Icc = 20 mA	22.5	25	28	V
Supply current						
$I_{start-up}$	Startup current	Before turn-on, V_{CC} = 10 V		65	150	µA
I_q	Quiescent current	After turn-on, V_{MULT} = 1 V		4	5	mA
I_{CC}	Operating supply current	At 70 kHz		5	6.0	mA
I_{qdis}	Idle state quiescent current	$V_{PFC\_OK} > V_{PFC\_OK\_S}$ and $V_{INV} < V_{INVD}$		200	280	µA
		$V_{PFC\_OK} < V_{PFC\_OK\_D}$		1.5	2.2	mA
I_q	Quiescent current	$V_{PFC\_OK} > V_{PFC\_OK\_S}$ or $V_{COMP} < 2.3$ V		2.2	3	mA
Multiplier input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 3 V		-0.2	-1	µA
V_{MULT}	Linear operation range		0 to 3			V
V_{CLAMP}	Internal clamp level	I_{MULT} = 1 mA	9	9.5		V
$\frac{\Delta V_{CS}}{\Delta V_{MULT}}$	Output max. slope	V_{MULT} = 0 to 0.4 V V_{VFF} = 0.915 V V_{COMP} = upper clamp	0.935	1.34		V/V
K_M	Gain(2)	$V_{MULT} = V_{COMP}$ = 0.915 V V_{COMP} = 4 V	0.248	0.304	0.360	V
Error amplifier						
V_{INV}	Voltage feedback input threshold	Tj = 25 °C	2.475	2.5	2.525	V
		10.3 V < V_{CC} < 22.5 V (1)	2.455		2.545	

a. Adjust V_{CC} above V_{CCOn} before setting at 12 V.

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
	Line regulation	V_{CC} = 10.3 V to 22.5 V		2	5	mV
I_{INV}	Input bias current	V_{INV} = 0 to 4 V		-0.2	-1	µA
$V_{INVCLAMP}$	Internal clamp level	I_{INV} = 1 mA	8	9		V
Gv	Voltage gain	Open loop	60	80		dB
GB	Gain-bandwidth product			1		MHz
I_{COMP}	Source current	V_{COMP} = 4 V, V_{INV} = 2.4 V	2	4		mA
	Sink current	V_{COMP} = 4 V, V_{INV} = 2.6 V	2.5	4.5		mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5 mA	5.7	6.2	6.7	V
	Burst-mode threshold	(1)	2.3	2.4	2.5	
	Lower clamp voltage	I_{SINK} = 0.5 mA (3)	2.1	2.25	2.4	
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			1	µA
t_{LEB}	Leading edge blanking		145	220	400	ns
$td_{(H-L)}$	Delay to output		100	200	300	ns
$V_{CSclamp}$	Current sense reference clamp	V_{COMP} = upper clamp V_{MULT} = V_{VFF} = 0.915 V (1)	0.84	0.88	0.93	V
Vcs_{ofst}	Current sense offset (2)	V_{MULT} = 0, V_{VFF} = 3 V		35	47	mV
		V_{MULT} = 3 V, V_{VFF} = 3 V		10		
Boost inductor saturation detector						
V_{CS_th}	Threshold on current sense	(1)	1.6	1.7	1.8	V
I_{INV}	E/A input pull-up current	V_{CS} > V_{CS_th}, before restart	5	10	13	µA
t_{START}	Restart delay			300		µs
Pfc_ok functions						
I_{PFC_OK}	Input bias current	V_{PFC_OK} = 0 to 2.6 V		-0.1	-1	µA
$V_{PFC\_OK\_C}$	Clamp voltage	I_{PFC_OK} = 1 mA	9	9.5		V
$V_{PFC\_OK\_S}$	OVP threshold	(1) Voltage rising	2.435	2.5	2.565	V
$V_{PFC\_OK\_R}$	Restart threshold after OVP	(1) Voltage falling	2.34	2.4	2.46	V
$V_{PFC\_OK\_D}$	Disable threshold	(1) Voltage falling	0.12	0.23	0.35	V
$V_{PFC\_OK\_E}$	Enable threshold	(1) Voltage rising	0.15	0.27	0.38	V
Feedback failure detection						
V_{INVD}	Feedback failure detection threshold (on V_{INV})	(1) Voltage falling, V_{PFC_OK} = $V_{PFC\_OK\_S}$	1.61	1.66	1.71	V
Voltage feedforward						
V_{VFF}	Linear operation range		1		3	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
ΔV	Dropout V_{MULTpk}-V_{VFF}	Before turn-on			800	mV
		After turn-on			20	
ΔV_{VFF}	Line drop detection threshold	Below peak value	25	60	100	mV
ΔV_{VFF}	Line drop detection threshold	Below peak value Tj = 0 to 100 °C	40	70	100	mV
R_{DISCH}	Internal discharge resistor		5	10	20	kΩ
V_{DIS}	Disable threshold	(1) Voltage falling	0.745	0.8	0.855	V
V_{EN}	Enable threshold	(1) Voltage rising	0.845	0.88	0.915	V
Fixed-off-time modulator						
I_{TIMER}	Programming current	V_{MULT} = 1 V	142	153	163	µA
T_{OFF}	Programmed off-time	V_{MULT} = 1 V	2.88	3.09	3.30	µs
R_{DIS}	Discharge resistance		35	60	120	W
C_{TIMER}	Timing capacitor range		0.1		2.2	nF
T_{OFF_pk}	Programming range	On the peak of V_{MULT}	1.45		50	µs
Soft-start						
T_{SS}	Activation time			300		µs
V_{MULTx}	Pull-up voltage	10 kΩ from MULT to GND		4.1		V
Gate driver						
V_{OL}	Output low voltage	I_{sink} = 100 mA		0.6	1.2	V
V_{OH}	Output high voltage	I_{source} = 5 mA	9.8	10.3		V
I_{srcpk}	Peak source current		-0.6			A
I_{snkpk}	Peak sink current		0.8			A
t_f	Voltage fall time			30	60	ns
t_r	Voltage rise time			45	110	ns
V_{Oclamp}	Output clamp voltage	I_{source} = 5 mA; Vcc = 20 V	10	12	15	V
	UVLO saturation	V_{CC} = 0 to V_{CCon}, I_{sink} = 2 mA			1.1	V

1. Parameters tracking each other.
2. The multiplier output is given by:

$$V_{CS} = V_{CS\_Offset} + K_M \cdot \frac{V_{MULT} \cdot (V_{COMP} - 2.5)}{V_{VFF}^2}$$

4 Typical electrical performance

Figure 3. IC consumption vs. V_{CC}

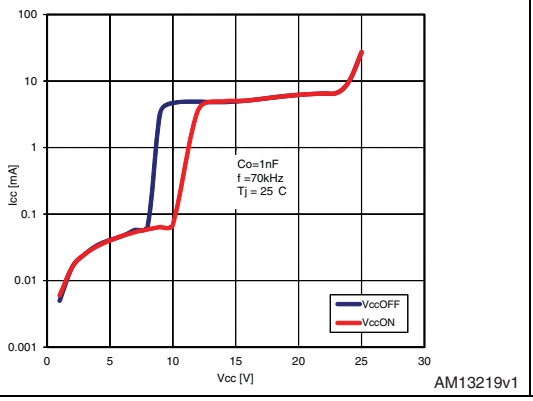


Figure 4. IC consumption vs. Tj

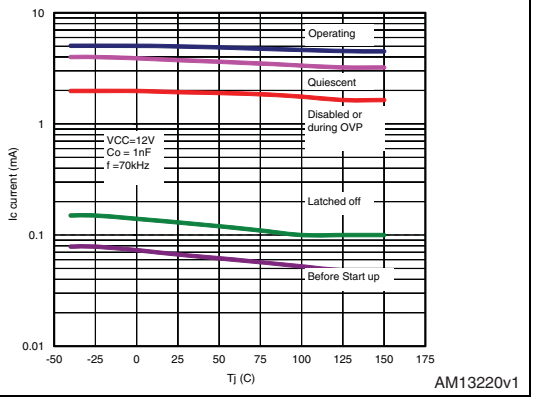


Figure 5. V_{CC} Zener voltage vs. Tj

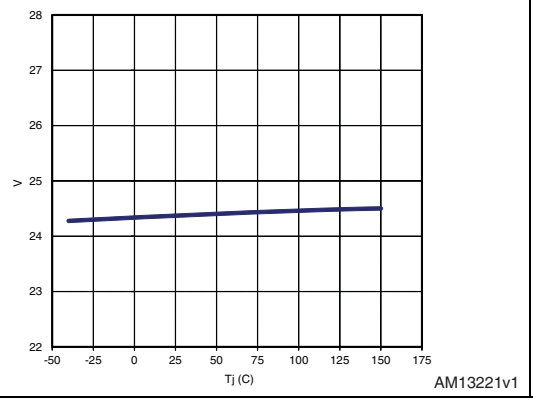


Figure 6. Startup & UVLO vs. Tj

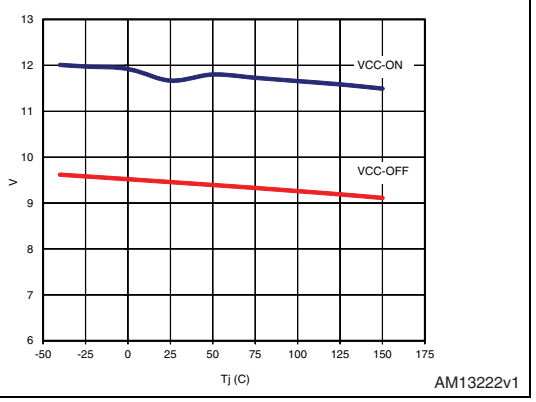


Figure 7. Feedback reference vs. Tj

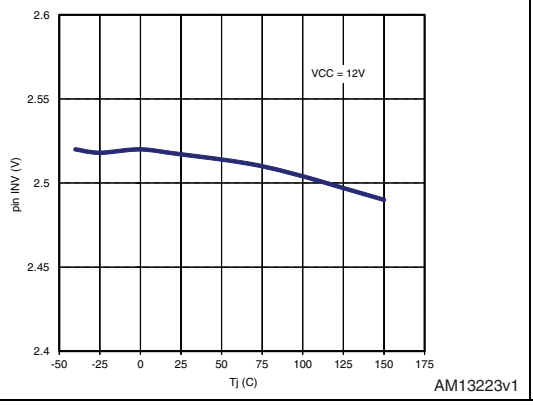


Figure 8. E/A output clamp levels vs. Tj

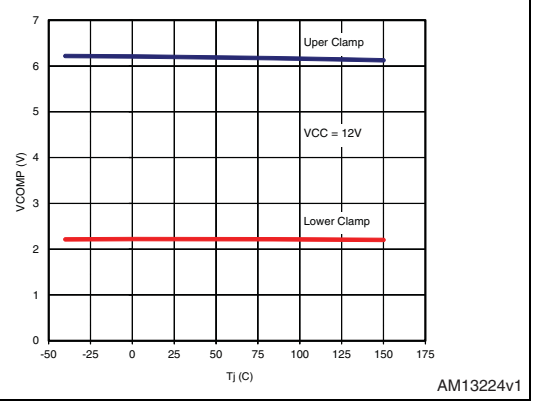


Figure 9. UVLO saturation vs. Tj

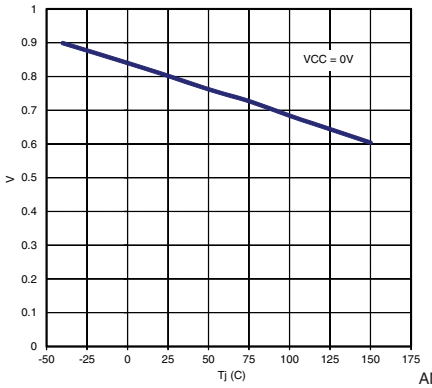


Figure 10. OVP levels vs. Tj

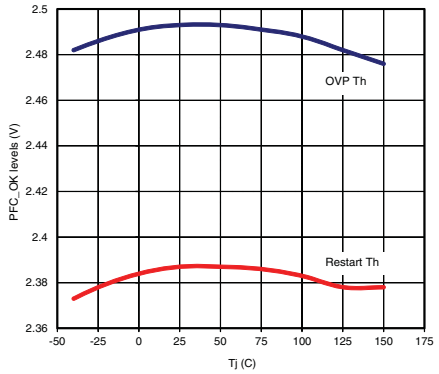


Figure 11. Inductor saturation threshold vs. Tj

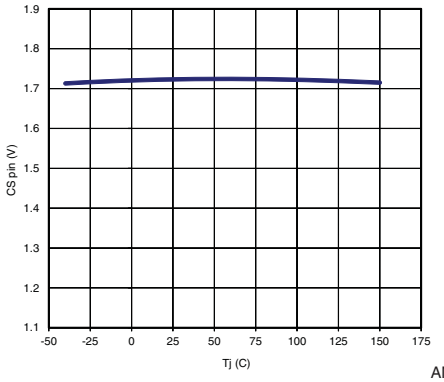


Figure 12. V_{cs} clamp vs. Tj

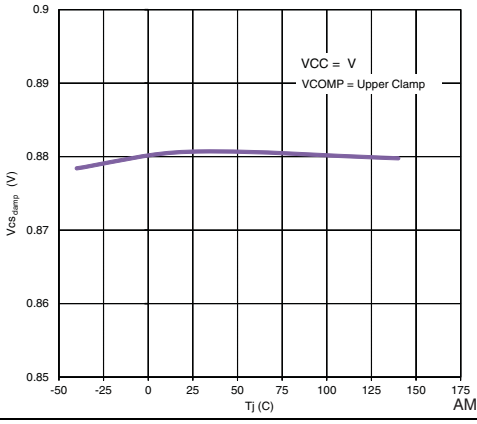


Figure 13. Timer pin charging current vs. Tj

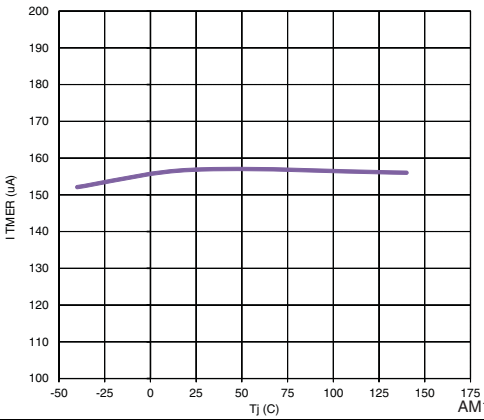


Figure 14. Brownout threshold (on VFF) vs. Tj

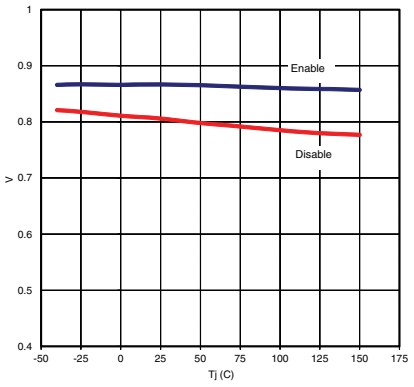


Figure 15. R_{FF} discharge vs. Tj

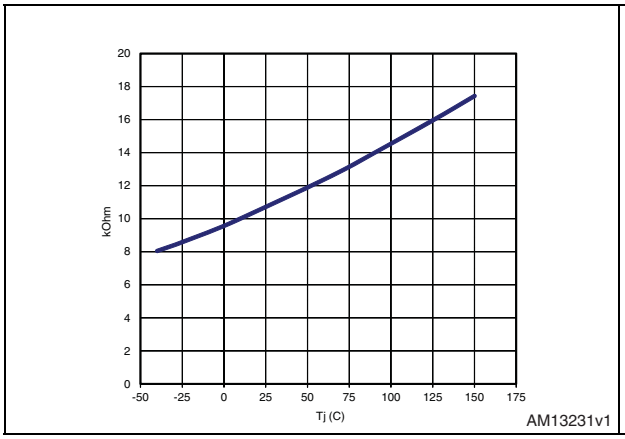


Figure 16. Line drop detection threshold vs. Tj

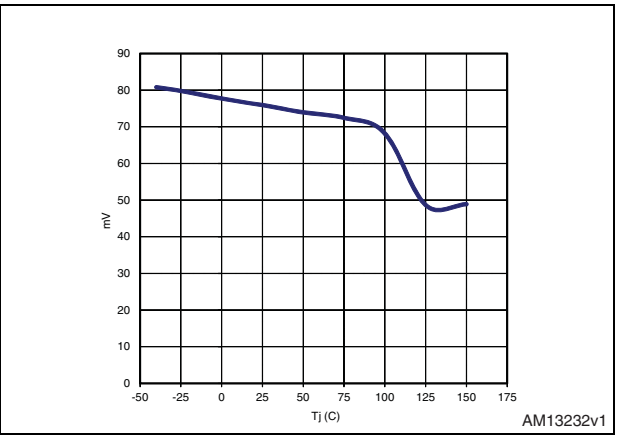


Figure 17. V_{MULTpk} - V_{VFF} dropout vs. Tj

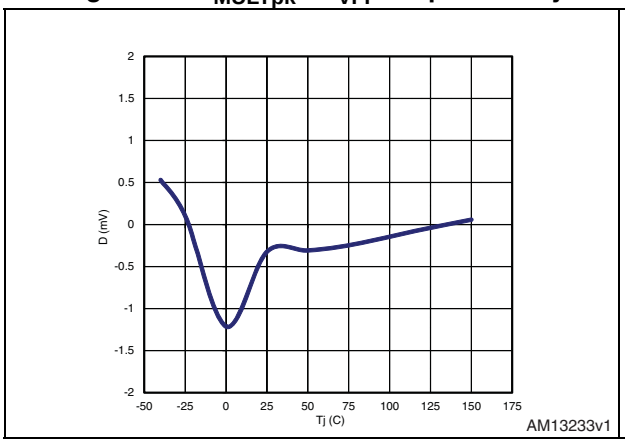


Figure 18. PFC_OK enable threshold vs. Tj

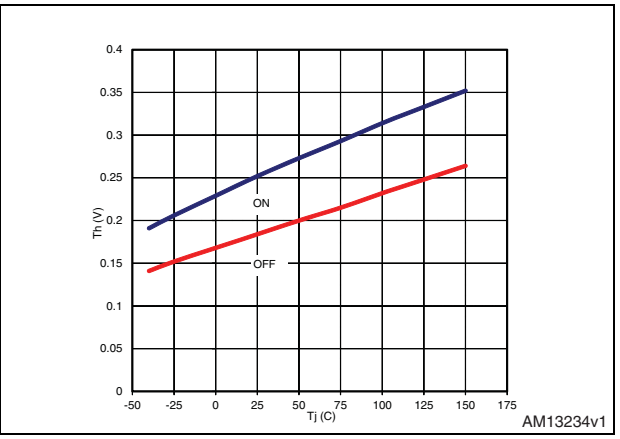


Figure 19. FFD threshold vs. Tj

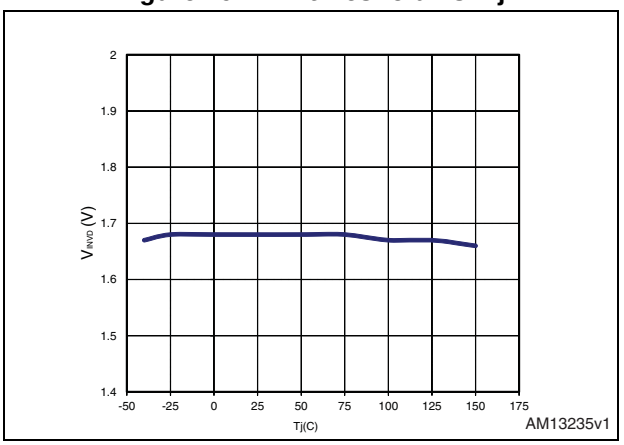


Figure 20. Multiplier characteristics at V_{FF}=1 V

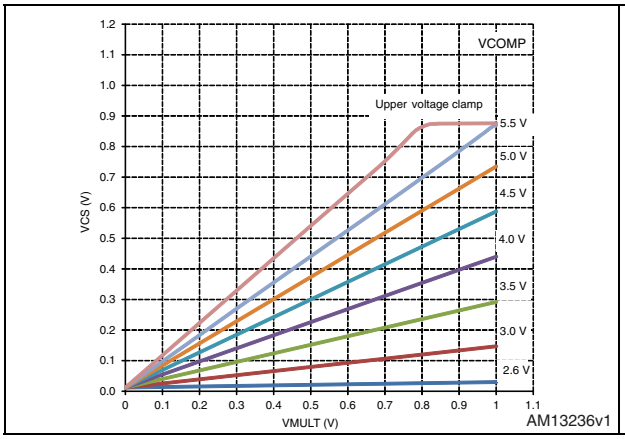


Figure 21. Multiplier characteristics at V_{FF}=3 V

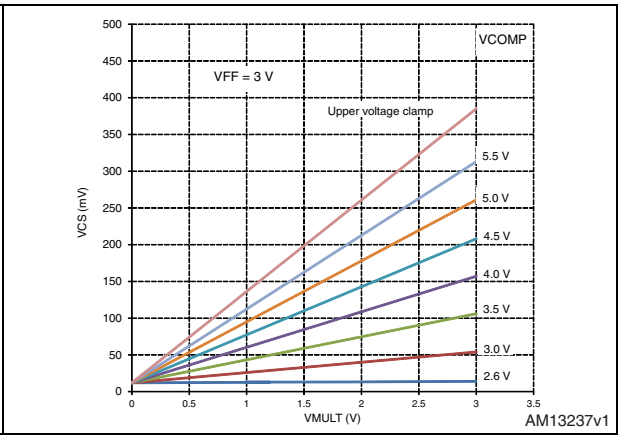


Figure 22. Multiplier gain vs. Tj

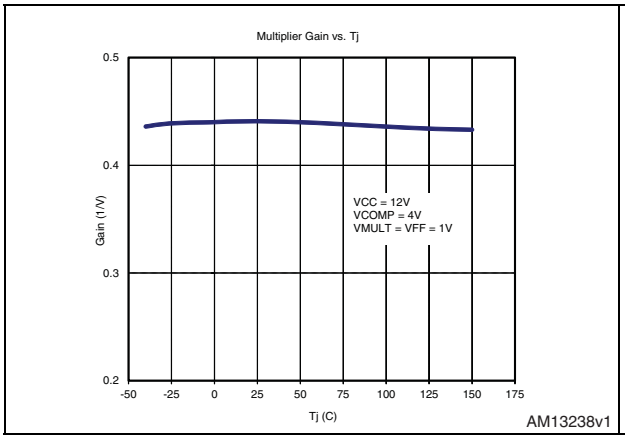


Figure 23. Gate drive clamp vs. Tj

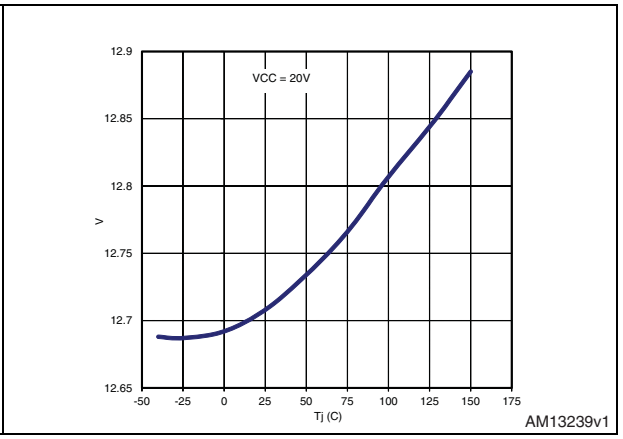


Figure 24. Gate drive output saturation vs. Tj

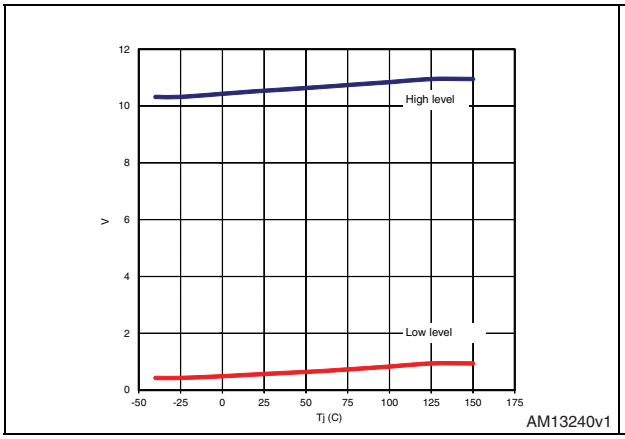
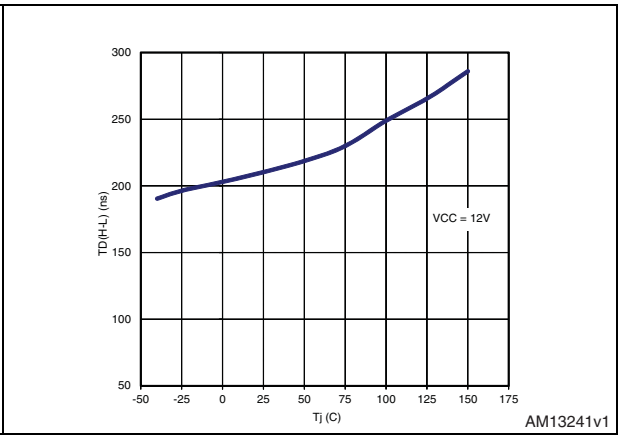


Figure 25. Delay to output vs. Tj



5 Application information

5.1 Theory of operation

The L4984D implements conventional “peak” current mode control, where the on-time TON of the external power switch is determined by the peak inductor current reaching the programmed value. The off-time TOFF, instead, is determined by a special fixed-off-time (FOT) modulator in such a way that the resulting switching period is constant as long as the boost converter is operated in CCM (i.e. the current in the boost inductor remains greater than zero in a switching cycle).

To understand how TOFF needs to be modulated to achieve a fixed switching frequency independent of the instantaneous line voltage and the load, it is useful to consider the V·s balance equation for the boost inductor under the assumption of CCM operation:

Equation 1

$$T_{ON}\,Vpk\sin\theta = T_{OFF}\left(Vout - Vpk\sin\theta\right)$$

where Vpk is the peak line voltage, Vout the regulated output voltage and θ the instantaneous phase angle of the line voltage. Solving for TON, we get:

Equation 2

$$T_{ON} = \left(\frac{Vout}{Vpk\sin\theta} - 1\right)T_{OFF}$$

then, the switching period T_{SW} is:

Equation 3

$$T_{sw} = T_{ON} + T_{OFF} = \left(\frac{Vout}{Vpk\sin\theta} - 1\right)T_{OFF} + T_{OFF} = \frac{Vout}{Vpk\sin\theta}T_{OFF}$$

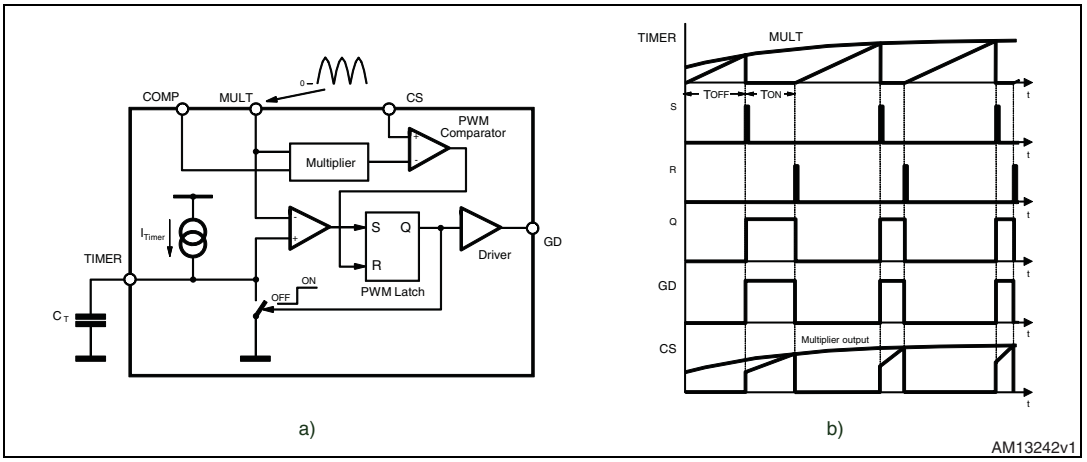
In the end, if T_{OFF} is changed proportionally to the instantaneous line voltage, i.e. if:

Equation 4

$$T_{OFF} = K_t\,Vpk\sin\theta$$

then T_{SW} is equal to $K_t \cdot V_{out}$ and, since V_{out} is regulated by the voltage loop, also T_{SW} (and $f_{SW} = 1/T_{SW}$) is fixed. This result is based on the sole assumption that the instantaneous line voltage and the output load are such that the boost inductor operates in CCM.

Figure 26. Line-modulated fixed-off-time modulator: a) internal block diagram; b) key waveforms



With reference to the schematic and the relevant key waveforms in *Figure 26*, an off-time proportional to the instantaneous line voltage is achieved by charging the capacitor CT with a constant current ITIMER, accurately fixed internally and temperature compensated, while the MOSFET is off and commanding MOSFET turn-on (and resetting CT at zero) as the voltage across CT equals that on the MULT pin. The voltage on this pin is:

Equation 5

$$V_{MULT} = K_P \, Vpk \sin\theta$$

where KP is the divider ratio of the resistors biasing the MULT pin. As a result:

Equation 6

$$T_{OFF} = \frac{C_T}{I_{TIMER}} K_P \, Vpk \sin\theta \quad \rightarrow \quad K_t = \frac{C_T}{I_{TIMER}} K_P$$

and the switching frequency is:

Equation 7

$$f_{sw} = \frac{1}{T_{sw}} = \frac{I_{TIMER}}{K_P \, C_T \, Vout} = \frac{1}{K_t \, Vout}$$

The timing capacitor CT, therefore, is selected with the following design formula:

Equation 8

$$C_T = \frac{I_{TIMER}}{K_P \, Vout \, f_{sw}}$$

V_{out} and fsw are design specifications, K_P is chosen so that the voltage on the MULT pin is within the multiplier linearity range (0 to 3 V) and ITIMER is specified in *Section 3: Electrical characteristics*.

Along a line half-cycle, TOFF goes all the way from a minimum near the zero-crossing to a maximum on the sinusoid peak. It is important to check that the off-time occurring on the peak of the voltage sinusoid at minimum input voltage is greater then the minimum programmable value:

Equation 9

$$T_{OFF\,min} = \frac{C_T}{I_{TIMER}} K_P \, Vpk_{min} > 1.45\ \mu s$$

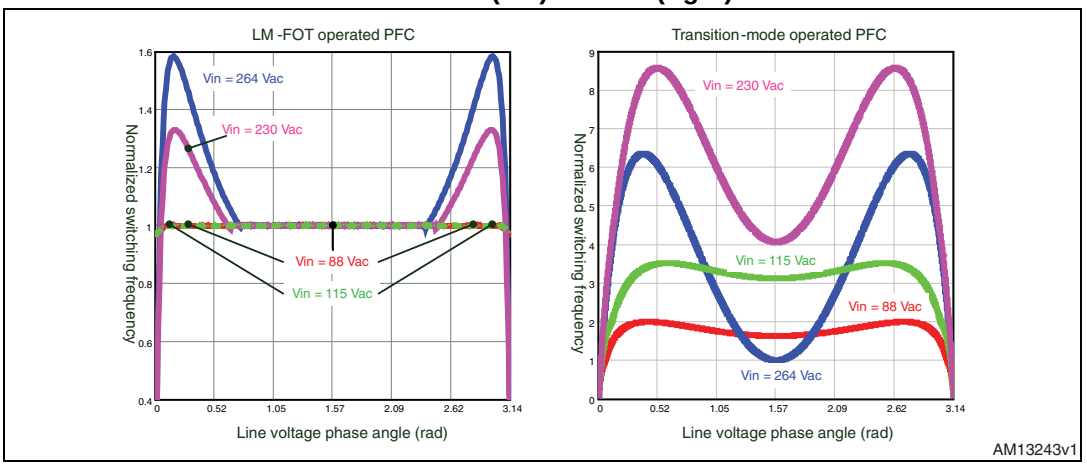
This constraint limits the maximum programmable frequency at:

Equation 10

$$f_{sw.max} = 690 \frac{Vpk_{min}}{Vout} \ [kHz]$$

As the line RMS voltage is increased and/or the output load is decreased, the boost inductor current tends to become discontinuous starting from the region around the zero-crossings. As a result, the switching frequency is no longer constant and tends to increase. However, the frequency rise is significantly lower as compared to that in a transition-mode (TM) operated boost PFC stage, as illustrated in *Figure 25*. The switching frequency can exceed fsw.max in the region where the inductor current is discontinuous.

Figure 27. Typical frequency change along a line half-cycle in a boost PFC operated in LM-FOT (left) and TM (right)



In this example the voltage ripple appearing across the output capacitor Cout has been neglected. This ripple at twice the line frequency fL has peak amplitude ΔVout proportional to the output current Iout:

Equation 11

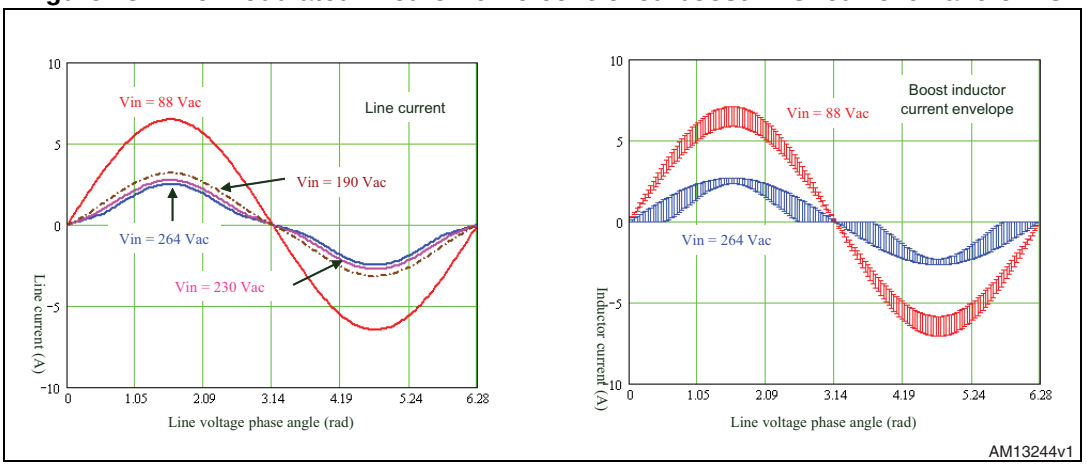
$$\Delta Vout = \frac{Iout}{4\pi f_L \, Cout}$$

As a consequence, fsw is not exactly constant but is modulated at 2fL, which spreads the spectrum of the electrical noise injected back into the power line and facilitates the compliance with conducted EMI emission regulations. The relative frequency change due to the output voltage ripple is:

Equation 12

$$\frac{\Delta f_{sw}}{f_{sw}} = \frac{\frac{\Delta Vout}{Vout}}{1+\frac{\Delta Vout}{Vout}}$$

Figure 28. Line-modulated fixed-off-time-controlled boost PFC: current waveforms

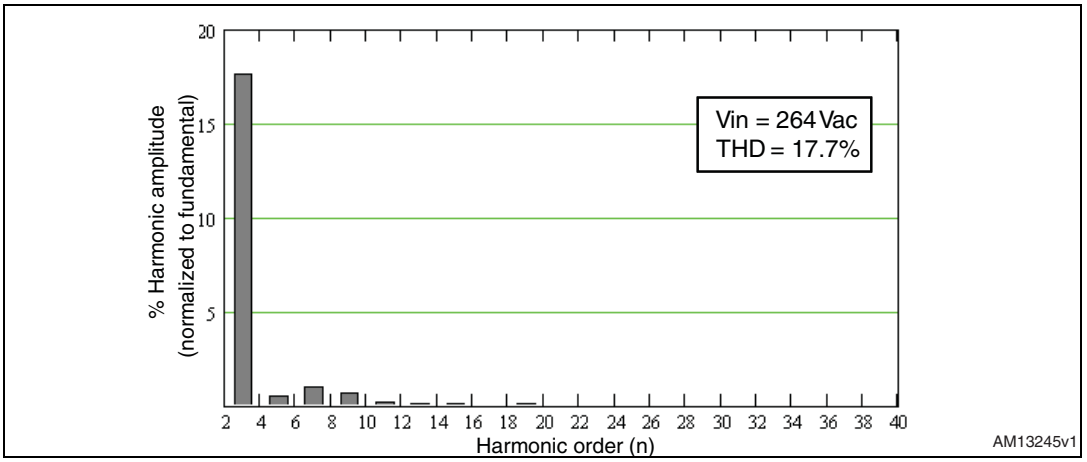


As a result of the operation of the circuit in *Figure 26*, the current that the boost PFC pre-regulator draws from the power line is not exactly sinusoidal but is affected by distortion that is lower as the current ripple in the boost inductor is smaller as compared to its peak value. *Figure 28* shows some theoretical waveforms, relevant to full load condition, in a line cycle at different input voltages.

In the diagram on the left-hand side the line (input) current waveform is shown for different line voltages, while on the right-hand side the envelope of the inductor current at minimum and maximum line voltage is shown.

The input current waveform relevant to Vin = 88 V_{ac} shows no visible sign of distortion; the operation of the boost inductor is CCM throughout the entire line cycle as testified by the inductor current envelope. The brown waveform is relevant to Vin = 190 V_{ac}, which is the condition where CCM operation no longer occurs at zero-crossings (this voltage value, for a given power level, depends on the inductance value of the boost inductor); a certain degree of distortion is already visible.

Figure 29. Line-modulated fixed-off-time-controlled boost PFC: input current harmonic contents

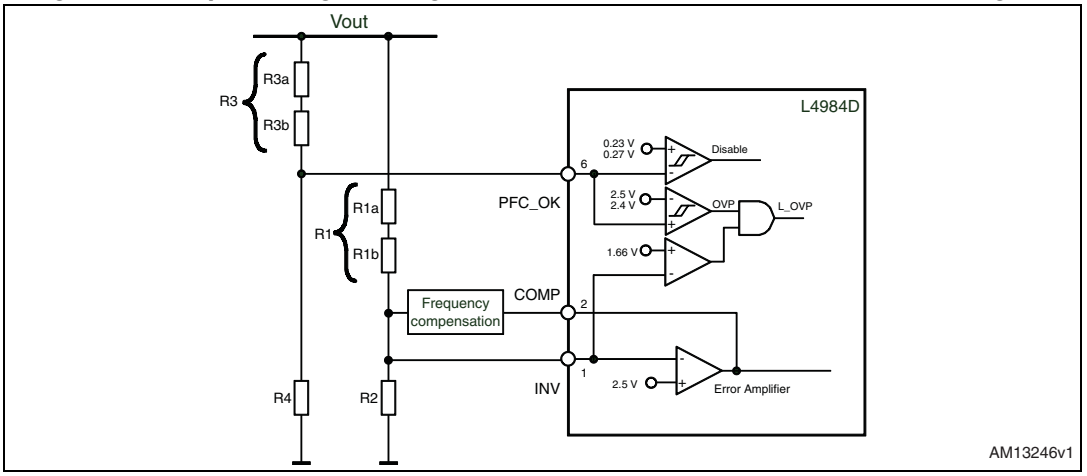


The waveform relevant to Vin = 264 V_{ac} shows the highest degree of distortion and the largest portion of the line cycle where boost inductor operates in discontinuous mode (DCM). However, its harmonic content, shown in *Figure 29*, is still so low that it is not an issue for EMC compliance. Almost all the distortion is concentrated in the third harmonic, whose amplitude is 17% of the fundamental one, while the THD is 17.7%.

6 Overvoltage protection (OVP)

Normally, the voltage control loop keeps the output voltage Vout of the PFC pre-regulator close to its nominal value, set by the ratio of the resistors R1 and R2 of the output divider. A pin of the device (PFC_OK) has been dedicated to monitor the output voltage with a separate resistor divider (R3 high, R4 low, see *Figure 30*). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value, usually larger than the maximum Vout that can be expected.

Figure 30. Output voltage setting, OVP and FFD functions: internal block diagram



Note: Example: V_{out} = 400 V, V_{outx} = 434 V.

Select: R3 = 8.8 M; then: R4 = 8.8 M ·2.5/(434-2.5) = 51 k.

When this function is triggered, the gate drive activity is immediately stopped until the voltage on the pin PFC_OK drops below 2.4 V. Notice that R1, R2, R3 and R4 can be selected without any constraints. The unique criterion is that both dividers must sink a current from the output bus which needs to be significantly higher than the bias current of both pins INV and PFC_OK (< 1 µA).

7 Feedback failure detection (FFD)

The OVP function handles “normal” overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. If the overvoltage is generated by a feedback failure, for instance when the upper resistor of the output divider (R1) fails open, eventually the error amplifier output (COMP) saturates high and the voltage on its inverting input (INV) drops from its steady-sate value (2.5 V). An additional comparator monitors the voltage on the INV pin, comparing it against a reference located at 1.66 V. When the voltage on pin PFC_OK exceeds 2.5 V and, simultaneously, that on the INV pin falls below 1.66 V, the FFD function is triggered: the gate drive activity is immediately stopped, the device is shut down and its quiescent consumption reduced. This condition is latched and to restart the IC it is necessary to recycle the input power, so that the V_{CC} voltage goes below 6 V. The pin PFC_OK doubles its function as a not-latched IC disable: a voltage below 0.23 V shuts down the IC, reducing its consumption below 2 mA. To restart, simply let the voltage on the pin go above 0.27 V. Note that these functions offer complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a pin PFC_OK floating results in shutting down the IC and stopping the pre-regulator.

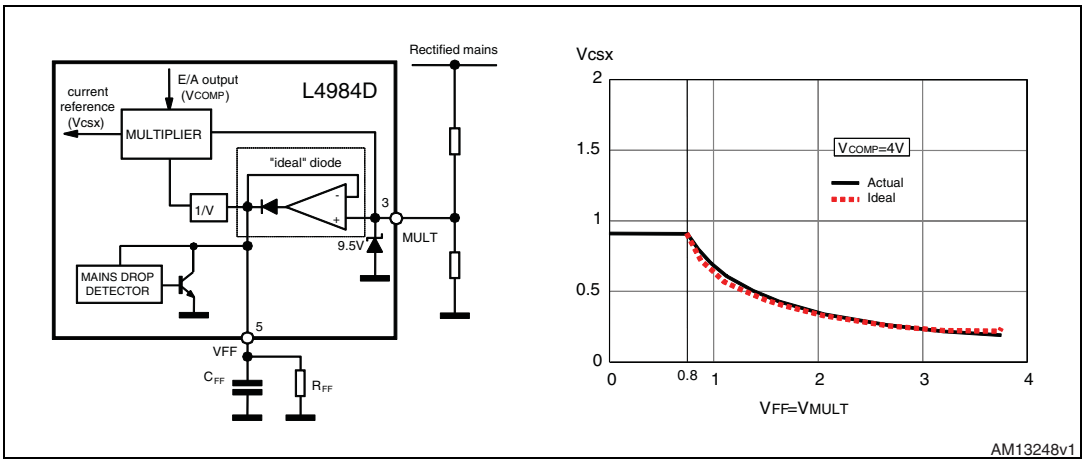
8 Voltage feedforward

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. So does the crossover frequency fc of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design.

For example, setting the gain of the error amplifier to get fc = 20 Hz at 264 V_{ac} means having fc = 4 Hz at 88 V_{ac}, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Input voltage feedforward compensates for the gain variation with the line voltage and allows all of the above-mentioned issues to be minimized. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit (1/V2 corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (see *Figure 31*).

Figure 31. Voltage feedforward: squarer-divider (1/V2) block diagram and transfer characteristic



In this way, if the line voltage doubles the amplitude of the multiplier, output is halved and vice versa, so that the current reference is adapted to the new operating conditions with (ideally) no need to invoke the slow response of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

Actually, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small, the voltage generated is affected by a considerable amount of ripple at twice the mains frequency that causes distortion of the current reference (resulting in high THD and poor PF); if it is too large there is a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator output voltage in response to large line voltage changes. Clearly, a trade-off is required.

The L4984D realizes a new voltage feedforward that, using just two external parts, strongly minimizes this time constant trade-off issue whichever voltage change occurs on the mains,

both surges and drops. A capacitor C_{FF} and a resistor R_{FF}, connected from the VFF pin to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the voltage applied on the MULT pin. In this way, in case of sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode; in case of line voltage drop, an internal “mains drop” detector enables a low impedance switch that suddenly discharges C_{FF}, therefore reducing the settling time needed to reach the new voltage level. The discharge of C_{FF} is stopped when either its voltage equals the voltage on the MULT pin or the voltage on the VFF pin falls below 0.88 V, to prevent the “brownout protection” function from being improperly activated (see *Section 12: Power management and housekeeping functions*). With this functionality, an acceptably low steady-state ripple of the VFF voltage (and, then, low current distortion) can be achieved with a limited undershoot or overshoot on the pre-regulator output during line transients.

The twice-mains-frequency (2· fL) ripple appearing across C_{FF} is triangular with peak-to-peak amplitude that, with good approximation, is given by:

Equation 13

$$\Delta V_{FF} = \frac{2 V_{MULTpk}}{1 + 4 f_L R_{FF} C_{FF}}$$

where fL is the line frequency. The amount of 3rd harmonic distortion introduced by this ripple, related to the amplitude of its 2· fL component, is:

Equation 14

$$D_3\% = \frac{100}{2\pi f_L R_{FF} C_{FF}}$$

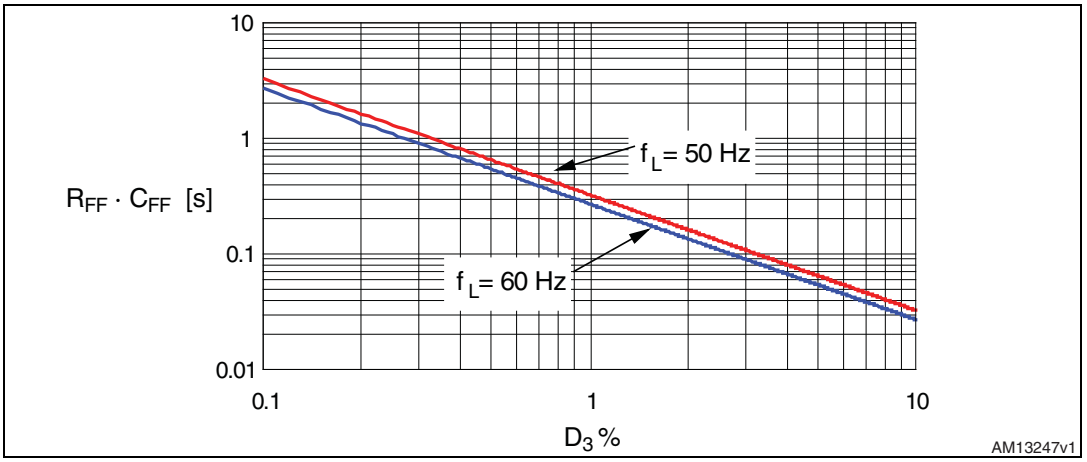
Figure 32 shows a diagram that helps choose the time constant $R_{FF}{\cdot}C_{FF}$ based on the amount of maximum desired 3rd harmonic distortion. Note, however, that there is a minimum value for the time constant $R_{FF}{\cdot}C_{FF}$ below which improper activation of the VFF fast discharge may occur. In fact, the twice-mains-frequency ripple across C_{FF} under steady-state conditions must be lower than the minimum line drop detection threshold (ΔV_{VFF_min} = 40 mV). Therefore:

Equation 15

$$R_{FF} \cdot C_{FF} > \frac{2\frac{V_{MULTpk\_max}}{\Delta V_{VFF\_min}} - 1}{4 f_{L\_min}}$$

Always connect R_{FF} and C_{FF} to the pin; the IC does not work properly if the pin is left floating or may be damaged if connected directly to ground.

Figure 32. R_{FF}·C_{FF} as a function of 3rd harmonic distortion introduced in the input current



9 Soft-start

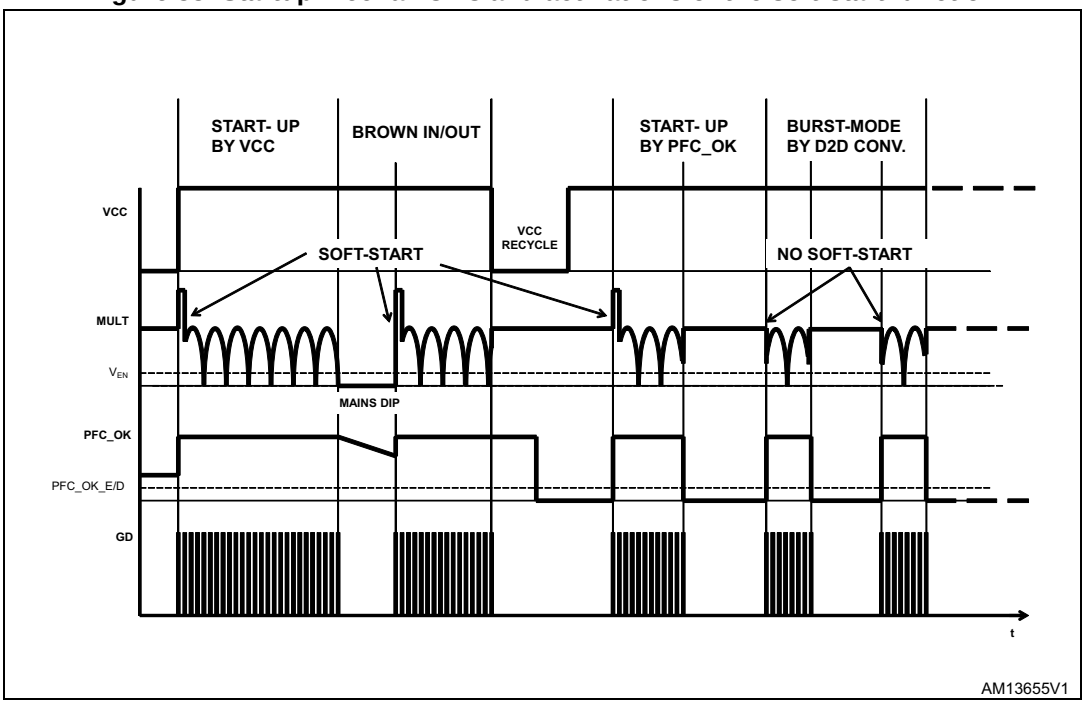
To reduce inrush energy at startup or after an auto-restart protection tripping, the L4984D uses soft-start. Please refer to *Table* in *Section 12: Power management and housekeeping functions* for more details of the events triggering soft-start.

The function is performed by internally pulling the voltage on the MULT pin towards an asymptotic level located at about 4.1 V as the device wakes up. This has a twofold effect: on the one hand, the output of the multiplier is lowered through the voltage feedforward function, therefore programming a lower peak current; on the other hand, the off-time of the power switch is considerably prolonged with respect to the normal values programmed by the capacitor connected to the TIMER pin. In this way, both the current inrush and the risk of saturating the boost inductor at startup are minimized.

After 300 µs from its activation, the pull-up is released. The voltage on the MULT pin decays with the time constant determined by the resistor divider that biases the pin and the bypass capacitor typically connected between the pin and ground to reduce noise pick-up. At the same time, C_{FF} is discharged by turning on the internal low impedance discharge switch (see *Section 8: Voltage feedforward*).

The soft-start function is performed at turn-on by VCC Turn-on threshold (V_{CCOn}), by the brownout function and at startup by PFC_OK. On the following activations by PFC_OK (like during burst-mode operation driven by a D2D converter controller) the soft-start function is not performed. *Figure 33* shows the different startup mechanisms and the activations of the soft-start function.

Figure 33. Startup mechanisms and activations of the soft-start function



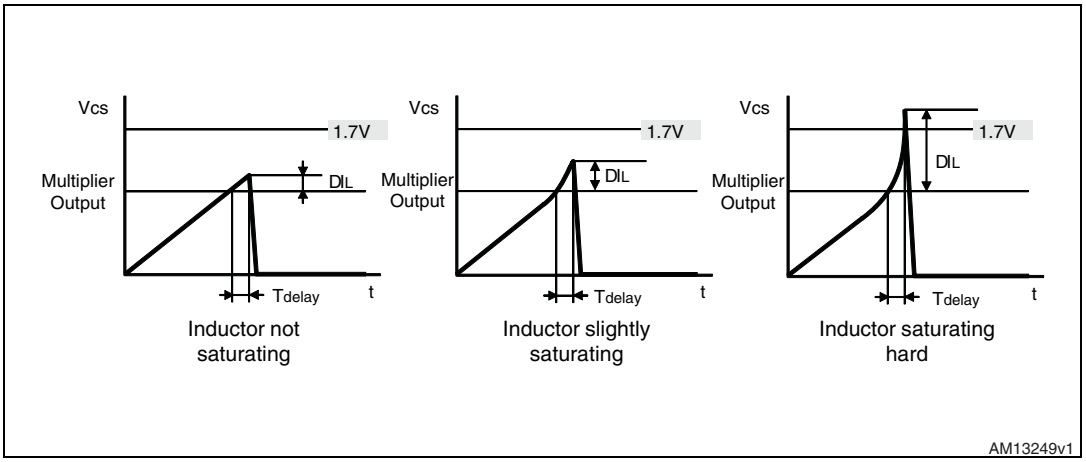
10 Inductor saturation detection

Boost inductor hard saturation may be a fatal event for a PFC pre-regulator: the current upslope becomes so large (50-100 times steeper, see *Figure 34*) that, during the current sense propagation delay, the current may reach abnormally high values. The voltage drop caused by this abnormal current on the sense resistor reduces the gate-to-source voltage, so that the MOSFET may work in the active region and dissipate a huge amount of power, which leads to a catastrophic failure after few switching cycles.

However, even a well-designed boost inductor may occasionally saturate when the boost stage recovers after a missing line cycle. This happens when the restart occurs at an unfavorable line voltage phase, i.e. when the output voltage is lower than the rectified input voltage as this reappears. As a result, in the boost inductor the inrush current coming from the bridge rectifier and going to the output capacitor adds up to the switched current. Furthermore, there is little or no voltage available for demagnetization.

To cope with a saturated inductor, the L4984D is provided with a second comparator on the current sense pin (CS, pin 4) that stops the IC if the voltage, normally limited within 0.88 V, exceeds 1.7 V. After that, the IC is restarted by the internal starter circuitry; the starter repetition time is low enough (300 µs typ.) to guarantee low stress for the inductor, the Power MOSFET and the boost diode.

Figure 34. Effect of boost inductor saturation on MOSFET current and detection method



11 THD optimizer circuit

The L4984D is provided with a special circuit that reduces the conduction dead-angle occurring at the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (total harmonic distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This results in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge.

Figure 35. THD optimizer circuit

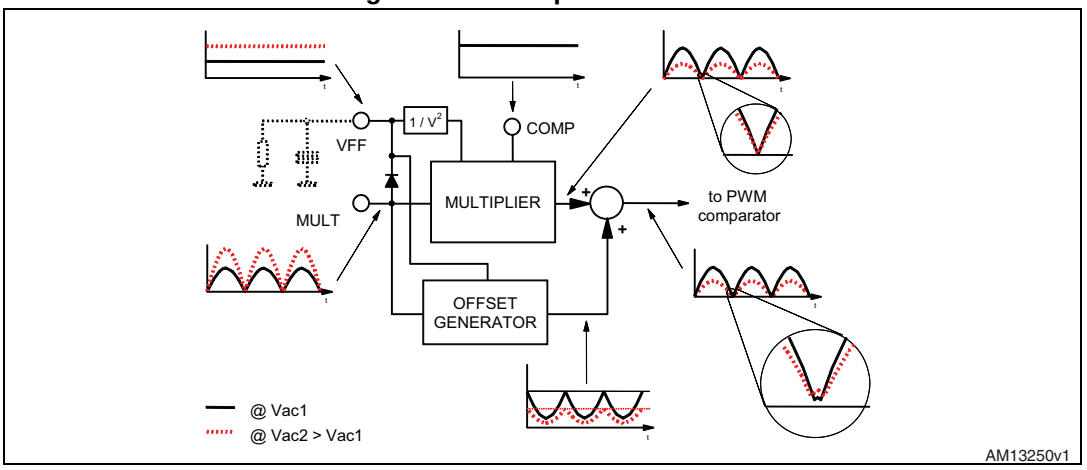


Figure 36. HD optimization: standard PFC controller

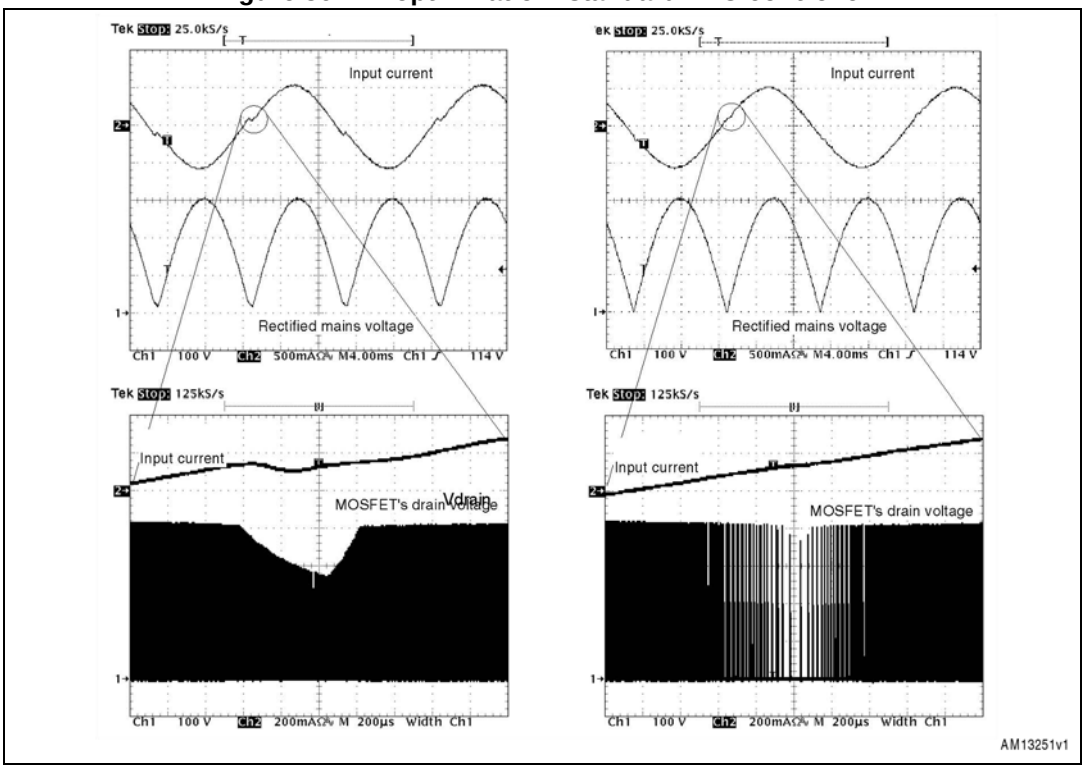


Figure 35 shows the internal block diagram of the THD optimizer circuit.

To take maximum benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current - even with an ideal energy transfer by the PFC pre-regulator - therefore reducing the effectiveness of the optimizer circuit.

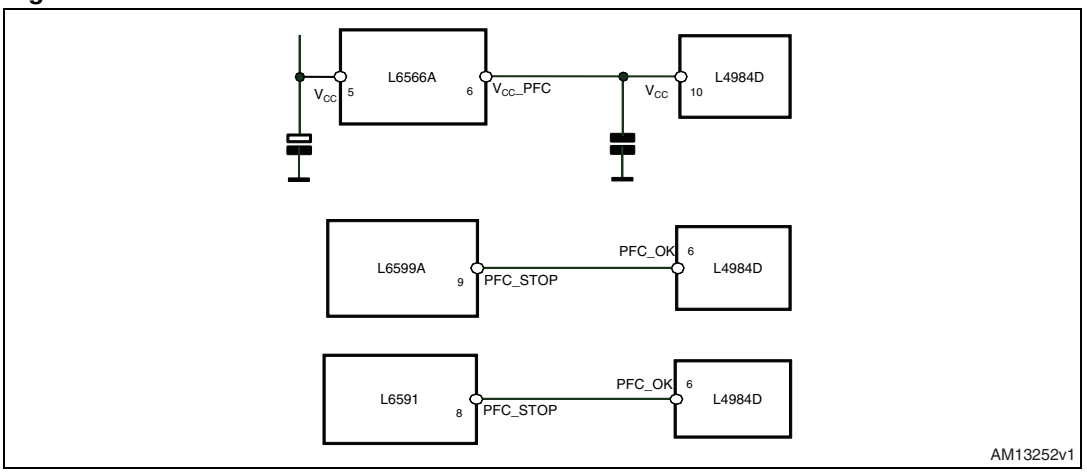
Essentially, the circuit artificially increases the on-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore, the offset is modulated by the voltage on the VFF pin (see *Section 8: Voltage feedforward*) so as to have little offset at low line, where energy transfer at zero-crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse.

The effect of the circuit is shown in *Figure 36*, where the key waveforms of a standard PFC controller are compared to those of this chip. Note the significant reduction in the region around the zero-crossing where the drain voltage cannot reach the output voltage and how switching frequency drops dramatically near the zero-crossing.

12 Power management and housekeeping functions

A communication line with the control IC of the cascaded DC-DC converter can be established via the disable function included in the PFC_OK pin (see *Section 7: Feedback failure detection (FFD)* for more details). Typically this line is used to allow the PWM controller of the cascaded DC-DC converter to shut down the L4984D in case of light load and to minimize the no-load input consumption. Should the residual consumption of the chip be an issue, it is also possible to cut down the supply voltage. Interface circuits like those are shown in *Figure 37*. Needless to say, this operation assumes that the cascaded DC-DC converter stage works as the master and the PFC stage as the slave or, in other words, that the DC-DC stage starts first; it powers both controllers and enables/disables the operation of the PFC stage.

Figure 37. Interface circuits that let DC-DC converter controller IC disable the L4984D



Another available function is brownout protection, which is basically a not-latched shutdown function that is activated when a condition of mains undervoltage is detected. This condition may cause overheating of the primary power section due to an excess of RMS current. Brownout can also cause the PFC pre-regulator to work in open loop, which may be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power-down and that cause the output voltage of the converter to not decay to zero monotonically. For these reasons it is usually preferable to shut down the unit in the case of brownout. The brownout threshold is internally fixed at 0.8 V and is sensed on the VFF pin while the voltage is falling. An 80 mV hysteresis prevents rebounding at input voltage turn-off.

The soft-start function is performed by PFC_OK enable threshold ($V_{PFC\_OK\_E}$) only at startup, but not on the following activations, to ensure a proper burst-mode operation (as described in *Figure 33*). For this reason pin MULT is suggested to be used as remote ON/OFF control.

In *Table 6* it is possible to find a summary of all of the above mentioned working conditions that cause the device to stop operating.

Table 6. Summary of L4984D idle states

Condition	Caused or revealed by	IC behavior	Restart condition	Typical IC consumption	SS activation
UVLO	$V_{CC} < V_{CCOff}$	Disabled	$V_{CC} > V_{CCOn}$	65 µA	Yes
Standby	$V_{PFC\_OK} < V_{PFC\_OK\_D}$	Stop switching	$V_{PFC\_OK} > V_{PFC\_OK\_E}$	1.5 mA	No
AC brownout	$V_{VFF} < V_{DIS}$	Stop switching	$V_{VFF} > V_{EN}$	1.5 mA	Yes
OVP	$V_{PFC\_OK} > V_{PFC\_OK\_S}$	Stop switching	$V_{PFC\_OK} < V_{PFC\_OK\_R}$	2.2 mA	No
Feedback failure	$V_{PFC\_OK} > V_{PFC\_OK\_S}$ AND $V_{INV} < 1.66$ V	Latched-off	$V_{CC} < V_{CCrestart}$ then $V_{CC} > V_{CCOn}$	180 µA	Yes
Low consumption	$V_{COMP} < 2.4$ V	Burst mode	$V_{COMP} > 2.4$ V	1.8 mA	No
Saturated boost inductor	$Vcs > V_{CS\_th}$	Stop switching	Auto restart after 300 ìs	4 mA	No

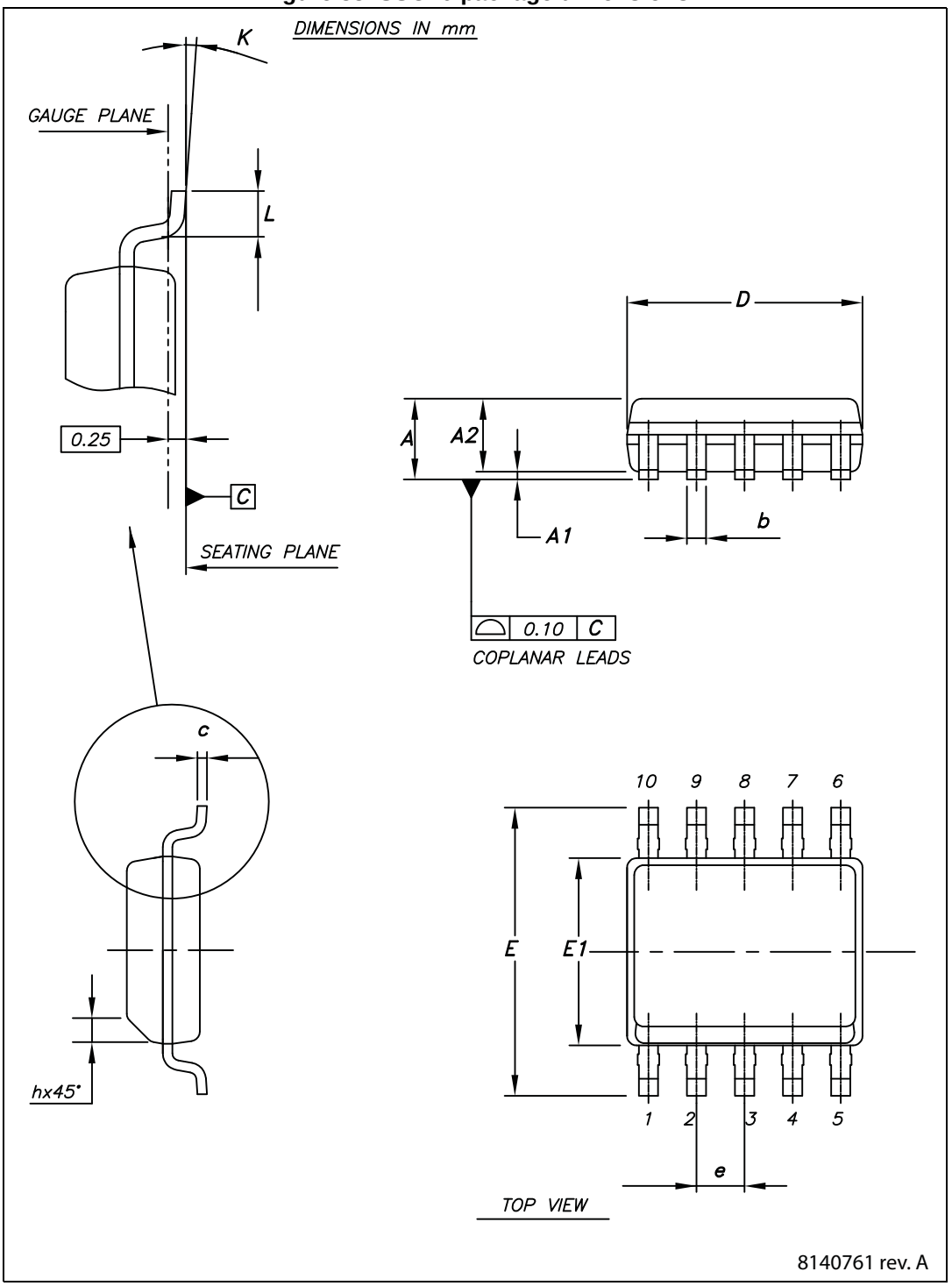
13 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 7. SSO10 mechanical data

Dim	Databook (mm)		
	Typ	Min	Max
A			1.75
A1		0.10	0.25
A2		1.25	
b		0.31	0.51
c		0.17	0.25
D	4.90	4.80	5
E	6	5.80	6.20
E1	3.90	3.80	4
e	1		
h		0.25	0.50
L		0.40	0.90
K		0°	8°

Figure 38. SSO10 package dimensions



14 Revision history

Table 8. Document revision history

Date	Revision	Changes
15-Apr-2013	1	Initial release.