OV7725 Color CMOS VGA (640x480) CAMERACHIP™ Sensor with OmniPixel2™ Technology

General Description

The OV7725 CAMERACHIP™ image sensor is a low voltage CMOS device that provides the full functionality of a single-chip VGA camera and image processor in a small footprint package. The OV7725 provides full-frame, sub-sampled or windowed 8-bit/10-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This device has an image array capable of operating at up to 60 frames per second (fps) in VGA with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface. In addition, OmniVision sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, blooming, etc., to produce a clean, fully stable color image.

Note: The OV7725 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Standard SCCB interface
- Output support for Raw RGB, RGB (GRB 4:2:2, RGB565/555/444) and YCbCr (4:2:2) formats
- Supports image sizes: VGA, QVGA, and any size scaling down from CIF to 40x30
- VarioPixel® method for sub-sampling
- Automatic image control functions including: Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Band Filter (ABF), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), and anti-blooming
- ISP includes noise reduction and defect correction
- Lens shading correction
- Saturation level auto adjust (UV adjust)
- Edge enhancement level auto adjust
- De-noise level auto adjust
- Frame synchronization capability

Ordering Information

Product	Package
OV07725-VL1A (Color, lead-free)	28-pin CSP2

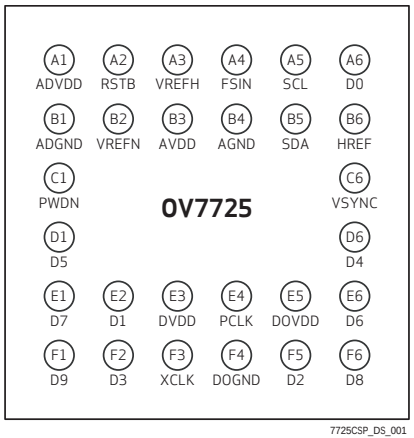
Applications

- Cellular and picture phones
- Toys
- PC Multimedia
- Digital still cameras

Key Specifications

Array Size		640 x 480
Power Supply	**Digital Core**	1.8VDC ± 10%
	Analog	3.0V to 3.6V
	I/O	1.7V to 3.3V
Power Requirements	**Active**	120 mW typical (60 fps VGA, YUV)
	Standby	< 20 µA
Temperature Range		-20°C to +70°C
Output Format	**8-bit**	• YUV/YCbCr 4:2:2 • RGB565/555/444 • GRB 4:2:2 • Raw RGB Data
	10-bit	• Raw RGB Data
Lens Size		1/4"
Lens Chief Ray Angle		25° non linear
Max Image Transfer Rate		60 fps for VGA
Sensitivity		3.8 V/(Lux • sec)
S/N Ratio		50 dB
Dynamic Range		60 dB
Scan Mode		Progressive
Electronic Exposure		Up to 510:1 (for selected fps)
Pixel Size		6.0 µm x 6.0 µm
Dark Current		40 mV/s
Well Capacity		26 Ke^-
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		3984 µm x 2952 µm
Package Dimensions		5345 µm x 5265 µm

Figure 1 OV7725 Pinout (Top View)



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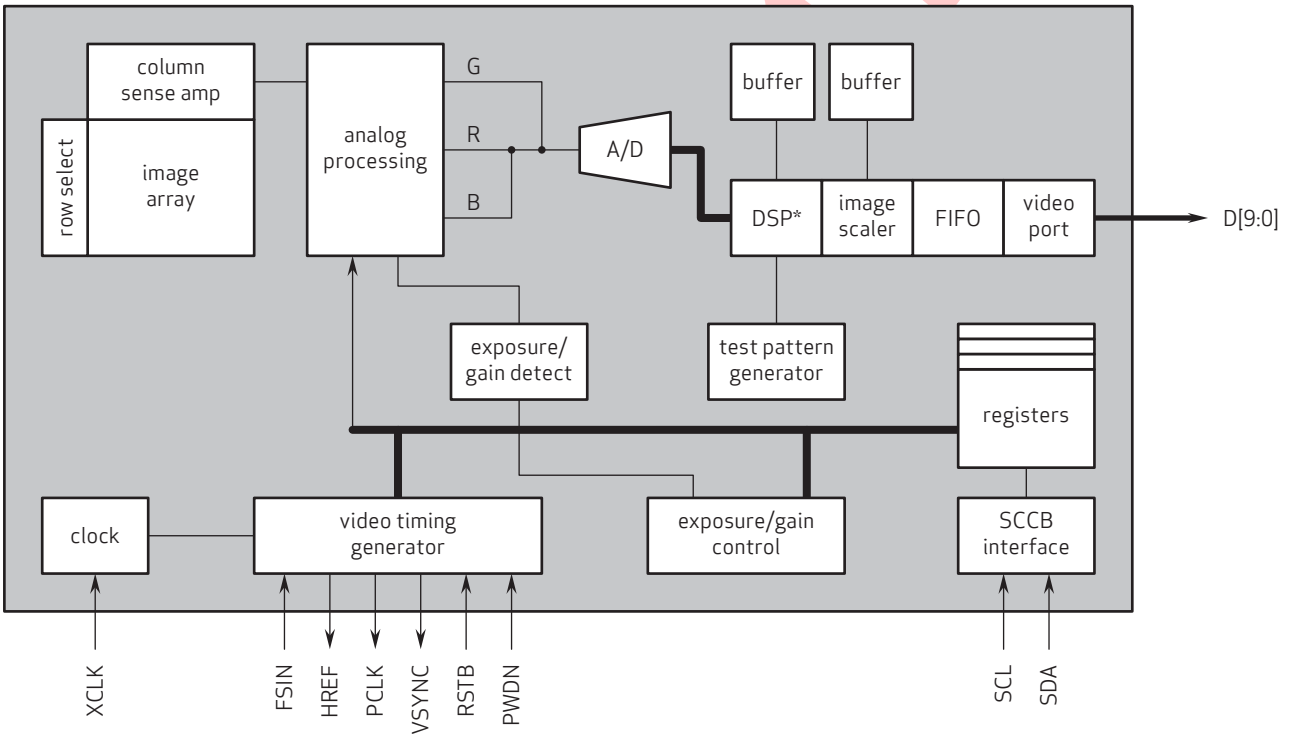
Functional Description

Figure 2 shows the functional block diagram of the OV7725 image sensor. The OV7725 includes:

- Image Sensor Array (total array of 656 x 488 pixels, with active pixels 640 x 480 in YUV mode)
- Analog Signal Processor
- A/D Converters
- Test Pattern Generator
- Digital Signal Processor (DSP)
- Image Scaler
- Timing Generator
- Digital Video Port
- SCCB Interface

Figure 2 Functional Block Diagram



note 1 DSP* (lens shading correction, de-noise, white/black pixel correction, auto white balance, etc.)

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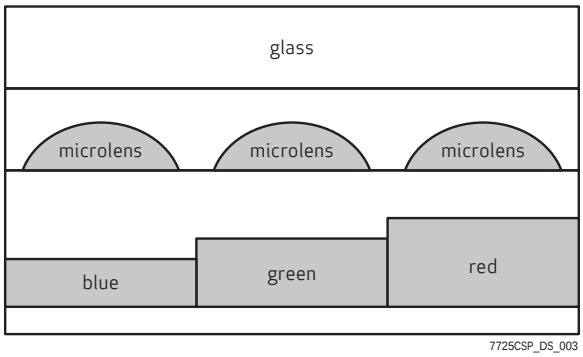
Image Sensor Array

The OV7725 sensor has an image array of 664 x 490 pixels for a total of 325,360 pixels, of which 640 x 480 pixels are active (307,200 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)

A/D Converters

After the Analog Processing block, the bayer pattern Raw signal is fed to a 10-bit analog-to-digital (A/D) converter shared by G and BR channels. This A/D converter operates at speeds up to 12 MHz and is fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Test Pattern Generator

The Test Pattern Generator features the following:

- 8-bar color bar pattern
- Shift "1" in output pin

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit

Image Scaler

This block controls all output and data formatting required prior to sending the image out. This block scales YUV/RGB output from VGA to CIF and almost any size under CIF.

Digital Video Port

Register bits COM2[1:0] increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP sensor operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Number	Name	Pin Type	Function/Description
A1	ADVDD	Power	ADC power supply
A2	RSTB	Input	System reset input, active low
A3	VREFH	Reference	Reference voltage - connect to ground using a 0.1 µF capacitor
A4	FSIN	Input (0)[b]	Frame synchronize input
A5	SCL	Input	SCCB serial interface clock input
A6	D0[a]	Output	Data output bit[0]
B1	ADGND	Power	ADC ground
B2	VREFN	Reference	Reference voltage - connect to ground using a 0.1 µF capacitor
B3	AVDD	Power	Analog power supply
B4	AGND	Power	Analog ground
B5	SDA	I/O	SCCB serial interface data I/O
B6	HREF	Output	HREF output
C1	PWDN	Input (0)[b]	Power Down Mode Selection 0: Normal mode 1: Power down mode
C6	VSYNC	Output	Vertical sync output
D1	D5	Output	Data output bit[5]
D6	D4	Output	Data output bit[4]
E1	D7	Output	Data output bit[7]
E2	D1	Output	Data output bit[1]
E3	DVDD	Power	Power supply (1.8 VDC) for digital logic core
E4	PCLK	Output	Pixel clock output
E5	DOVDD	Power	Digital power supply for I/O (1.7V ~ 3.3V)
E6	D6	Output	Data output bit[6]
F1	D9[c]	Output	Data output bit[9]
F2	D3	Output	Data output bit[3]
F3	XCLK	Input	System clock input
F4	DOGND	Power	Digital ground
F5	D2	Output	Data output bit[2]
F6	D8	Output	Data output bit[8]

a. D[9:0] for 10-bit Raw RGB data (MSB: D9; LSB: D0)

b. Input (0) represents an internal pull-down resistor and should be grounded when not used.

c. D[9:2] for 8-bit YUV or RGB565/RGB555 (MSB: D9; LSB: D2)

Electrical Characteristics

Table 2 Operating Conditions

Parameter	Min	Max
Operating temperature	-20°C	+70°C
Storage temperature[a]	-40°C	+125°C

a. Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the sensor at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.

Table 3 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-C}	3 V
	V_{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+0.5V
Lead-free Temperature, Surface-mount process		245ºC

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 4 DC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – analog	–	3.0	3.3	3.6	V
V_{DD-C}	DC supply voltage – digital core	See Note [a]	1.62	1.8	1.98	V
V_{DD-IO}	DC supply voltage – I/O	See Note [a]	1.7	–	3.3	V
I_{DDA}	Active (operating) current	See Note [b]		10 + 19[c]		mA
$I_{DDS-SCCB}$	Standby current	See Note [d]		1		mA
$I_{DDS-PWDN}$	Standby current			10	20	µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.2 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [e]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-IO} should not be lower than 2.45V when using the internal regulator for V_{DD-C} (1.8V). When not using the internal regulator, V_{DD-C} requires external 1.8V power that must not be higher than V_{DD-IO}.

b. At 25ºC, V_{DD-A} = 3.3V, V_{DD-C} = 1.8V, V_{DD-IO} = 3.3V
$I_{DDA} = \Sigma\{I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 30 fps YUV output, no I/O loading

c. I_{DD-C} = 10mA, I_{DD-A} = 19mA, without loading

d. At 25ºC, V_{DD-A} = 3.3V, V_{DD-C} = 1.8V, V_{DD-IO} = 3.3V
$I_{DDS-SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to a PWDN pin-initiated Standby

e. Standard Output Loading = 25pF, 1.2KΩ

Table 5 Functional and AC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential non-linearity		± 1/2		LSB
	A/D Integral non-linearity		± 1		LSB
	AGC Range			30	dB
	Red/Blue adjustment range			12	dB
Inputs (PWDN, CLK, RESET#)					
f_{CLK}	Input clock frequency	10	24	48	MHz
t_{CLK}	Input clock period	21	42	100	ns
$t_{CLK:DC}$	Clock duty cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB Timing (see Figure 4)					
f_{SCL}	Clock frequency			400	KHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_{AA}	SCL low to data out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition hold time	600			ns
$t_{SU:STA}$	START condition setup time	600			ns
$t_{HD:DAT}$	Data in hold time	0			µs
$t_{SU:DAT}$	Data in setup time	100			ns
$t_{SU:STO}$	STOP condition setup time	600			ns
t_{R}, t_{F}	SCCB rise/fall times			300	ns
t_{DH}	Data out hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and D[9:0] (see Figure 5, Figure 6, Figure 7, and Figure 8)					
t_{PDV}	PCLK[↓] to data out Valid			5	ns
t_{SU}	D[9:0] setup time	15			ns
t_{HD}	D[9:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-C} = 1.8V, V_{DD-A} = 3.3V, V_{DD-IO} = 3.3V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 3.3V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

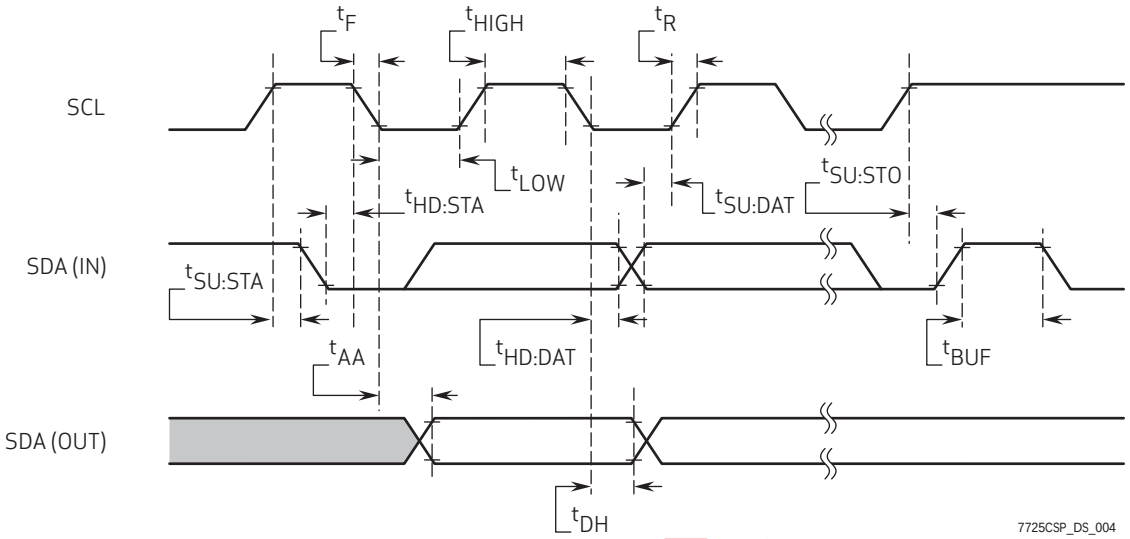


Figure 5 Horizontal Timing

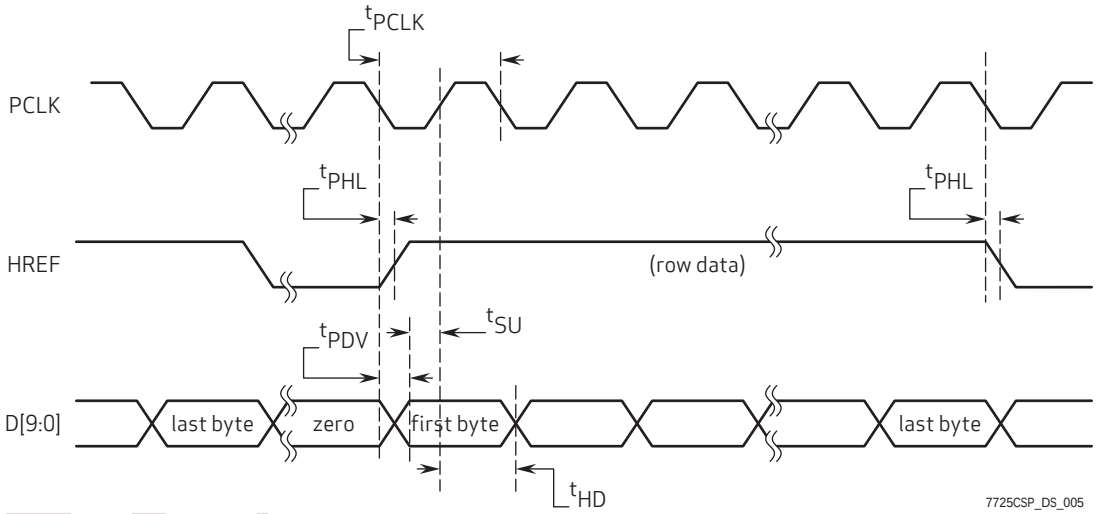
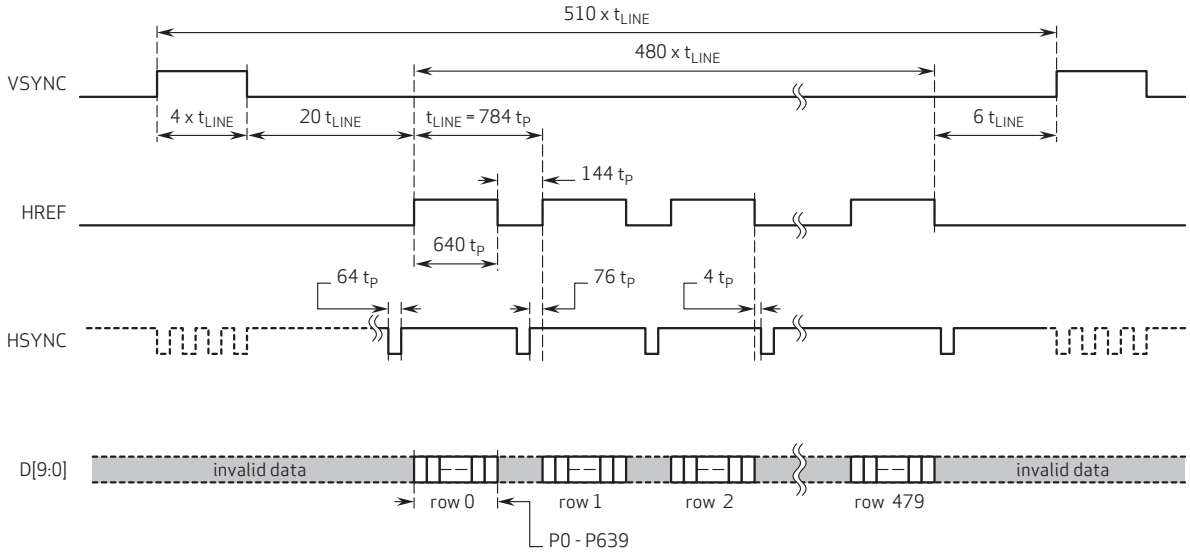


Figure 6 VGA Frame Timing



note 1 for raw data, $t_P = t_{PCLK}$

note 2 for YUV/RGB, $t_P = 2 \times t_{PCLK}$

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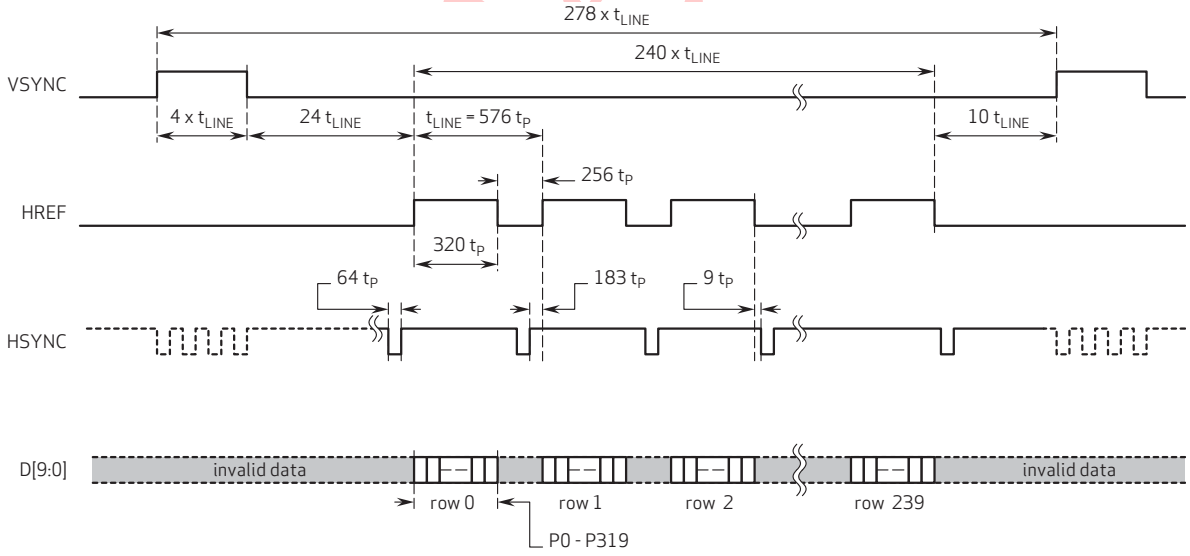
Figure 7 QVGA Frame Timing



note 1 for raw data, $t_P = t_{PCLK}$

note 2 for YUV/RGB, $t_P = 2 \times t_{PCLK}$

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Figure 8 CIF Frame Timing

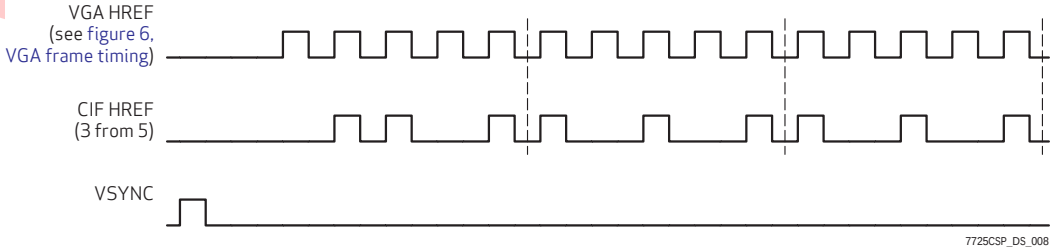

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Figure 9 RGB 565 Output Timing Diagram

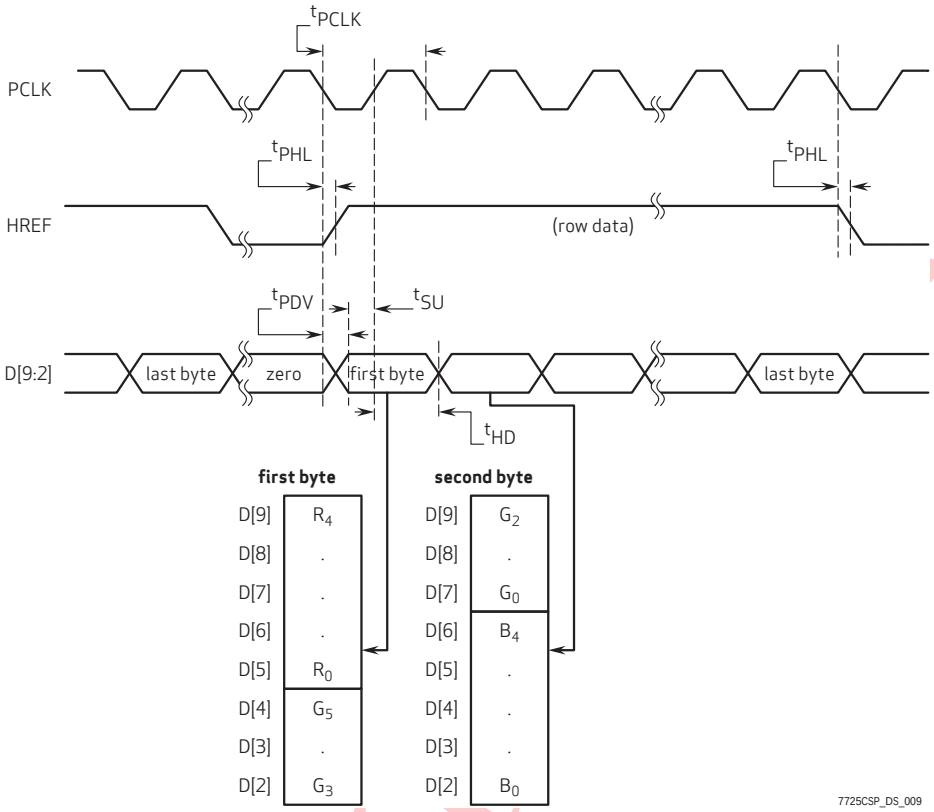


Figure 10 RGB 555 Output Timing Diagram

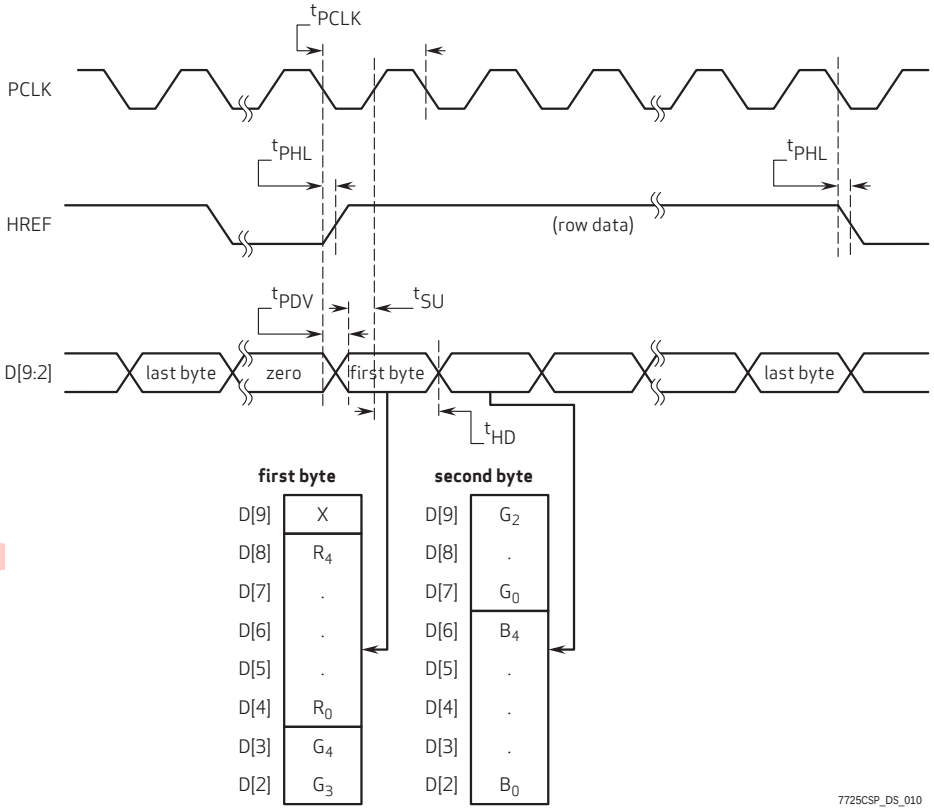
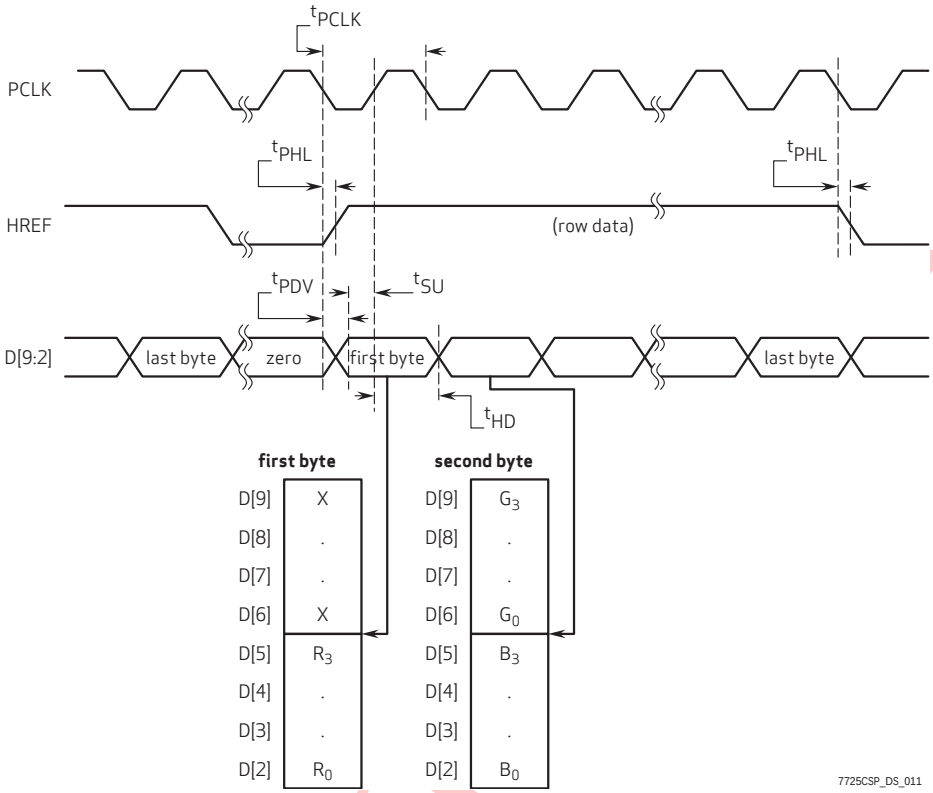


Figure 11 RGB 444 Output Timing Diagram



Register Set

Table 6 provides a list and description of the Device Control registers contained in the OV7725. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x42 for write and 0x43 for read.

Table 6 Device Control Register List (Sheet 1 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting Gain = (GAIN[7] + 1) × (GAIN[6] + 1) × (GAIN[5] + 1) × (GAIN[4] + 1) × (GAIN[3:0] / 16 + 1)
01	BLUE	80	RW	AWB – Blue channel gain setting Blue Gain = BLUE / 0x40 when AWBCtrl1[2] = 1 Blue Gain = BLUE / 0x80 when AWBCtrl1[2] = 0 ***Note:*** *This register should be ≥ 1x.*
02	RED	80	RW	AWB – Red channel gain setting Blue Gain = RED / 0x40 when AWBCtrl1[2] = 1 Blue Gain = RED / 0x80 when AWBCtrl1[2] = 0 ***Note:*** *This register should be ≥ 1x.*
03	GREEN	80	RW	AWB – Green channel gain setting Blue Gain = GREEN / 0x40 when AWBCtrl1[2] = 1 Blue Gain = GREEN / 0x80 when AWBCtrl1[2] = 0 ***Note:*** *This register should be ≥ 1x.*
04	RSVD	XX	–	Reserved
05	BAVG	00	R	B Average Level Automatically updated based on chip output format
06	GAVG	00	R	G Average Level Automatically updated based on chip output format
07	RAVG	00	R	R Average Level Automatically updated based on chip output format
08	AECH	00	RW	Exposure Value – AEC MSBs Bit[7:0]: AEC[15:8] (see register AEC for AEC[7:0]} Automatically updated when AEC is enabled
09	COM2	00	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Soft sleep mode Bit[3:2]: Reserved Bit[1:0]: Output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
0A	PID	77	R	Product ID Number MSB (Read only)
0B	VER	21	R	Product ID Number LSB (Read only)

Table 6 Device Control Register List (Sheet 2 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0C	COM3	10	RW	Common Control 3 Bit[7]: Reserved Bit[6]: Horizontal mirror image ON/OFF selection Bit[5]: Swap B/R output sequence in RGB output mode Bit[4]: Swap Y/UV output sequence in YUV output mode (see register DSP_Ctrl3[7] (0x66)) Bit[3]: Swap output MSB/LSB Bit[2]: Tri-state option for output clock including PCLK, HREF, and VSYNC at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[1]: Tri-state option for output data at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[0]: Sensor color bar test pattern output enable
0D	COM4	41	RW	Common Control 4 Bit[7:6]: PLL frequency control 00: Bypass PLL 01: PLL 4x 10: PLL 6x 11: PLL 8x Bit[5:4]: AEC evaluate window 00: Full window 01: 1/2 window 10: 1/4 window 11: Low 2/3 window Bit[3:0]: Reserved
0E	COM5	79	RW	Common Control 5 Bit[7]: Auto frame rate control ON/OFF selection (night mode) Bit[6]: Auto frame rate control speed selection 0: Normal 1: Fast Bit[5:4]: Auto frame rate max rate control 00: No reduction of frame rate 01: Max reduction to 1/2 frame rate 10: Max reduction to 1/4 frame rate 11: Max reduction to 1/8 frame rate Bit[3:2]: Auto frame rate active point control 00: Not allowed 01: Add frame when AGC reaches 4x gain 10: Add frame when AGC reaches 8x gain 11: Add frame when AGC reaches 16x gain Bit[1:0]: Reserved
0F	COM6	A9	RW	Common Control 6 Bit[7:1]: Reserved Bit[0]: Auto window setting ON/OFF selection when format changes

Table 6 Device Control Register List (Sheet 3 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
10	AEC	00	RW	Exposure Value Bit[7:0]: AEC[7:0] (see register AECH for AEC[15:8]) AEC[15:0] = {AECH[7:0] (0x08), AEC[7:0] (0x10)} $T_{exposure}$ = AEC[15:0] × $T_{row\ interval}$
11	CLKRC	00	RW	Internal Clock Bit[7]: Reserved Bit[6]: Use external clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar $f_{internal\ clock}$ = $f_{input\ clock}$ × PLL multiplier / [(CLKRC[5:0] + 1) × 2]
12	COM7	00	RW	Common Control 7 Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: Resolution selection 0: VGA 1: QVGA Bit[5]: BT.656 protocol ON/OFF selection Bit[4]: Sensor RAW Bit[3:2]: RGB output format control 00: GBR4:2:2 01: RGB565 10: RGB555 11: RGB444 Bit[1:0]: Output format control 00: YUV 01: Processed Bayer RAW 10: RGB 11: Bayer RAW

Table 6 Device Control Register List (Sheet 4 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COM8	CF	RW	Common Control 8 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - Step size limit 0: Step size is limited to vertical blank 1: Unlimited step size Bit[5]: Banding filter ON/OFF Bit[4]: Enable AEC below banding value 0: Limit the minimum exposure time to 1/100 or 1/120 second under any lighting conditions when the banding filter is enabled 1: Allow exposure time to be less than 1/100 or 1/120 second under strong lighting conditions when the banding filter is enabled Bit[3]: Fine AEC ON/OFF control 0: Limit the minimum exposure time to 1 row 1: Allow exposure time to be less than 1 row Bit[2]: AGC Enable 0: Manual mode 1: Auto mode Bit[1]: AWB Enable 0: Manual mode 1: Auto mode Bit[0]: AEC Enable 0: Manual mode 1: Auto mode
14	COM9	40	RW	Common Control 9 Bit[7]: Histogram or average based AEC/AGC selection Bit[6:4]: Automatic Gain Ceiling - maximum AGC value 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101 Not allowed 110: Not allowed 111: Not allowed Bit[3]: Reserved Bit[2]: Drop VSYNC output of corrupt frame Bit[1]: Drop HREF output of corrupt frame Bit[0]: Reserved

Table 6 Device Control Register List (Sheet 5 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COM10	00	RW	Common Control 10 Bit[7]: Output negative data Bit[6]: HREF changes to HSYNC Bit[5]: PCLK output option 0: Free running PCLK 1: PCLK does not toggle during horizontal blank Bit[4]: PCLK reverse Bit[3]: HREF reverse Bit[2]: Reserved Bit[1]: VSYNC negative Bit[0]: Output data range selection 0: Full range 1: Data from [10] to [F0] (8 MSBs)
16	REG16	00	RW	Register 16 Bit[7]: Bit shift test pattern options - should set to 1 for bit shift test pattern Bit[6:0]: Reserved
17	HSTART	26 (VGA) 3F (QVGA)	RW	Horizontal Frame (HREF column) Start 8 MSBs HStart = {HSTART[7:0] (0x17), HREF[5:4] (0x32)}
18	HSIZE	A0 (VGA) 50 (QVGA)	RW	Horizontal Sensor Size HSize = {HSIZE[7:0] (0x18), HREF[1:0] (0x32)}
19	VSTRT	07 (VGA) 03 (QVGA)	RW	Vertical Frame (row) Start 8 MSBs VStart = {VSTRT[7:0] (0x19), HREF[6] (0x32)}
1A	VSIZE	F0 (VGA) 78 (QVGA)	RW	Vertical Sensor Size VSize = {VSIZE[7:0] (0x1A), HREF[2] (0x32)}
1B	PSHFT	40	RW	Data Format - Pixel Delay Select (delays timing of the D[9:0] data relative to HREF in pixel units) • Range: [00] (no delay) to [FF] (256 pixel delay which accounts for whole array)
1C	MIDH	7F	R	Manufacturer ID Byte – High
1D	MIDL	A2	R	Manufacturer ID Byte – Low
1E	RSVD	XX	–	Reserved
1F	LAEC	00	RW	Fine AEC Value - defines exposure value less than one row period
20	COM11	10	RW	Common Control 11 Bit[7:2]: Reserved Bit[1]: Single frame ON/OFF selection Bit[0]: Single frame transfer trigger
21	RSVD	XX	–	Reserved
22	BDBase	FF	RW	Banding Filter Minimum AEC Value
23	BDMStep	01	RW	Banding Filter Maximum Step

Table 6 Device Control Register List (Sheet 6 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
24	AEW	58	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	AEB	48	RW	AGC/AEC - Stable Operating Region (Lower Limit)
26	VPT	C3	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: High nibble of upper limit of fast mode control zone Bit[3:0]: High nibble of lower limit of fast mode control zone
27	RSVD	XX	–	Reserved
28	REG28	00	RW	Register 28 Bit[7:1]: Reserved Bit[0]: Selection on the number of dummy rows
29	HOutSize	A0 (VGA) 50 (QVGA)	RW	Horizontal Data Output Size 8 MSBs H Output Size = {HOutSize[7:0] (0x29), EXHCH[1:0] (0x2A)}
2A	EXHCH	00	RW	Dummy Pixel Insert MSB Bit[7:4]: 4 MSBs for dummy pixel insert in horizontal direction Bit[3]: Reserved Bit[2]: Vertical data output size LSB Bit[1:0]: Horizontal data output size 2 LSBs
2B	EXHCL	00	RW	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction
2C	VOutSize	F0 (VGA) 78 (QVGA)	RW	Vertical Data Output Size MSBs V Output Size = {VOutSize[7:0] (0x2C), EXHCH[2] (0x2A)}
2D	ADVFL	00	RW	LSB of Insert Dummy Rows in Vertical Sync (1 bit equals 1 row)
2E	ADVFH	00	RW	MSB of Insert Dummy Rows in Vertical Sync
2F	YAVE	00	R	Y/G Channel Average Value
30	LumHTh	80	RW	Histogram AEC/AGC Luminance High Level Threshold
31	LumLTh	60	RW	Histogram AEC/AGC Luminance Low Level Threshold
32	HREF	00	RW	Image Start and Size Control Bit[7]: Mirror image edge alignment - should set to 1 in mirror mode Bit[6]: Vertical HREF window start control LSB Bit[5:4]: Horizontal HREF window start control LSBs Bit[3]: Data output bit shift test pattern ON/OFF control Bit[2]: Vertical sensor size LSB Bit[1:0]: Horizontal sensor size 2 LSBs
33	DM_LNL	00	RW	Low 8 Bits of the Number of Dummy Rows
34	DM_LNH	00	RW	High 8 Bits of the Number of Dummy Rows
35	ADoff_B	80	RW	AD Offset Compensation Value for B Channel
36	ADoff_R	80	RW	AD Offset Compensation Value for R Channel
37	ADoff_Gb	80	RW	AD Offset Compensation Value for Gb Channel

Table 6 Device Control Register List (Sheet 7 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
38	ADoff_Gr	80	RW	AD Offset Compensation Value for Gr Channel
39	Off_B	80	RW	B Channel Offset Compensation Value
3A	Off_R	80	RW	R Channel Offset Compensation Value
3B	Off_Gb	80	RW	Gb Channel Offset Compensation Value
3C	Off_Gr	80	RW	Gr Channel Offset Compensation Value
3D	COM12	80	RW	Common Control 12 Bit[7:6]: Reserved Bit[5:0]: DC offset for analog process
3E	COM13	E2	RW	Common Control 13 Bit[7]: BLC enable Bit[6]: ADC channel BLC ON/OFF control Bit[5]: Analog processing channel BLC ON/OFF control Bit[4:3]: Reserved Bit[2]: ABLC gain trigger enable Bit[1:0]: Reserved
3F	COM14	1F	RW	Edge Enhancement Adjustment Bit[7:4]: Reserved Bit[3:2]: AD offset compensation option x0: Use R/Gr channel value for B/Gb 01: Use B/Gb channel value for R/Gr 11: Use B/Gb/R/Gr channel value independently Bit[1:0]: Analog processing offset compensation option x0: Use R/Gr channel value for B/Gb 01: Use B/Gb channel value for R/Gr 11: Use B/Gb/R/Gr channel value independently
40	RSVD	XX	–	Reserved
41	COM16	00	RW	Common Control 16 Bit[7:0]: Reserved
42	TGT_B	80	RW	BLC Blue Channel Target Value Register value = 0x80 + Black level target value
43	TGT_R	80	RW	BLC Red Channel Target Value Register value = 0x80 + Black level target value
44	TGT_Gb	80	RW	BLC Gb Channel Target Value Register value = 0x80 + Black level target value
45	TGT_Gr	80	RW	BLC Gr Channel Target Value Register value = 0x80 + Black level target value

Table 6 Device Control Register List (Sheet 8 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
46	LC_CTR	00	RW	Lens Correction Control Bit[7:3]: Reserved Bit[2]: Lens correction control select 0: R, G, and B channel compensation coefficient is set by registers LC_COEF (0x49) 1: R, G, and B channel compensation coefficient is set by registers LC_COEFB (0x4B), LC_COEF (0x49), and LC_COEFR (0x4C), respectively Bit[1]: Reserved Bit[0]: Lens correction enable 0: Disable 1: Enable
47	LC_XC	00	RW	X Coordinate of Lens Correction Center Relative to Array Center Bit[7]: Sign bit 0: Positive 1: Negative Bit[6:0]: X coordinate of lens correction center relative to array center
48	LC_YC	00	RW	Y Coordinate of Lens Correction Center Relative to Array Center Bit[7]: Sign bit 0: Positive 1: Negative Bit[6:0]: Y coordinate of lens correction center relative to array center
49	LC_COEF	50	RW	Lens Correction Coefficient G channel compensation coefficient when LC_CTR[2] (0x46) is 1 R, G, and B channel compensation coefficient when LC_CTR[2] is 0
4A	LC_RADI	30	RW	Lens Correction Radius – radius of the circular section where no compensation applies
4B	LC_COEFB	50	RW	Lens Correction B Channel Compensation Coefficient (effective only when LC_CTR[2] is high)
4C	LC_COEFR	50	RW	Lens Correction R Channel Compensation Coefficient (effective only when LC_CTR[2] is high)

Table 6 Device Control Register List (Sheet 9 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
4D	FixGain	00	RW	Analog Fix Gain Amplifier Bit[7:6]: Gb channel fixed gain 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[5:4]: Gr channel fixed gain 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[3:2]: B channel fixed gain 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[1:0]: R channel fixed gain 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x
4E	RSVD	XX	–	Reserved
4F	AREF1	10	RW	Sensor Reference Current Control Bit[7:4]: Reserved Bit[3]: Internal regulator bypass selection 0: Enable 1: Bypass Bit[2:0]: Reserved
50-53	RSVD	XX	–	Reserved
54	AREF6	7A	RW	Analog Reference Control Bit[7]: Internal power supply control for power down mode - should be set to 0 when internal regulator is used 0: Enable 1: Bypass Bit[6:0]: Reserved
55-5F	RSVD	XX	–	Reserved
60	UFix	00	RW	U Channel Fixed Value Output
61	VFix	05	RW	V Channel Fixed Value Output
62	AWBb_blk	FF	RW	AWB Option for Advanced AWB
63	AWB_Ctrl0	F0	RW	AWB Control Byte 0 Bit[7]: AWB gain enable Bit[6]: AWB calculate enable Bit[5:0]: Reserved

Table 6 Device Control Register List (Sheet 10 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
64	DSP_Ctrl1	BF	RW	DSP Control Byte 1 Bit[7]: FIFO enable/disable selection Bit[6]: UV adjust function ON/OFF selection Bit[5]: SDE enable Bit[4]: Color matrix ON/OFF selection Bit[3]: Interpolation ON/OFF selection Bit[2]: Gamma function ON/OFF selection Bit[1]: Black defect pixel auto correction ON/OFF Bit[0]: White defect pixel auto correction ON/OFF
65	DSP_Ctrl2	00	RW	DSP Control Byte 2 Bit[7:4]: Reserved Bit[3]: Vertical DCW enable Bit[2]: Horizontal DCW enable Bit[1]: Vertical zoom out enable Bit[0]: Horizontal zoom out enable
66	DSP_Ctrl3	10	RW	DSP Control Byte 3 Bit[7]: UV swap (works with register COM3[4] (0x0C)) {COM3[4], DSP_Ctrl3[7]} 00: Y0U0, Y1V1, Y2U2, Y3V3, ... 01: Y0V0, Y1U1, Y2V2, Y3U3, ... 10: U0Y0, V1Y1, U2Y2, V3Y3, ... 11: V0Y0, U1Y1, V2Y2, U3Y3, ... Bit[6]: Reserved Bit[5]: DSP color bar ON/OFF selection Bit[4:0]: Reserved
67	DSP_Ctrl4	00	RW	DSP Control Byte 4 Bit[7:3]: Reserved Bit[2]: AEC reference point selection 0: Before gamma 1: After gamma Bit[1:0]: Output selection 00: YUV or RGB 01: YUV or RGB 10: RAW8 11: RAW10
68	AWB_bias	00	RW	AWB BLC Level Clip
69	AWBCtrl1	5C	RW	AWB Control 1 Bit[7:4]: Reserved Bit[3]: G gain enable 0: AWB adjusts R and G gain only 1: AWB adjusts R, G, and B gain Bit[2]: Max color gain 0: Max color gain is 2x 1: Max color gain is 4x Bit[1:0]: Reserved

Table 6 Device Control Register List (Sheet 11 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
6A	AWBCtrl2	11	RW	AWB Control 2
6B	AWBCtrl3	A2	RW	AWB Control 3 Bit[7]: AWB mode select 0: Advanced AWB 1: Simple AWB
6C	AWBCtrl4	01	RW	AWB Control 4
6D	AWBCtrl5	50	RW	AWB Control 5
6E	AWBCtrl6	80	RW	AWB Control 6
6F	AWBCtrl7	80	RW	AWB Control 7
70	AWBCtrl8	0F	RW	AWB Control 8
71	AWBCtrl9	00	RW	AWB Control 9
72	AWBCtrl10	00	RW	AWB Control 10
73	AWBCtrl11	0F	RW	AWB Control 11
74	AWBCtrl12	0F	RW	AWB Control 12
75	AWBCtrl13	FF	RW	AWB Control 13
76	AWBCtrl14	00	RW	AWB Control 14
77	AWBCtrl15	10	RW	AWB Control 15
78	AWBCtrl16	10	RW	AWB Control 16
79	AWBCtrl17	70	RW	AWB Control 17
7A	AWBCtrl18	70	RW	AWB Control 18
7B	AWBCtrl19	F0	RW	AWB R Gain Range
7C	AWBCtrl20	F0	RW	AWB G Gain Range
7D	AWBCtrl21	F0	RW	AWB B Gain Range
7E	GAM1	0E	RW	Gamma Curve 1st Segment Input End Point 0x04 Output Value
7F	GAM2	1A	RW	Gamma Curve 2nd Segment Input End Point 0x08 Output Value
80	GAM3	31	RW	Gamma Curve 3rd Segment Input End Point 0x10 Output Value
81	GAM4	5A	RW	Gamma Curve 4th Segment Input End Point 0x20 Output Value
82	GAM5	69	RW	Gamma Curve 5th Segment Input End Point 0x28 Output Value
83	GAM6	75	RW	Gamma Curve 6th Segment Input End Point 0x30 Output Value
84	GAM7	7E	RW	Gamma Curve 7th Segment Input End Point 0x38 Output Value
85	GAM8	88	RW	Gamma Curve 8th Segment Input End Point 0x40 Output Value
86	GAM9	8F	RW	Gamma Curve 9th Segment Input End Point 0x48 Output Value
87	GAM10	96	RW	Gamma Curve 10th Segment Input End Point 0x50 Output Value

Table 6 Device Control Register List (Sheet 12 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
88	GAM11	A3	RW	Gamma Curve 11th Segment Input End Point 0x60 Output Value
89	GAM12	AF	RW	Gamma Curve 12th Segment Input End Point 0x70 Output Value
8A	GAM13	C4	RW	Gamma Curve 13th Segment Input End Point 0x90 Output Value
8B	GAM14	D7	RW	Gamma Curve 14th Segment Input End Point 0xB0 Output Value
8C	GAM15	E8	RW	Gamma Curve 15th Segment Input End Point 0xD0 Output Value
8D	SLOP	20	RW	Gamma Curve Highest Segment Slope - calculated as follows: SLOP[7:0] = (0x100 - GAM15[7:0]) × 4/3
8E	DNSTh	00	RW	De-noise Threshold In automatic mode, this register is updated automatically. In manual mode, this register is set by the user.
8F	EDGE0	00	RW	Sharpness (Edge Enhancement) Control 0 Bit[7:5]: Reserved Bit[4:0]: Sharpness (edge enhancement) strength control In automatic mode, this register is updated automatically. In manual mode, this register is set by the user.
90	EDGE1	08	RW	Sharpness (Edge Enhancement) Control 1 Bit[7:4]: Reserved Bit[3:0]: Threshold for edge detection
91	DNSOff	10	RW	Lower Limit of De-noise Threshold - effective in auto mode only
92	EDGE2	1F	RW	Sharpness (Edge Enhancement) Strength Upper Limit
93	EDGE3	01	RW	Sharpness (Edge Enhancement) Strength Lower Limit
94	MTX1	2C	RW	Matrix Coefficient 1
95	MTX2	24	RW	Matrix Coefficient 2
96	MTX3	08	RW	Matrix Coefficient 3
97	MTX4	14	RW	Matrix Coefficient 4
98	MTX5	24	RW	Matrix Coefficient 5
99	MTX6	38	RW	Matrix Coefficient 6
9A	MTX_Ctrl	9E	RW	Matrix Control Bit[7]: Matrix double ON/OFF selection Bit[6]: Reserved Bit[5]: Sign bit for MTX6 Bit[4]: Sign bit for MTX5 Bit[3]: Sign bit for MTX4 Bit[2]: Sign bit for MTX3 Bit[1]: Sign bit for MTX2 Bit[0]: Sign bit for MTX1
9B	BRIGHT	00	RW	Brightness

Table 6 Device Control Register List (Sheet 13 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
9C	CNST	40	RW	Contrast Normalized by 0x20
9D	RSVD	XX	–	Reserved
9E	UVADJ0	11	RW	Auto UV Adjust Control 0 Bit[7:4]: Auto UV adjust offset control 4 LSBs Bit[3:0]: Auto UV adjust threshold control
9F	UVADJ1	02	RW	Auto UV Adjust Control 1 Bit[7:3]: Auto UV adjust value Bit[2]: Reserved Bit[1]: Auto UV adjust stop control Bit[0]: Auto UV adjust offset control MSB
A0	SCAL0	00	RW	DCW Ratio Control Bit[7:4]: Reserved Bit[3:2]: Vertical down sampling select 00: Bypass 01: 1/2 vertical down sampling 10: 1/4 vertical down sampling 11: 1/8 vertical down sampling Bit[1:0]: Horizontal down sampling select 00: Bypass 01: 1/2 horizontal down sampling 10: 1/4 horizontal down sampling 11: 1/8 horizontal down sampling
A1	SCAL1	40	RW	Horizontal Zoom Out Control Horizontal zoom ratio = 0x40 / SCAL1
A2	SCAL2	40	RW	Vertical Zoom Out Control Vertical zoom ratio = 0x40 / SCAL2
A3-A5	RSVD	XX	–	Reserved
A6	SDE	00	RW	Special Digital Effect (SDE) Control Bit[7]: Reserved Bit[6]: Negative image enable Bit[5]: Gray scale image enable Bit[4]: V fixed value enable Bit[3]: U fixed value enable Bit[2]: Contrast/Brightness enable Bit[1]: Saturation enable Bit[0]: Hue enable
A7	USAT	40	RW	U Component Saturation Gain $U = U_0 \times USAT / 0x40$
A8	VSAT	40	RW	V Component Saturation Gain $V = V_0 \times VSAT / 0x40$
A9	HUECOS	80	RW	Cosine value × 0x80

Table 6 Device Control Register List (Sheet 14 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
AA	HUESIN	80	RW	|Sine value| × 0x80
AB	SIGN	06	RW	Sign Bit for Hue and Brightness Bit[7:4]: Reserved Bit[3]: Brightness sign bit Bit[2]: Reserved Bit[1]: Sign bit for HueSin (in Cr' equation) Bit[0]: Sign bit for HueSin (in Cb' equation) Hue Control: Cb' = Cos(A) × C_Cb + SIGN[0] × |Sin(A)| × C_Cr + 0x80 Cr' = Cos(A) × C_Cr + SIGN[1] × |Sin(A)| × C_Cb + 0x80 where C_Cb = Cb - 0x80 C_Cr = Cr - 0x80 Cos(A) = HUECOS[7:0] / 0x80, (-90 ≤ A ≤ 90) |Sin(A)| = HUESIN[7:0] / 0x80, (-90 ≤ A ≤ 90) Contrast/Brightness Control: $Y = (Y_0 - Y_{avg}) \times CNST / 0x20 + Y_{avg} + SIGN[3] \times BRIGHT$ where Y_{avg} value is the average image luminance and is automatically calculated by the sensor.
AC	DSPAuto	FF	RW	DSP Auto Function ON/OFF Control Bit[7]: AWB auto threshold control Bit[6]: De-noise auto threshold control 0: Manual mode - de-noise strength is set by register DNSTh (0x8E) 1: Automatic mode - de-noise strength is adjusted automatically and saved in register DNSTh (0x8E) Bit[5]: Sharpness (edge enhancement) auto strength control 0: Manual mode - sharpness is set by register EDGE0[4:0] (0x8F) 1: Automatic mode - sharpness is adjusted automatically and saved in register EDGE0[4:0] (0x8F) Bit[4]: UV adjust auto slope control Bit[3]: Auto scaling factor control (register SCAL0 (0xA0)) Bit[2]: Auto scaling factor control (registers SCAL1 (0xA1 and SCAL2 (0xA2)) Bit[1:0]: Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7725 uses a 28-ball Chip Scale Package 2 (CSP2). Refer to Figure 12 for package information, Table 7 for package dimensions and Figure 13 for the array center on the chip.

Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 12 OV7725-CSP2 Package Specifications

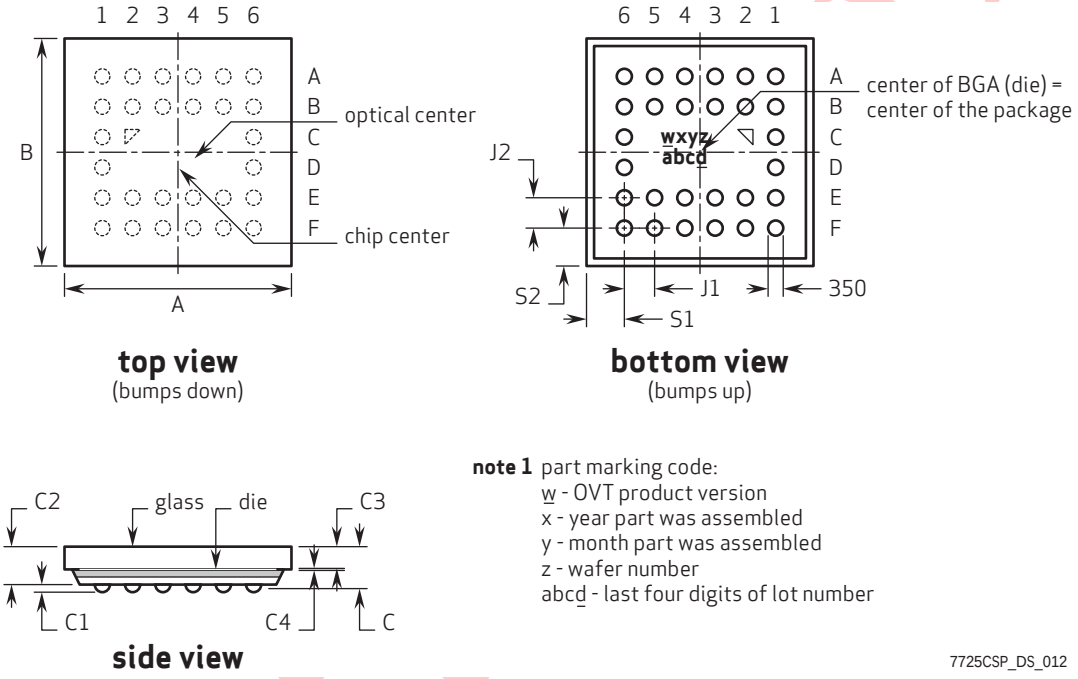
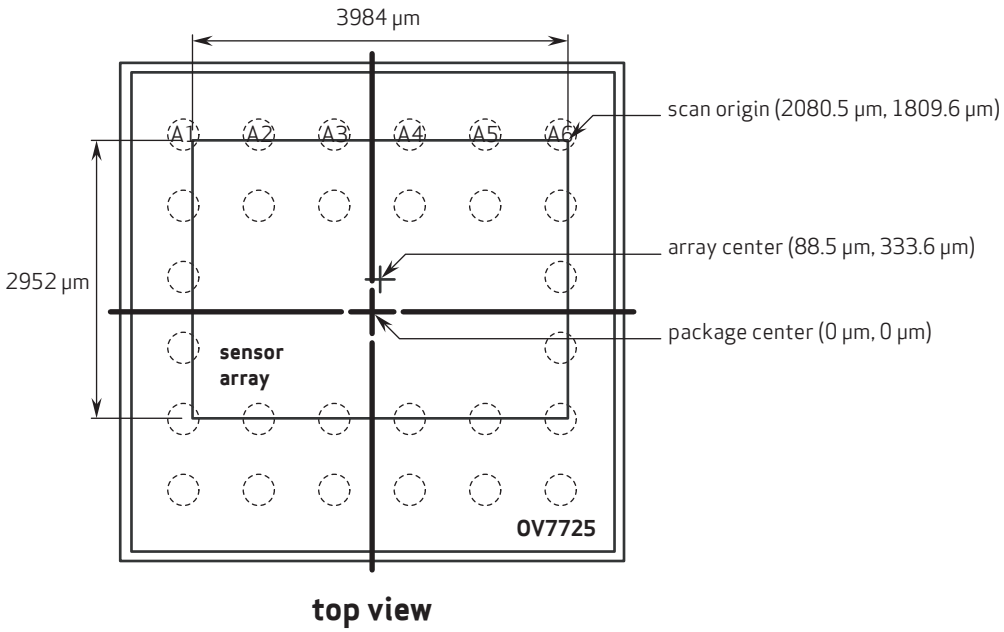


Table 7 OV7725-CSP2 Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package body dimension X	A	5320	5345	5370	µm
Package body dimension Y	B	5240	5265	5290	µm
Package height	C	845	905	965	µm
Ball height	C1	150	180	210	µm
Package body thickness	C2	680	725	770	µm
Cover glass thickness	C3	375	400	425	µm
Airgap between cover glass and sensor	C4	30	45	60	µm
Ball diameter	D	320	350	380	µm
Total pin count	N		28		
Pin count X-axis	N1		6		
Pin count Y-axis	N2		6		
Pins pitch X-axis	J1		800		µm
Pins pitch Y-axis	J2		750		µm
Edge-to-pin center distance analog X	S1	643	673	703	µm
Edge-to-pin center distance analog Y	S2	728	758	788	µm

Sensor Array Center

Figure 13 OV7725 Sensor Array Center



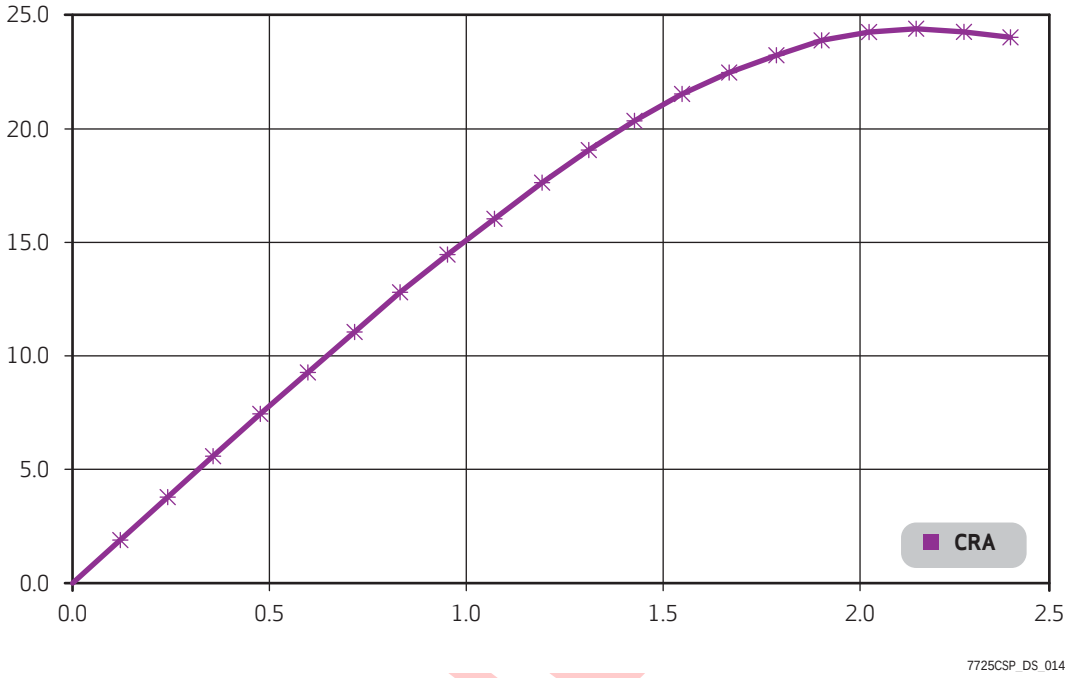
note1 this drawing is not to scale and is for reference only.

note2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

7725CSP_DS_013

Chief Ray Angle

Figure 14 OV7725 Chief Ray Angle



IR Reflow Ramp Rate Requirements

OV7725 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 15 IR Reflow Ramp Rate Requirements

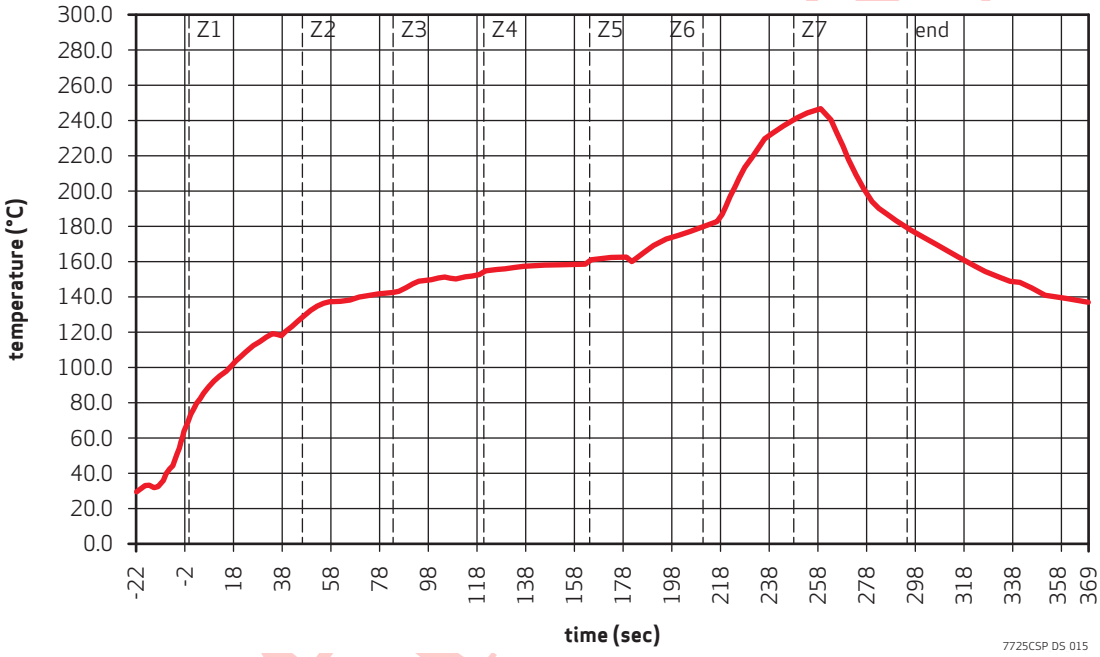


Table 8 Reflow Conditions

Condition	Exposure
Average ramp-up rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak temperature	245°C
Cool-down rate (peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV7725 Datasheet **Version:** 1.0

DESCRIPTION OF CHANGES

- Initial Release

REVISION CHANGE LIST

Document Title: OV7725 (CSP2) Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.1:

- In Table 6 on page 11, deleted “(see GREEN[7:6] (0x03) for AGC [9:8])” from register description
- In Table 6 on page 11, changed name, default value, R/W status and description of register 0x04 to “RSVD”, “XX”, “–”, and “Reserved”, respectively
- In Table 6 on page 11, changed default value of register VER (0x0B) from “20” to “21”
- In Table 6 on page 12, changed default value of register COM3 (0x0C) from “00” to “10”
- In Table 6 on page 12, changed default value of register COM4 (0x0D) from “00” to “41”
- In Table 6 on page 13, changed description of register bits COM7[5:4] (0x12) from:

  Bit[5]: ITU656 protocol ON/OFF selection
  Bit[4]: Reserved

  to:

  Bit[5]: BT.656 protocol ON/OFF selection
  Bit[4]: Sensor RAW
- In Table 6 on page 14, changed description of register bits COM9[6:4] (0x14) from:

  Bit[6:4]: Automatic Gain Ceiling - maximum AGC value
  000: 2x
  001: 4x
  010: 8x
  011: 16x
  100: 32x
  101 64x
  110: 128x
  111: Not allowed

  to:

  Bit[6:4]: Automatic Gain Ceiling - maximum AGC value
  000: 2x
  001: 4x
  010: 8x
  011: 16x
  100: 32x
  101 Not allowed
  110: Not allowed
  111: Not allowed
- In Table 6 on page 14, changed name, default value, and R/W status of register 0x16 from “RSVD”, “XX”, and “–” to “REG16”, “00”, and “RW”, respectively

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 6 on page 14, changed description of register 0x16 from “Reserved” to:

  Register 16

  Bit[7]: Bit shift test pattern options

  Bit[6:0]: Reserved
- In Table 6 on page 14, changed description of register 0x17 from “Horizontal Sensor Size” to “Horizontal Frame (HREF column) Start 8 MSBs (2 LSBs are at HREF[5:4])”
- In Table 6 on page 14, changed description of register 0x18 from “Horizontal Frame (HREF column) end high 8-bit (low 2 bits are at HREF[1:0])” to “Horizontal Sensor Size (2 LSBs are at HREF[1:0])”
- In Table 6 on page 14, changed description of register 0x19 from “Vertical Frame (row) start high 8-bit (low 1 bit is at HREF[6])” to “Vertical Frame (row) Start 8 MSBs (1 LSB is at HREF[6])”
- In Table 6 on page 14, changed description of register 0x1A from “Vertical Sensor Size” to “Vertical Sensor Size (1 LSB is at HREF[2])”
- In Table 6 on page 15, changed default value of register COM11 (0x20) from “04” to “10”
- In Table 6 on page 15, changed name, default value, and R/W of register 0x28 from “RSVD”, “XX”, and “–” to “REG28”, “00”, and “RW”, respectively
- In Table 6 on page 15, changed description of register 0x28 from “Reserved” to:

  Register 28

  Bit[7:1]: Reserved

  Bit[0]: Selection on the number of dummy rows, N
- In Table 6 on page 16, changed default value of register HREF (0x32) from “80” to “00”
- In Table 6 on page 16, changed description of register DM_LNL (0x33) from “Dummy Line Low 8 Bits” to “Dummy Row Low 8 Bits”
- In Table 6 on page 16, changed description of register DM_LNH (0x34) from “Dummy Line High 8 Bits” to “Dummy Row High 8 Bits”
- In Table 6 on page 16, changed default value of register COM13 (0x3E) from “F3” to “E2”
- In Table 6 on page 16, changed description of register COM13 (0x3E) from:

  Common Control 13

  Bit[7]: Analog processing channel BLC ON/OFF control

  Bit[6]: ADC channel BLC ON/OFF control

  Bit[5:0]: Reserved

  to:

  Common Control 13

  Bit[7]: BLC enable

  Bit[6]: ADC channel BLC ON/OFF control

  Bit[5]: Analog processing channel BLC ON/OFF control

  Bit[4:3]: Reserved

  Bit[2]: ABLC gain trigger enable

  Bit[1:0]: Reserved

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 6 on page 17, changed names of registers 0x46, 0x47, 0x48, 0x49, 0x4A, and 0x4B from “LCC0”, “LCC1”, “LCC2”, “LCC3”, “LCC4”, and “LCC5” to “LC_CTR”, “LC_XC”, “LC_YC”, “LC_COEF”, “LC_RADI”, and “LC_COEFB”
- In Table 6 on page 17, changed description of register 0x47 from “Lens Correction Option 1 – X Coordinate of Lens Correction Center Relative to Array Center” to:

  X Coordinate of Lens Correction Center Relative to Array Center

  Bit[7]: Sign bit
  0: Positive
  1: Negative

  Bit[6:0]: X coordinate of lens correction center relative to array center
- In Table 6 on page 17, changed description of register 0x48 from “Lens Correction Option 2 – Y Coordinate of Lens Correction Center Relative to Array Center” to:

  Y Coordinate of Lens Correction Center Relative to Array Center

  Bit[7]: Sign bit
  0: Positive
  1: Negative

  Bit[6:0]: Y coordinate of lens correction center relative to array center
- In Table 6 on page 17, changed description of register 0x49 from “Lens Correction Option 3” to “Lens Correction Coefficient”
- In Table 6 on page 17, changed description of register 0x4A from “Lens Correction Option 4 – radius ...” to “Lens Correction Radius – radius ...”
- In Table 6 on page 17, changed description of register 0x4B from “Lens Correction Option 5 (effective ...” to “Lens Correction B Channel Compensation Coefficient (effective ...”
- In Table 6 on page 18, changed name of register 0x4C from “LCC6” to “LC_COEFR”
- In Table 6 on page 18, changed description of register 0x4C from “Lens Correction Option 6 (effective ...” to “Lens Correction R Channel Compensation Coefficient (effective ...”
- In Table 6 on page 18, changed default value of register AREF0 (0x4E) from “F0” to “EF”
- In Table 6 on page 18, changed default value of register AREF2 (0x50) from “30” to “60”
- In Table 6 on page 18, changed default value of register AREF6 (0x54) from “3A” to “7A”
- In Table 6 on page 19, changed description of register bit DSP_Ctrl1[5] (0x64) from “YUV444 to 422 UV channel option selection” to “SDE enable”
- In Table 6 on page 19, changed description of register bits DSP_Ctrl2[3:0] (0x65) from:

  Bit[3:0]: Scaling control

  to:

  Bit[3]: Vertical DCW enable
  Bit[2]: Horizontal DCW enable
  Bit[1]: Vertical zoom out enable
  Bit[0]: Horizontal zoom out enable

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 6 on page 19, changed description of register DSP_Ctrl4 (0x67) from:

  DSP Control Byte 4

  to:

  DSP Control Byte 4

  Bit[7:3]: Reserved
  Bit[2]: AEC selection
  0: Before gamma
  1: After gamma
  Bit[1:0]: Output selection
  00: YUV or RGB
  01: YUV or RGB
  10: RAW8
  11: RAW10

- In Table 6 on page 20, changed description of register AWBCtrl1 (0x69) from:

  AWB Control 1

  to:

  AWB Control 1

  Bit[7:4]: Reserved
  Bit[3]: G gain enable
  0: AWB adjusts R and G gain
  1: AWB adjusts R, G, and B gain
  Bit[2]: Max color gain
  0: Max color gain is 2x
  1: Max color gain is 4x
  Bit[1]: Reserved
  Bit[0]: AWB mode select
  0: Advanced AWB mode
  1: Normal AWB mode

- In Table 6 on page 21, changed description of register EDGE0 (0x8F) from:

  Edge Enhancement Control 0

  Bit[7:5]: Reserved
  Bit[4:0]: Edge enhancement strength control

  to

  Sharpness (Edge Enhancement) Control 0

  Bit[7:5]: Reserved
  Bit[4:0]: Sharpness (edge enhancement) strength control

- In Table 6 on page 21, changed description of register EDGE1 (0x90) from:

  Edge Enhancement Control 1

  Bit[7:4]: Reserved
  Bit[3:0]: Edge enhancement threshold control

  to:

  Sharpness (Edge Enhancement) Control 1

  Bit[7:4]: Reserved
  Bit[3:0]: Sharpness (edge enhancement) threshold detection

- In Table 6 on page 21, changed description of register 0x92 from “Edge Enhancement Strength Low Point Control” to “Sharpness (Edge Enhancement) Strength Upper Limit”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 6 on page 21, changed description of register 0x93 from “Edge Enhancement Strength High Point Control” to “Sharpness (Edge Enhancement) Strength Lower Limit”
- In Table 6 on page 22, added “gain × 0x20” to description of register CNST (0x9C)
- In Table 6 on page 22, changed name, default value, R/W status and description of register 0x9D to “RSVD”, “XX”, “–”, and “Reserved”, respectively
- In Table 6 on page 22, changed description of register SCAL0 (0xA0) from “Scaling Control 0” to:

  DCW Ratio Control

  Bit[7:4]: Reserved
  Bit[3:2]: Vertical down sampling select
  00: Bypass
  01: 1/2 vertical down sampling
  10: 1/4 vertical down sampling
  11: 1/8 vertical down sampling
  Bit[1:0]: Horizontal down sampling select
  00: Bypass
  01: 1/2 horizontal down sampling
  10: 1/4 horizontal down sampling
  11: 1/8 horizontal down sampling
- In Table 6 on page 22, changed description of register SCAL1 (0xA1) from “Scaling Control 1 – for horizontal scaling control” to:

  Horizontal Zoom Out Control

  $$\text{Horizontal zoom ratio} = \frac{0x40}{SCAL1[7:0]}$$
- In Table 6 on page 22, changed description of register SCAL2 (0xA2) from “Scaling Control 2 – for vertical scaling control” to:

  Vertical Zoom Out Control

  $$\text{Vertical zoom ratio} = \frac{0x40}{SCAL2[7:0]}$$
- In Table 6 on page 23, changed description of register SDE (0xA6) from “Special Digital Effect Control” to:

  Special Digital Effect Control

  Bit[7]: Reserved
  Bit[6]: Negative image enable
  Bit[5]: Gray scale image enable
  Bit[4]: V fixed value enable
  Bit[3]: U fixed value enable
  Bit[2]: Contrast/Brightness enable
  Bit[1]: Saturation enable
  Bit[0]: Hue enable
- In Table 6 on page 23, added “gain × 0x40” to description of registers USAT (0xA7) and VSAT (0xA8)

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 6 on page 23, changed name of register 0xA9 from “HUE0” to “HUECOS”
- In Table 6 on page 23, changed name of register 0xAA from “HUE1” to “HUESIN”
- In Table 6 on page 23, changed description of register 0xA9 from “Hue Control 0” to “Cosine value × 0x80”
- In Table 6 on page 23, changed description of register 0xAA from “Hue Control 1” to “Sine value × 0x80”
- In Table 6 on page 23, changed description of register SIGN (0xAB) from:

  Sign Bit for Hue and Contrast

  Bit[7:4]: Reserved
  Bit[3:2]: Contrast sign bit
  Bit[1:0]: Hue sign bit

  to:

  Sign Bit for Hue and Brightness

  Bit[7:4]: Reserved
  Bit[3]: Brightness sign bit
  Bit[2]: Reserved
  Bit[1]: Sign bit for HueSin (in Cr’ equation)
  Bit[0]: Sign bit for HueSin (in Cb’ equation)
- In Table 6 on page 23, changed description of register bit DSPAuto[5] (0xAC) from “Edge enhancement auto strength control” to “Sharpness (edge enhancement) auto strength control”
- In Figure 12 on page 24, changed underlined ‘w’ in the drawing and in the notes

REVISION CHANGE LIST

Document Title: OV7725 (CSP2) Datasheet **Version:** 1.2

DESCRIPTION OF CHANGES

The following changes were made to version 1.1:

- Under Key Specifications on page 1, changed Sensitivity from “TBD” to| “3.0 V/(Lux • sec)”
- Under Key Specifications on page 1, changed S/N Ratio from “TBD” to| “50 dB”
- Under Key Specifications on page 1, changed Dynamic Range from “TBD” to| “60 dB”
- Under Key Specifications on page 1, changed Dark Current from “TBD” to| “40 mV/s”
- Under Key Specifications on page 1, changed Well Capacity from “TBD” to| “26 Ke^-”
- In Table 6 on page 11, changed description of register bits COM2[3:2] (0x09) to “Reserved”
- In Table 6 on page 12, changed description of register bits COM5[3:2] (0x0E) from:

  Bit[3:2]: Auto frame rate active point control
  - 00: Add frame when AGC reaches 2x gain
  - 01: Add frame when AGC reaches 4x gain
  - 10: Add frame when AGC reaches 8x gain
  - 11: Add frame when AGC reaches 16x gain

  to:

  Bit[3:2]: Auto frame rate active point control
  - 00: Not allowed
  - 01: Add frame when AGC reaches 4x gain
  - 10: Add frame when AGC reaches 8x gain
  - 11: Add frame when AGC reaches 16x gain

REVISION CHANGE LIST

Document Title: OV7725 (CSP2) Datasheet **Version:** 1.3

DESCRIPTION OF CHANGES

The following changes were made to version 1.2:

- Under Key Specifications on page 1, changed specification for Analog Power Supply from “3.0V to 3.3V” to “3.0V to 3.6V” and deleted footnote a from I/O Power Supply specification
- Under Image Sensor Array section on page 3, changed first sentence from “... array of 656 x 488 pixels for a total of 320,128 pixels ...” to “... array of 664 x 490 pixels for a total of 325,360 pixels ...”
- In Table 1 on page 4, changed Pad Type for pad 27 from “Input” to “Input (0)[a]” and added “and should be grounded when not used” to footnote a.
- In Table 4 on page 6, changed Min specification for DC supply voltage – I/O from “2.5” to “1.7”
- In Table 4 on page 6, added “See Note [a]” to Condition of DC supply voltage – digital core parameter and to Condition of DC supply voltage – I/O parameter
- In Table 4 on page 6, added footnote a, “V_{DD-IO} should not be lower than 2.45V when using the internal regulator for V_{DD-C} (1.8V). When not using the internal regulator, V_{DD-C} requires external 1.8V power that must not be higher than V_{DD-IO}.”
- In Table 4 on page 6, changed Typ value for Active (operating) current (I_{DDA}) from “10 + 8[c]” to “10 + 19[c]”
- In Table 4 on page 6, changed footnote b from “$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, ...” to “$I_{DDA} = \Sigma\{I_{DD-C} + I_{DD-A}\}$, ...”
- In Table 4 on page 6, changed footnote c from “I_{DD-C} = 10mA, I_{DD-A} = 8mA, without loading” to “I_{DD-C} = 10mA, I_{DD-A} = 19mA, without loading”
- In Table 4 on page 6, changed Max value for Input voltage LOW (V_{IL}) from “0.3 x V_{DD-IO}” to “0.2 x V_{DD-IO}”
- On page 9, changed four callouts in Figure 6 and five callouts in Figure 7
- In Table 6 on page 12, made extensive changes to descriptions of registers 0x00 (GAIN), 0x01 (BLUE), 0x02 (RED), and 0x03 (GREEN)
- In Table 6 on page 12, changed description of registers BAVG (0x05), GAVG (0x06), and RAVG (0x07) from “U/B Average Level”, “Y/Gb Average Level”, and V/R Average Level” to “B Average Level”, “G Average Level”, and “R Average Level”, respectively
- In Table 6 on page 12, changed description of register AECH (0x08) from “Automatically updated based on chip output format” to “Automatically updated when AEC is enabled”

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 6 on page 13, added “(see register DSP_Ctrl3[7] (0x66))” to description of register bit COM3[4] (0x0C)
- In Table 6 on page 13, changed description of register bit COM3[2] (0x0C) from “Tri-state option for output clock at power-down period” to “Tri-state option for output clock including PCLK, HREF, and VSYNC at power-down period”
- In Table 6 on page 13, added the following to description of register bit COM5[6] (0x0E):
  - 0: Normal
  - 1: Fast
- In Table 6 on page 13, changed the description of register bit COM5[0] (0x0E) to Reserved
- In Table 6 on page 14, made extensive changes to descriptions of registers 0x10 (AEC) and 0x11 (CLKRC)
- In Table 6 on page 15, made extensive changes to description of register 0x13 (COM8)
- In Table 6 on page 16, changed description of register bit COM10[2] (0x15) to Reserved
- In Table 6 on page 16, added “should be set to 1 for bit shift test pattern” to description of register bit REG16[7] (0x16)
- In Table 6 on page 16, made extensive changes to descriptions of registers 0x17 (HSTART), 0x18 (HSIZE), 0x19 (VSTRT), and 0x1A (VSIZE)
- In Table 6 on page 17, deleted “, N” from description of register bit REG28[0] (0x28)
- In Table 6 on page 17, made extensive changes to descriptions of registers 0x29 (HOutSize) and 0x2C (VOutSize)
- In Table 6 on page 17, added “should set to 1 in mirror mode” to description of register bit HREF[7] (0x32)
- In Table 6 on page 17, changed description of register DM_LNL (0x33) to “Low 8 Bits of the Number of Dummy Rows”
- In Table 6 on page 17, changed description of register DM_LNH (0x34) to “High 8 Bits of the Number of Dummy Rows”
- In Table 6 on page 18, deleted “Analog Process” from description of registers Off_B (0x39), Off_R (0x3A), Off_Gb (0x3B), and Off_Gr (0x3C)
- In Table 6 on page 18, deleted “compensation” from description of register bits COM12[5:0] (0x3D)
- In Table 6 on page 18, changed name, default value, R/W type, and description of register 0x40 to RSVD, XX, –, and Reserved, respectively
- In Table 6 on page 18, changed description of register bits COM16[1:0] (0x41) to “Reserved”
- In Table 6 on page 18, made extensive changes to descriptions of registers 0x42 (TGT_B), 0x43 (TGT_R), 0x44 (TGT_Gb), and 0x45 (TGT_Gr)
- In Table 6 on page 20, made extensive changes to description of register 0x4D (FixGain)

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 6 on page 20, changed name, default value, R/W type, and description of register 0x4E to RSVD, XX, –, and Reserved, respectively
- In Table 6 on page 20, changed description of register bits AREF1[7:4] and AREF1[1:0] 0x4F to Reserved
- In Table 6 on page 20, changed description of register bit AREF[3] from “Internal regulator ON/OFF selection” to “Internal regulator bypass selection” and added description for ‘0’ and ‘1’
- In Table 6 on page 20, changed name, default value, R/W type, and description of registers 0x50 to 0x53 to RSVD, XX, –, and Reserved, respectively
- In Table 6 on page 20, changed description of register AREF6 (0x54) to:

  Analog Reference Control

  Bit[7]: Internal power supply control for power down mode - should be set to 0 when internal regulator is used
  - 0: Enable
  - 1: Bypass

  Bit[6:0]: Reserved
- In Table 6 on page 20, changed name, default value, R/W type, and description of register 0x55 to RSVD, XX, –, and Reserved, respectively
- In Table 6 on page 20, changed description of register bits AWB_Ctrl0[4:0] (0x63) to Reserved
- In Table 6 on page 21, changed description of register bits DSP_Ctrl1[1:0] (0x64) to:

  Bit[1]: Black defect pixel auto correction ON/OFF
  Bit[0]: White defect pixel auto correction ON/OFF
- In Table 6 on page 21, made extensive changes to description of register 0x66 (DSP_Ctrl3)
- In Table 6 on page 21, changed description of register bit DSP_Ctrl4[2] (0x67) from “AEC selection” to “AEC reference point selection”
- In Table 6 on page 21, changed description of register bit AWBCtrl1[3] (0x69) to:

  Bit[3]: G gain enable
  - 0: AWB adjusts R and G gain only
  - 1: AWB adjusts R, G, and B gain
- In Table 6 on page 23, changed description of register bits EDGE1[3:0] (0x90) from “Sharpness (edge enhancement) threshold detection” to “Threshold for edge detection”
- In Table 6 on page 23, changed description of register DNSOff (0x91) to “Lower Limit of De-noise Threshold - effective in auto mode only”
- In Table 6 on page 23, deleted “Control” from the description of register BRIGHT (0x9B)
- In Table 6 on page 24, changed description of register CNST (0x9C) to “Contrast Normalized by 0x20”
- In Table 6 on page 24, made extensive changes to description of register 0xA1 (SCAL1)

DESCRIPTION OF CHANGES (CONTINUED)

- In Table 6 on page 20, changed name, default value, R/W type, and description of registers 0xA3 and 0xA4 to RSVD, XX, –, and Reserved, respectively
- In Table 6 on pages 24 and 25, made extensive changes to description of register 0xA2 (SCAL1), 0xA7 (USAT), 0xA8 (VSAT), 0xAA (HUESIN), and 0xAB (SIGN)
- In Table 6 on page 24, added “(SDE)” to description of register SDE (0xA6)
- In Table 6 on page 26, made extensive changes to description of register 0xAC (DSPAuto)

REVISION CHANGE LIST

Document Title: OV7725 (CSP2) Datasheet **Version:** 1.31

DESCRIPTION OF CHANGES

The following changes were made to version 1.3:

- In Table 6 on page 13, changed description of register bit COM3[7] (0x0C) to “Reserved”

REVISION CHANGE LIST

Document Title: OV7725 (CSP2) Datasheet **Version:** 1.4

DESCRIPTION OF CHANGES

The following changes were made to version 1.31:

- Under Key Specifications on page 1, changed Sensitivity from “3.0 V/(Lux • sec)” to “3.8 V/(Lux • sec)”
- In Table 6 on page 12, changed R/W for registers 0x05, 0x06, and 0x07 from “RW” to “R”
- In Table 6 on page 12, changed default value for register 0x03 from “00” to “80”
- In Table 6 on page 12, changed default value for register 0x09 from “01” to “00”
- In Table 6 on page 13, changed default value for register 0x0E from “01” to “79”
- In Table 6 on page 13, changed default value for register 0x0F from “43” to “A9”
- In Table 6 on page 14, changed default value for register 0x10 from “40” to “00”
- In Table 6 on page 14, changed default value for register 0x11 from “80” to “00”
- In Table 6 on page 15, changed default value for register 0x13 from “8F” to “CF”
- In Table 6 on page 15, changed default value for register 0x14 from “4A” to “40”
- In Table 6 on page 16, changed default value for register 0x17 from “23 (VGA)” to “26 (VGA)”
- In Table 6 on page 17, changed default value for register 0x24 from “75” to “58”
- In Table 6 on page 17, changed default value for register 0x25 from “63” to “48”
- In Table 6 on page 17, changed default value for register 0x26 from “D4” to “C3”
- In Table 6 on page 17, changed R/W for register 0x2F from “RW” to “R”
- In Table 6 on page 18, changed default value for register 0x41 from “08” to “00”
- In Table 6 on page 20, changed default value for register 0x60 from “80” to “00”
- In Table 6 on page 20, changed default value for register 0x61 from “80” to “05”
- In Table 6 on page 21, changed default value for register 0x64 from “1F” to “BF”
- In Table 6 on page 22, changed default value for register 0x76 from “FF” to “00”
- In Table 6 on page 22, changed default value for register 0x77 from “FF” to “10”